Design Challenges in the use of Silicon Carbide JFETs in Matrix Converter Applications

Lee Empringham, *Member, IEEE,* Liliana de Lillo, *Member, IEEE,* Martin Schulz, *Member, IEEE,*

***Abstract*—This paper investigates some of the challenges encountered during the implementation of a Silicon Carbide JFET matrix converter which has been designed to meet a specific power density of 20kW/litre with forced air cooling. After a brief introduction to the main features of the hardware implementation of the power converter, an insight into the control strategy and controller platform adopted is given with a particular attention to the issues relating to the high switching frequencies on the controller requirements and the performance implications of the gate drive circuitry. An analysis of the results which show the effects of gate driver and controller induced commutation time limitations on the output waveform quality is presented. Wide bandgap semiconductor devices offer the power electronic engineer new opportunities for high speed, high efficiency designs but these devices cannot be used as a simple like for like replacements and as such the whole converter system needs to be looked at.**

Keywords: AC - AC power conversion; Digital Control

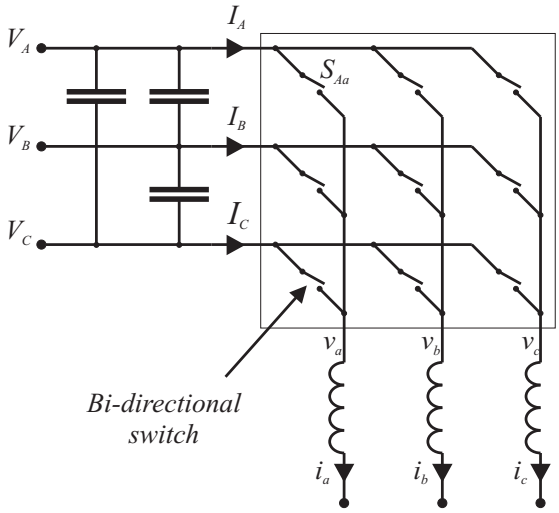

Fig. 1. Schematic diagram of the three phase to three phase matrix converter structure

I. Introduction

One of the megatrends in power electronic development is reducing cost/kW installed and increase the volumetric power densities. Inherently, the matrix converter provides a solution without DC-Link capacitors that add up to 15% to the BOM and account for a major fraction of the volume of an industrial inverter[1]. Additionally, wound filter components are expensive and should be reduced as much as possible. This can be done by increasing the switching frequency. This however will reduce the power/volume ratio if classical IGBTs are considered as the higher switching losses will lead to reduced output power in a given design. The SiC-switch can be used to increase the switching frequency without sacrificing too much of the thermal budget to switching losses.

A conventional direct matrix converter circuit [2] is shown in Figure 1, which consists of a three by three matrix of bidirectional switches. These switches can be modulated in such a way as to generate the desired output voltage and input current. Assuming a sinusoidal input supply and sinusoidal output demand, sinusoidal input currents can be drawn. The input displacement factor can be controlled (typically to 1) to some extent depending on the modulation strategy used, the output power factor and the modulation index required. An input filter is included to filter the high frequency switching components from the input current. A high speed input and output diode bridge is also used as an over-voltage clamp circuit. The latter is used to prevent ringing of the input filter when the supply is powered and to provide a path for the load current when a condition such as an open circuit of the load should occur as no freewheeling diodes are used in this power converter topology. An alternative to the direct matrix converter, the indirect matrix converter using vertical SiC JFETS, has been addressed in [3].

The matrix converter discussed in this paper has the conventional circuit structure for a direct matrix converter as mentioned above but it is made of normally ON Silicon Carbide (SiC) JFET bidirectional switches [4]configured in a three by three matrix of bi-directional switches.

Figure 2 describes how each of the bidirectional switches is structured using two anti-series connected, 1200V, 40A SiC JFETs with an intrinsic body diode in antiparallel which eliminates the need of introducing an extra die for the diode as it would be the case for all silicon IGBT based converters.

At the time of the design of the presented converter SiC MOSFET devices still suffered from a stability issue with gate oxides. The JFET's cell structure eliminates the need of this particular oxide layer with the consequence of being a

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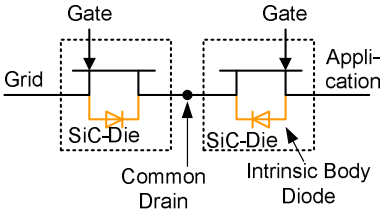

Fig. 2. Diagram to show how the bi-directional switches within the converter are implemented

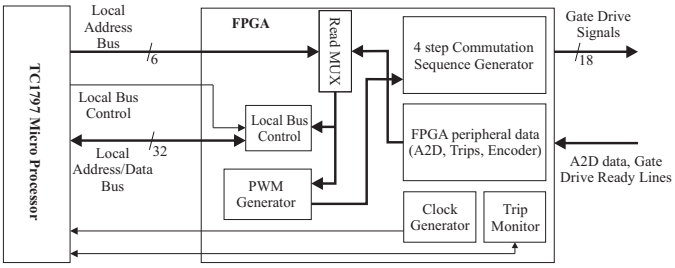

Fig. 3. Schematic of the controller developed for the demonstrator

normally on device. Additionally, the effort needed to properly drive the SiC JFET is far less than for a MOSFET. It is recommended that a typical CREE SiC MOSFET should be driven using a bipolar, +20V/-5V power rails whereas the SiC JFET, although a lower on-state resistance can be obtained using a +2V/-18V supply, can be driven by a single 18V supply, thus simplifying the power supply requirements of the system. The particular challenge for the use of SiC JFETs is getting the system started properly, ensuring that control supply is available before the grid is connected since they are a normally-on device. A controllable input contactor arrangement or simple battery backup cell for the control electronics could be used to solve this problem. Much of the existing literature on the protection of normally-on JFETs is specific to the voltage source inverter topology. Applicable solutions to the matrix converter often make use of very fast isolated power supplies in order to ensure that the gate is powered to a safe state within a few microseconds in order to prevent catastrophic results such as in [5] and in [6] where a fast negative gate voltage is created using charge pumps. In [7] the speed of the proposed gate drive power supply is based on the analysis and measurement of avalanche and short circuit capabilities of different JFET chips. Self protection techniques are described in [8][9] and [10] where in [8], a negative supply voltage is created whenever the main bus voltage is present, [9] reports an additional turn-off circuit within the gate driver which keeps the device off if the gate drive power supply fails and [10] describes a self-powered gate drive which utilizes the drain-source voltage of the JFET to provide the necessary power.

The use of SiC devices has been reported for different applications in the literature. The potential improvements regarding the system efficiency and performance are reported in [11][12][13] and [14]. In [15] a high power density SiC JFET based automotive inverter system is reported. These highlight the continuing work to investigate and utilize these high speed devices.

The use of SiC devices has permitted a different hardware and control implementation approach from the common all silicon matrix converter. The main advantage of the use of high speed switching devices in the hardware implementation is the reduction in size of the passive components, especially in the input filter. The target power density of the demonstrator converter was 20kW/litre. The higher switching speeds that SiC devices can offer is an important aspect which contributes to hardware and software implications for the design and control of this converter. At higher switching frequencies however, issues such as digital controller resolution and the effect of stray inductances become more dominant and result in waveform distortion and overvoltages at turning on and off of the devices respectively.

After the high speed control strategy and the control platform implementation is introduced, this paper investigates the performance of the converter in terms of quality of output currents which relates to the chosen switching frequency and the commutation times set by the commutation technique implemented. Experimental results are presented to highlight the effect of the commutation times limitations and considerations on the results are drawn considering the importance of such a compact hardware layout.

II. Digital Control Implementation and Issues

Due to the higher potential switching speeds available when using silicon carbide devices, it was desirable to increase the system switching frequency in order to minimize the volume used by the input filter passive components and hence maximize the volumetric power density of the converter.

A. Controller

Currently available micro-controllers are typically able to control converter structures such as inverters but there are none that can inherently control a matrix converter. For this reason, it is now commonplace to use a solution based on a digital signal processor (DSP) or micro-controller connected to a field programmable gate array (FPGA). The low level converter control functionality is implemented in the FPGA and the high level modulation and control calculations are performed using the Micro-controller. A schematic of the controller is shown in Figure 3. In this instance, the Infineon TC1797 micro-controller together with a MicroSemi SoC (Formerly Actel) A3P400 FPGA was used. The micro-controller was chosen for its high temperature operation and its ability to perform floating point calculations.

The FPGA is responsible for:

- The space vector PWM generator
- Bi-directional switch current commutation sequencing
- The analog to digital converter (A2D) interface
- Trip monitoring

The micro controller is connected to the FPGA via the high speed external memory interface. During normal operation,

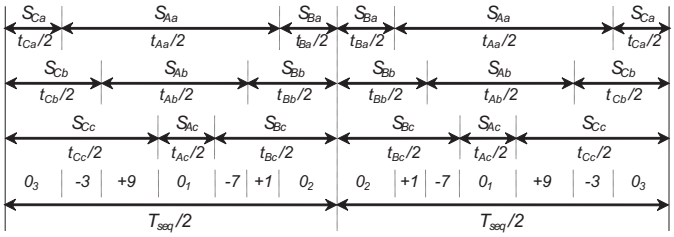

Fig. 4. Typical space vector sequence

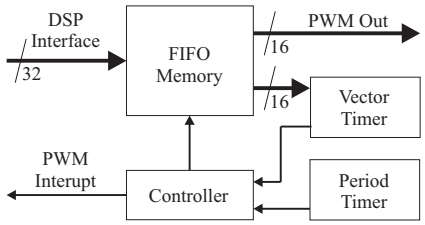

Fig. 5. Schematic diagram of the space vector PWM generator

the PWM generator contained within the FPGA as well as generating the desired vector timings, also triggers an interrupt within the micro-controller. During this interrupt, the most recent A2D information is transferred from the FPGA to the micro controller and is used in order to calculate the desired PWM vector timings that will be used for the next PWM interrupt. After the calculations have been performed the PWM data is then transferred to the PWM generator in the FPGA.

The PWM signals are then sent to the current commutation sequencing unit which is used to perform a safe commutation of the load current from one bi-directional switch to another.

The A2D interface is sampled at 500kHz. The load current measurements are taken from shunt resistors which are integrated into the power module and are used for the micro controller control algorithm, over-current protection and the direction information is used in the commutation sequencing system.

B. PWM Generation

Simulations during the design phase showed that a good compromise between the reduction of the passive component size whilst keeping the switching losses to an acceptable level would be a switching frequency between 50kHz and 100kHz. The minimum target switching frequency for the converter therefore needed to be greater than 50kHz in order to reduce the passive component sizes to required volume. The space vector modulation technique [16][17] is used to control the switching of the converter. Figure 4 shows a typical space vector sequence using three zero vectors where, S_{Xy} denotes the bidirectional switch connected between input phase X and output phase y to be on, for a time of t_{Xy} seconds. The key used here to indicate the devices in the switching matrix is the same as shown in Figure 1.

Since space vectors and vector times are calculated by the micro controller, a PWM generator which directly accepts this vector information has been implemented within the FPGA. Space vector PWM implementations typically need to convert the space vector time and vector information into the times needed by carrier based PWM generators. The use of a space vector PWM generator removes this extra calculation overhead from the control system. Figure 5 shows a schematic diagram of the PWM generator. It consists mainly of a first-in, first-out (FIFO) memory block, two timers and control logic. Firstly, the period timer is used to fix the PWM period and generate an interrupt for the micro-controller at the beginning of each period in order to perform the calculations at the required point. After the next set of modulation calculations have been completed. The micro-controller then writes a series of space-vector words to the FIFO memory which directly correspond to the required switching state of the converter together with a time for each of the vectors. The vectors and times are written in the order that they are to be used. At this point, the vector sequence and a time for each vector is now stored in order on the FIFO memory. At the beginning of the next PWM period, the vectors are clocked out of the FIFO, one by one. The process is paused at each vector for the previously written vector time for that vector. This process is controlled by the vector timer. In this way, the PWM sequence is then re-constructed according to the desired modulation strategy.

It was not possible to perform the matrix converter modulation and control calculations using the chosen micro controller at the desired 50kHz. The modulation calculations, grid synchronization, motor control and debug / user interface functions were performed at a frequency of 5kHz and the effective switching frequency of the power stage was increased. This was done by reducing the space vector times in the standard sequence by a factor of 10 and then the space vector sequence was output 10 times to the PWM generator. In this way, total time for each individual vector was maintained whilst increasing the effective switching frequency. Because of the rounding of the vector times, the original 20ns FPGA resolution effectively became equivalent to a PWM resolution of 200ns. This may affect waveform quality if high input or output frequencies are required.

Whilst the PWM update frequency, or the modulation frequency is now 5kHz, the effective switching frequency of the power section has been increased to 50kHz. From a control point of view, the limitation is still the 5kHz update frequency but from the point of view of the switching harmonics that are to be filtered by the passive components, The 50kHz switching frequency is more important. In this way, the passive component volume could be minimized. A 5kHz modulation frequency may not be adequate for many high bandwidth applications but since the demonstrator was intended to only use an input frequency of 50Hz, and a similar motor output frequency and as such, this was deemed to be acceptable.

C. Commutation

With high speed devices and a high switching frequency, the sequencing of the gate drive signals becomes more critical. The first issue with current commutation is to provide uninterrupted path for the load current whilst being certain not to create a short circuit of the input phases in order to

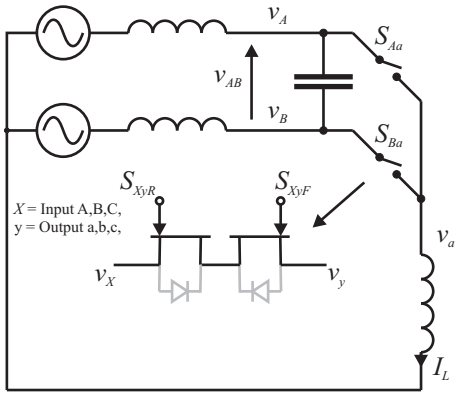

Fig. 6. Diagram of a two phase to single phase matrix converter

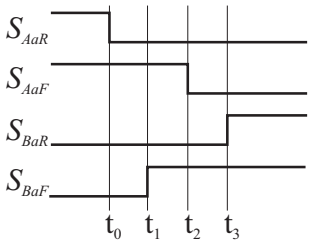

Fig. 7. Gate driver timing diagram for the four step commutation process

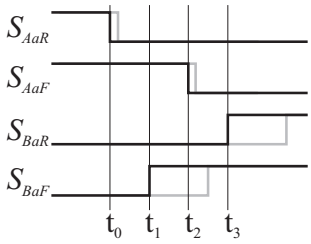

Fig. 8. Gate driver timing diagram for the four step commutation process where the falling edge delay is less than the rising edge delay

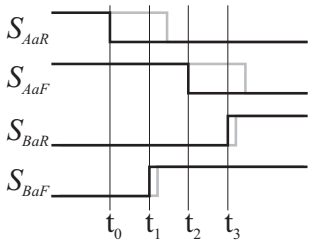

Fig. 9. Gate driver timing diagram for the four step commutation process where the rising edge delay is less than the falling edge delay

create safe commutation of the current from one bi-directional switch to another. There are many ways of implementing a suitable commutation strategy and each have advantages and disadvantages from simple dead-time based control [18] strategies which use specific hardware implementations, implementations which rely on specific PWM strategies and input voltage configurations [19] to advanced two step [20][21] and one step [22] strategies.

The 4-step current commutation method [23] was chosen for the implementation of the converter because of the reliability and robustness to errors in current direction information [24]. For explanation purposes, Figure 6 shows a two phase to single phase matrix converter and its operation is as follows:

For the following explanation, it is assumed that both devices in switch S_{Aa} are gated and the load current is in the direction shown. When a commutation to switch S_{Ba} is desired, the direction of the current is used to determine which device in S_{Aa} is not conducting in the forward direction. This device is then turned off and the current commutates to the internal body diode of the outgoing device. The same current direction information is then used to turn on the device in S_{Ba} that will conduct the load current in the forward direction. The remaining device in S_{Aa} is then turned off and finally, the remaining device in S_{Ba} is then turned on. A timing diagram to highlight this is shown in Figure 7.

The four step commutation process was chosen mainly for two reasons. Firstly it is considered to be one of the more robust commutation techniques [24] since a mistake in the commutation sequence due to poor current direction information results in an open-circuit of the load which is taken care of by the clamp circuit, whereas, if one were using the input voltage polarity information to perform the commutation, a mistake causes a short circuit of the input supply. The second reason is more specific to the use of SiC JFETs as in this case. If during the time that a bidirectional switch should be conducting, both forward and reverse devices are gated (not the case in some two step techniques) the current would flow through the body channel or the reverse device and not the body diode. This diodeless operation improves the overall efficiency of the converter by reducing the conduction losses. Other topologies can also benefit from the reverse channel conduction of a JFET where a diode would normally be used. In [25], diodeless operation of the cells in a multi-level modular converter using SiC JFETS is discussed and in [26], SiC JFETs replace the standard diodes in synchronous rectifiers.

1) Gate Drive Timing Issues: It is critical that the four step commutation sequence is followed without changing the order of the sequence in order to provide a safe commutation. The desired timings when using high speed devices such as SiC JFETs are in the order of 10's of ns and as such, any jitter in the timing waveforms may cause a failure. Whilst the jitter in the timer units of the FPGA can be carefully controlled, uneven turn-on and turn-off delays due to the gate driver circuitry cannot. Figures 8 and 9 show the potential effect of having a faster turn off time and turn on time respectively.

Figure 8 shows that with a larger delay for the turn on, there is the potential to create an open circuit of the load since S_{AaF} and S_{BaF} are never on at the same time. Conversely, Figure 9 shows that with a larger delay for the turn off, there is the potential for creating a short circuit of the input phases since S_{AaR} and S_{BaF} are on at the same time, as are S_{AaF} and S_{BaR}.

The datasheet values for the turn-on and turn off times of the gate-drive circuits used, and more importantly, the potential

	I_L +ve	I_L -ve
$V_A > V_B$	t_2	t_1
$V_A < V_B$	t_1	t_2

TABLE I
TABLE TO SHOW COMMUTATION POINT WITH RESPECT TO INPUT VOLTAGE POLARITY AND OUTPUT CURRENT DIRECTION

difference between two 'identical' parts has to be taken into consideration when setting the commutation sequence times. Nominally, integrated gate drive circuits have a faster turn off than turn on. This is due to the requirement for standard voltage source inverter circuits to create a 'dead time' in order to perform a safe commutation. This means that the situation in Figure 8 generally occurs more often.

III. Output Waveform Distortion

Although switching converters in general offer a high fidelity in demanded output voltage, there can be small errors and non-linearities. In a standard voltage source inverter (VSI) the voltage drop across the devices and the dead time used to prevent a short circuit as the load current commutates between the upper and lower devices, causes an effective voltage drop in the output. That is, the actual voltage-time-area (VTA) applied to the load is not quite the demanded value. Similarly, there are also two phenomenon in a matrix converter that contribute to a deviation in the output voltage with respect to the demanded voltage [27]. There still exists the non-linear voltage drop across the semiconductor devices but unlike the VSI, the commutation times of a matrix converter actually cause a voltage boost in the output voltage. Although the mechanisms similar when comparing Si IGBTs and SiC JFETS, there are however significant differences in disturbances at the output of the converter.

A. Voltage Boost Due to Commutation Timings

The output voltage of the matrix converter will commutate at either point t_1 or t_2 shown in Figure 7. For the purposes of clarity, the time period between t_1 and t_2 will be defined as the overlap time t_O. The precise point at which the load current commutates depends on both the input voltage polarity and the load current direction. Again, using the basic two phase to single phase converter schematic, shown in Figure 6 for reference, Table I shows at which point the output voltage changes with respect to the input voltage and output current.

This implies that the output of the converter will favor the phases that are at a higher voltage when the output current is positive and the lower voltages when the current is negative.

This effect causes a voltage-time-area (VTA) error in the output of the converter at every commutation. The output voltage of the converter tends to favor the higher phase voltages if the output current is positive and the most negative voltages if the current is negative. If the space vector sequence shown in Figure 4 is taken as a reference and the input voltage sector is 1 [17] where the voltage on phase A is the most positive and both VB and VC are both negative. In this situation, if the output current is positive, each on-time for

ωit range	$-\frac{\pi}{6} \rightarrow \frac{\pi}{6}$	$\frac{\pi}{6} \rightarrow \frac{\pi}{2}$	$\frac{\pi}{2} \rightarrow \frac{5\pi}{6}$
Input	$V_A > V_B$	$V_C < V_A$	$V_B > V_A$
Magnitude	$V_A > V_C$	$V_C < V_B$	$V_B > V_C$
$I_L > 0$	$(V_{AB} + V_{AC})$	$(V_{AC} + V_{BC})$	$(V_{BA} + V_{BC})$
$I_L < 0$	$(V_{AB} + V_{AC})$	$(V_{AC} + V_{BC})$	$(V_{BA} + V_{BC})$

ωit range	$\frac{5\pi}{6} \rightarrow \frac{7\pi}{6}$	$\frac{7\pi}{6} \rightarrow \frac{3\pi}{2}$	$\frac{3\pi}{2} \rightarrow \frac{11\pi}{6}$
Input	$V_A < V_B$	$V_C > V_A$	$V_B < V_A$
Magnitude	$V_A < V_C$	$V_C > V_B$	$V_B < V_C$
$I_L > 0$	$(V_{BA} + V_{CA})$	$(V_{CA} + V_{CB})$	$(V_{AB} + V_{CB})$
$I_L < 0$	$(V_{BA} + V_{CA})$	$(V_{CA} + V_{CB})$	$(V_{AB} + V_{CB})$

Voltage Magnitude V_M such that the error voltage = $V_M t_O / T_{seq}$

TABLE II
AVERAGE VOLTAGE ERROR DUE TO COMMUTATION TIME UNCERTAINTY USING THREE ZERO SVM

S_{Ax} will be extended by t_O at both the beginning and end of the pulse. Since there are two points in the sequence where S_{Ax} is active, four times t_O will be added to the VTA of S_{Ax} and similarly, two times t_O will be subtracted from the VTA of both S_{Bx} and S_{Cx} causing a boost in output voltage. Similarly, in the same situation, if the output current is negative, the VTA for both S_{Cx} and S_{Bx} will be extended in the same way. The on time for S_{Bx} and S_{Cx} will be increased by two times t_O and the VTA of S_{Ax} will be reduced by four times t_O. The net effect of the commutation times on output waveforms are summarized in table II [28]

Ideally, the delay between t_1 and t_2 shown in Figure 7 should be set to zero [29] in order to obtain the highest quality output waveform but for the reasons outlined in the previous section, the delay must be set to a value larger than the maximum possible gate driver skew. This would not normally be a major issue for a low frequency IGBT based converter. The commutation time used in the SiC matrix converter is small but since the switching frequency is however significantly high even a small voltage-time area error can cause a significant distortion in the output voltage demand. The calculated error voltages caused by this effect can be seen in figure 10. The calculated results are the same for both conditions where the switching frequency and commutation delay t_O are set to 50kHz and 80ns respectively as used in the SiC converter and 8kHz and 500ns respectively as typical values that would be used in an IGBT based matrix converter. It is important to note that as switching frequencies increase, the commutation times become more significant and should be minimized where possible. This may not be possible if the turn on-turn off jitter specification of the gate drive circuit prevents this.

This phenomenon highlights the importance of the choice of gate drive components for this type of high switching frequency converter. The effect of different delay times on the output waveform quality can be seen in Section V.

B. Semiconductor Device Voltage Drop

The second source of distortion in the output voltage is due to the voltage drop across the semiconductor devices used in

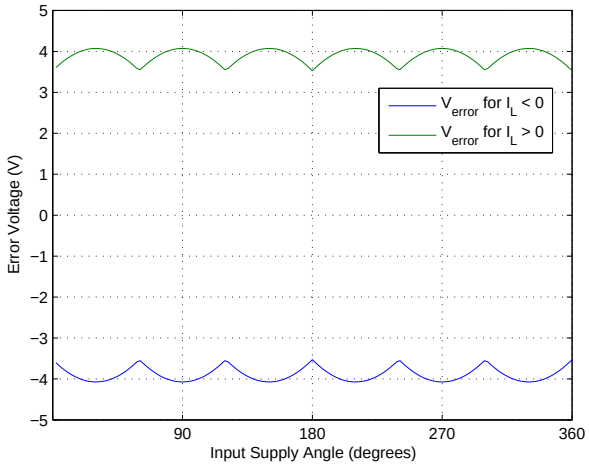

Fig. 10. Output boost voltage caused by commutation delays, Vin=240V(L-N)

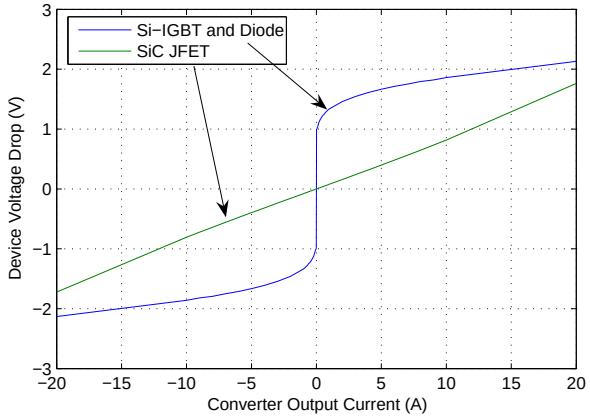

Fig. 11. Voltage drop across the switching matrix for both an all silicon IGBT-diode based converter and the all SiC JFET converter

the converter structure. This is a common problem in all power converters but can be larger in a matrix converter than a typical VSI since many bidirectional switch structures involve the use of series connected IGBT's and diodes. Figure 11 shows a comparison of the voltage drop of both the SiC power devices and a typical Si based IGBT-Diode implementation for devices of the same current rating. It can be seen that the voltage drop for the SiC devices is lower for much of the operating area leading to lower conduction losses but this may not be an advantage in terms of waveform quality.

The problem for the control of the converter if these non-linearities are not compensated for is that there is a very sudden change as the current crosses zero. This causes either an output voltage disturbance for open loop control systems or a disturbance to closed loop current controlled systems. The combined effect of the two distortion effects, voltage drop and VTA boost is that they oppose each other in IGBT based converters. The sudden change in voltage drop at zero crossing compensates in some way to the sudden change in voltage boost effect in an IGBT based converter. In the SiC JFET converter however, there is very little voltage drop as the current crosses zero and as such the disturbance to the control system from the voltage boost effect is increased.

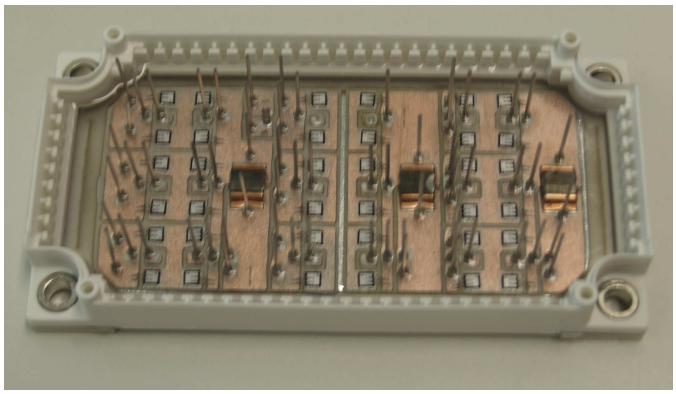

Fig. 12. Photograph of the EconoPack3 power module implementation of the 3 x 3 SiC JFET matrix converter

IV. Converter Design

In order to address all of the implications which followed the use of high speed switching devices such as SiC JFETs, the hardware implementation of the presented power converter had to take into account factors such as the minimization of the stray inductance between the input and output device paths, reducing the size of the input filter passive components and maintaining high thermal performance which necessitated the design of a high performance air-cooled heatsink. This section will illustrate how these key factors have been translated into hardware design features and will lead to the description of the experimental set-up which has been used to investigate the control implementation issues described in the previous section and the results which have been observed.

A. Power Module Implementation

The biggest challenge for Infineon was to build the prototype module as for the prototype several module technologies were combined which were not initially intended to be used in this combination. Using Econo3 as a carrier, enough DCB-space could only be made available by implementing EconoDUAL3 ceramics. The Econo3 frame however does not feature enough positions for connectors to allow the necessary 68 pins (power, gate connections, sensor connections) to be connected. Instead, the pin-rivet system used in low-power Easy-type products was adapted and the whole setup was build manually. A photograph of the internal structure of the finished power module is shown in Figure 12.

Each bi-directional switch was constructed using four lateral-channel SiC JFETS, wired so that there were two in parallel for each current direction. The devices used were rated at 1200V and had an on state resistance of 100mΩ at 25°C. This combination together with the heatsink used created a set of bi-directional switches with a nominal 40A current rating.

Vertical channel JFETS were available as samples at the time the converter was made but these suffered from a higher

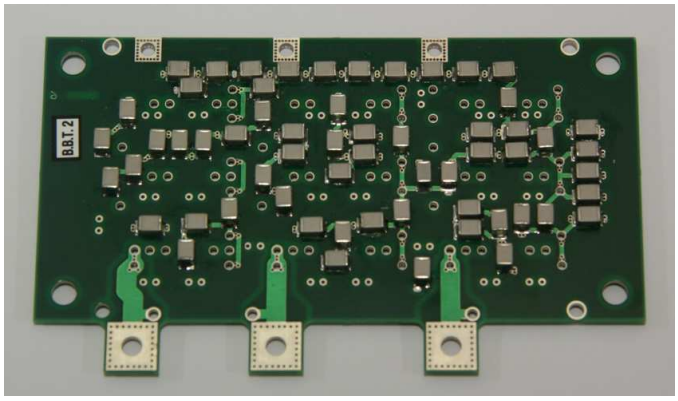

Fig. 13. Photograph of the power plane PCB containing some of the input filter capacitors and connects directly to the power module

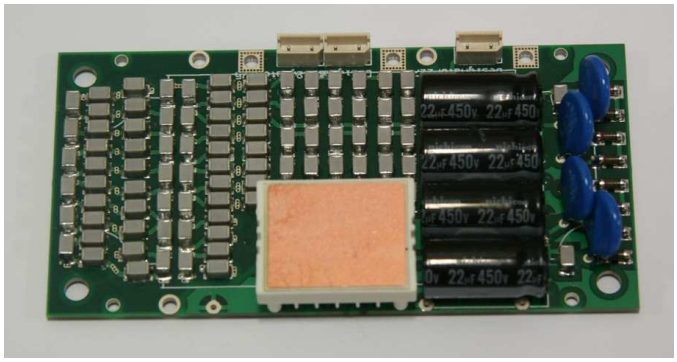

Fig. 14. Photograph of the second power PCB

Device	T-on Delay		T-off Delay		Skew	
	Min	Max	Min	Max	Min	Max
Infineon 2ED020I12FA	145	195	145	190	-35	25
Analog Dev ADuM3220	35	60	36	68	12	12
Agilent HCPL316J	100	500	100	500	-350	350
Agilent HCPL3020	100	700	100	700	-500	500
Agilent HCPL3180	50	200	100	500	-90	90

TABLE III
TABLE OF ISOLATED GATE DRIVE SOLUTIONS AND THEIR RELATIVE DELAY TIMES

on state resistance increase with temperature and their internal structure meant that no internal body diode was present. This lack of the need for an external body diode when using the lateral channel JFET meant that it was possible to include all of the devices needed for the converter into the package chosen. If an equivalent number of diodes also needed to be included, a larger package would have been required. Bipolar gate drive supplies would have also been needed to drive a vertical channel JFET as discussed previously for the SiC MOSFET.

B. Power Plane Implementation

In order to minimize the parasitic inductance between the switching devices and the input filter, a PCB with laminated internal power planes was used to connect the power module to a large proportion of the ceramic capacitors that formed the input capacitance. The normally wasted space in the cavity at the top of the power module was used to house the capacitors. The effect of using many individual capacitors in this way is to create a distributed capacitance across the entire surface of the power module and creates a commutation loop with minimal inductance. Figure 13 shows a photograph of the underside of the power plane where the input filter capacitors can be clearly seen.

The remainder of the input filter capacitors were mounted on a second power board which also included the high speed input-output diode bridge clamp circuit, clamp capacitors and clamp voltage measurement resistors. A photograph of the second power board is shown in Figure 14.

C. Gate drive Design

With SiC-Devices, the gate control loop has to be of minimum stray inductance to allow maximum switching speed. Ideally, the gate drive circuit should be integrated with the power package to allow it to be as close as possible. This would optimize the gate loop inductance but could potentially pose problems with the thermal management if the switching devices are to be used at elevated temperatures. A gate driver electronic section with 18 independent channels however in a MC contributes a significant part to the device's volume, therefore a highly integrated solution would be impossible so achieve. Component selection is therefore very important in order to support a design with minimum volume. Common driver solutions today are designed to drive single switches, half-bridges or full bridges, the latter usually in a bootstrap configuration which is not an option in a MC setup.

As discussed previously, the performance of the converter can depend heavily on the gate driver chosen. In [30] detailed switching analysis and gate drive design for vertical SiC JFETS is discussed . Because of the space available, an integrated - isolated solution was preferred. Typical commercially available opto-coupler based solutions exhibit a worst case propagation delay difference of between 100ns and 500ns. A table showing typical delay times for various commercially available isolated gate drive solutions together with maximum and minimum skew$T_{OFF} - T_{ON}$ (between identical parts is shown in Table III. The effect on the waveform quality when varying the commutation time between 50ns and 350ns can be seen in Section V.

The highest level of integration as of today is a driver with two independent channels that can be configured to operate one bidirectional switch. It was therefore decided to use the Infineon 2ED020I12FA dual gate driver which uses a core-less transformer coupler technique and has a datasheet worst case propagation delay difference of between -35ns and 25ns. All of the devices used were also tested and found to be less than 20ns.

A circuit diagram of the drive circuit for one bi-directional switch is shown in Figure 15. The 2ED020I12FA gate drive IC is used together with an emitter-follower circuit to boost

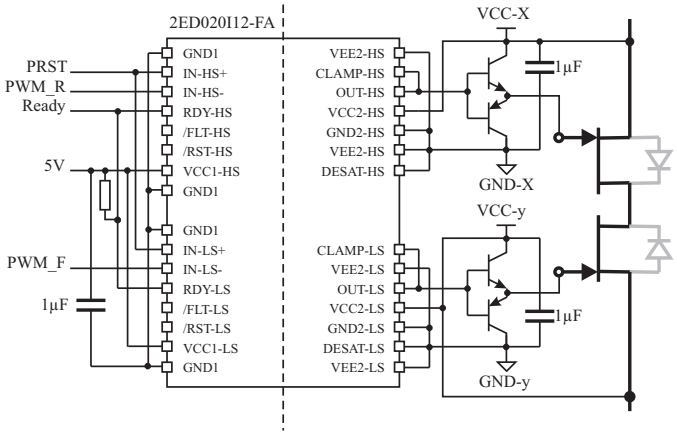

Fig. 15. Schematic diagram of the gate driver circuit used for the matrix converter

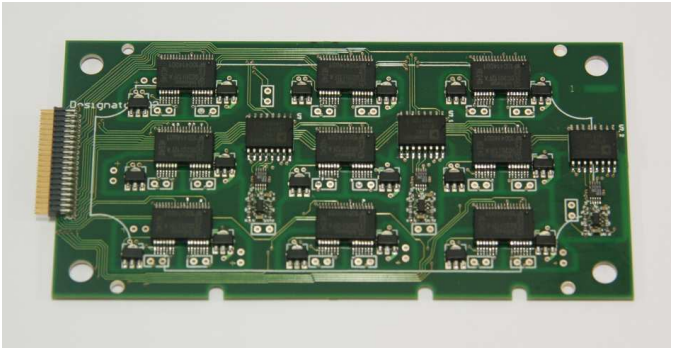

Fig. 16. Six layer gate driver board

the output current capability. No external gate resistor is used in order to drive the JFET as fast as possible. The only resistance in the gate drive current path is the internal gate resistance of the JFET. The transistors used to form the emitter follower stage are the ZXTN2010Z and ZXTP2012Z. The VCE saturation protection functionality of the gate driver IC was not needed and therefore disabled by connecting the 'DESAT' pins to the local ground. This meant that the 'Fault' and 'Reset' lines on the input to the IC were not needed. A 'Ready' Line is provided from the gate drive IC which can be used to ensure that the power supplies on the isolated side of the circuit are functioning, together with the internal communications system within the IC. The PWM_R and PWM_F signals are the demand signals from the FPGA for the reverse and forward conducting devices respectively. the 'PRST' signal is a power-on-reset signal. In the schematic, 'VCC_X' and 'VCC_y' correspond to the +18V local supplies referenced to an input phase (where X = A,B or C) or output phase (where y = a, b, or c) respectively. the 'GND_X' and 'GND_y' nets are the 0V connections for the previously mentioned supplies. This means that the gate of the JFET will be driven with 0V to turn it on and -18V to turn it off. The 'turn off' voltage was chosen with care to ensure that the gate-source avalanche ratings were not exceeded Due to the arrangement of the JFETS (common drain), only 6 isolated power supplies were needed to supply all of secondary sides of the gate drive IC's.

The gate driver board provided a total of nine dual channel integrated gate driver circuits, each JFET used one channel of the 2ED020I12FA isolated gate driver integrated circuit [31]. In order to minimize the distance between the gate driver and JFET connection, the gate driver card shown in Figure 16 was placed as close as possible to the devices and was designed using a six layer PCB occupying an area of 122mm x 62mm, positioned between the two power planes.

This board also includes the signal conditioning circuitry for the three output current measuring shunts integrated in the power module. The correct current direction information is essential to safely implement the current commutation in the matrix converter and integrating the shunts into the power module saved further volume that would have been required if external hall effect current transducers were used.

One of the biggest challenges in the design of the gate driver board was the spacial separation of the internal connections on the power planes of the individual gate driver circuits. The six isolated power supplies were routed and distributed to the individual gate driver circuits using the internal layers of the printed circuit board (PCB). Care had to be taken that a very fast moving 'output' plane did not couple or interfere with any of the other outputs or the input phases. In order to minimize the parasitic capacitance and hence interaction between different power nets, isolated areas were created around each gate drive circuit and, where connection across the board was required, the area where the input and output phase connections were to cross was minimized and the connections always placed at right angles to each other. In this way the parasitic capacitance and the magnetic coupling between outputs with a high dV/dt and inputs with a much lower dV/dt.

D. Experimental Setup

Figure 17 shows the JFETs SiC matrix converter discussed in this paper in its final implementation.

Two of the mentioned key aspects are visible in this picture. On the top of the stack of boards, lays the input filter inductor card and at the base of the stack, the custom made copper heatsink can be seen. The input filter inductors are rated at 25μH per phase, while a line to line total of 1μF of low inductance ceramic capacitance was distributed between two multilayered power planes, mounted directly on top of the power modules. The space between the power pin connections was used to guarantee the shortest path between the devices and the input filter components and in this way, reduce the influence of stray inductance on the switching behavior of the devices.

The gate drive board is placed directly above the power plane and as such it can be placed very close to the switching matrix with less than 1cm gate control loop. Only with an approach like this, the SiC-Switch can be utilized to its full potential. Apart from the afore-mentioned issues with minimization of cross coupling on the gate driver card, the controller was connected to the gate driver card using differ-

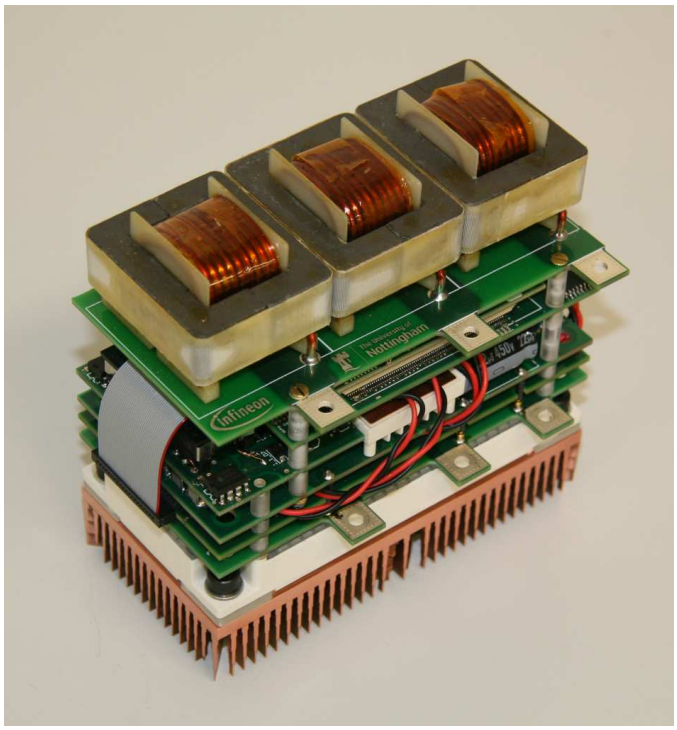

Fig. 17. 20kW SiC JFET Matrix Converter

ential buffers in order to further reduce the effect of the fast switching edges on the control of the converter.

V. Results

In order to determine the effect of varying the commutation time, the converter was run at a low modulation depth, constant output voltage with an output frequency of 30Hz. It can be seen in Figures 18-21 that the output waveform quality deteriorates as the delay is increased, indicating that the output voltage distortion increases with delay. This highlights the need to not only optimize the power circuit layout but also the digital control and gate drive architecture in order to fully utilize the advantages offered by high speed devices. For the purpose of the investigation, the converter has been powered by a three phase sinusoidal supply at 50Hz and the output connected to an RL load.

The results are generated in open-loop and therefore the effect seen in the following results can of course be minimized with the use of a high bandwidth current control strategy. The output demand of the current controller in this case would be a combination of the required motor voltage and the non-linearities of the converter. This high bandwidth control would not help for methods that require a good knowledge of the actual output voltage applied to the load however. Many motor drive applications that requires sensor-less speed and position control, require a high quality estimate of the applied motor terminal voltages to operate and any deviation of the reference from actual applied voltage causes the estimation performance to deteriorate. This emphasizes further the importance of the control and gate drive design in order to minimize these effects.

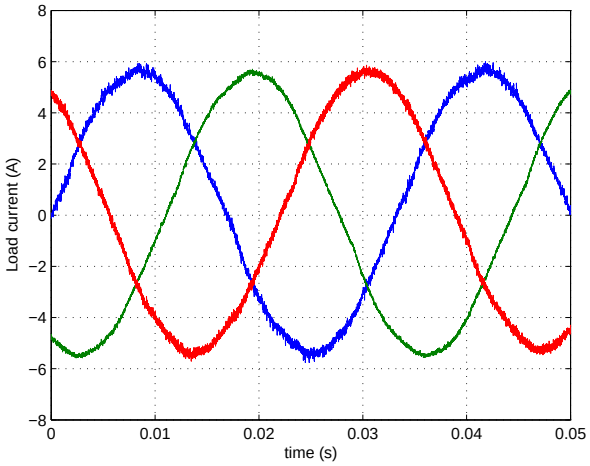

Fig. 18. Converter output waveforms using a 50ns commutation time

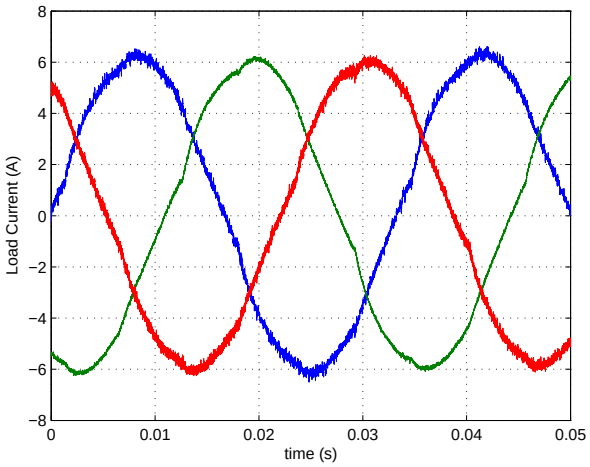

Fig. 19. Converter output waveforms using a 150ns commutation time

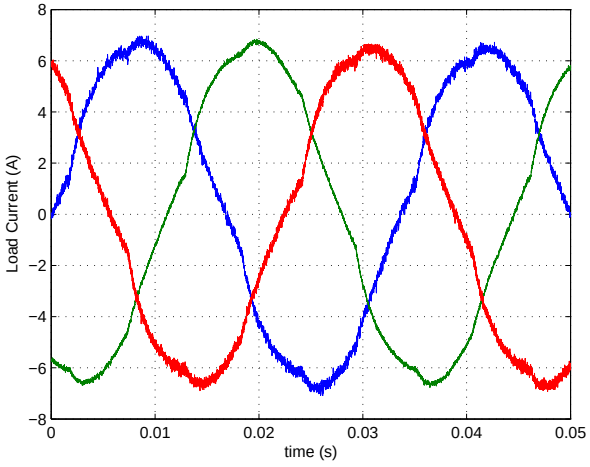

Fig. 20. Converter output waveforms using a 250ns commutation time

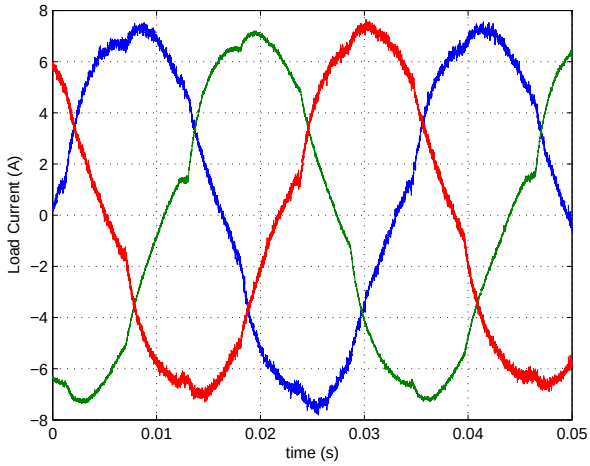

Fig. 21. Converter output waveforms using a 350ns commutation time

VI. Conclusions

The potential advantages that silicon carbide switching devices can offer such as, high speed, high temperature operation and low losses cannot be realized unless the whole circuit is optimized. The high speed of these devices forces the user to minimize the stray inductance of the power circuit using novel layout and bus-bar techniques. The digital control architectures must also be optimized in order to utilize these highly dynamic devices.

This paper has described the design and implementation of a high power density silicon carbide JFET based matrix converter. The importance of power circuit and gate drive circuit layout has been discussed. Initial investigations into the performance and limitations of the digital control structure of such a high switching frequency converter has been addressed. Results highlighting the effect of commutation delays based on gate driver limitations have been presented.

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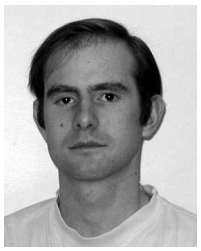

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