On the suitability of 3C- Silicon Carbide as an alternative to 4H- Silicon Carbide for power diodes

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***Abstract* -- Major recent developments in growth expertise related to the cubic polytype of Silicon Carbide, the 3C-SiC, coupled with its remarkable physical properties and the low fabrication cost, suggest that within the next years, 3C-SiC devices can become a commercial reality. Inevitably, a comparison to the most well developed polytype of SiC, the 4H-SiC, should exist. It is therefore important to develop Finite Element Method (FEM) techniques and models for accurate device design, analysis and comparison. It is also needed to perform an exhaustive investigation with scope to identify which family of devices, which voltage class and for which applications this polytype is best suited. In this work, we validate the recently developed Technology Computer Aided Design (TCAD) material models for 3C-SiC and those of 4H-SiC with measurements on power diodes. An excellent agreement between measurements and TCAD simulations was obtained. Thereafter, based on this validation, 3C- and 4H-SiC vertical power diodes are assessed, to create trade-off maps. Depending on the operation requirements imposed by the application, the developed trade-off maps set the boundary of the realm for those two polytypes and allows to predict which applications would benefit once electrically graded 3C-SiC becomes available.**

***Index Terms*-- 3C-SiC, 4H-SiC, FEM, TCAD, simulations, material physical model, PiN, JBS, device characterization.**

NOMENCLATURE OF SYMBOLS USED IN EQUATIONS

$\mu_{LowFields}$	Carrier's mobility in low field conditions.
μ_{min}	Carriers' mobility in highly doped material.
μ_{max}	Carriers' mobility of an unintentionally doped sample.
N	Total doping concentration.
N_{ref}	Doping concentration at which the mobility is halfway between its minimum and maximum value.
α	A measure of how quickly the mobility changes between μ_{min} and μ_{max}.
$\mu_{HighFields}$	Carrier's mobility in high field conditions.
β	Exponent fitting parameter.
v_{sat}	Carriers' saturation velocity.
E_{ava}	Electric field as a driving force for the avalanche.
$\alpha_{n,p}(E_{ava})$	Impact ionization rates of carriers.
$a_{n,p}$ / $b_{n,p}$	Impact ionization coefficients of carriers.
γ	Ionization fitting parameter.
$\delta_{n,p}$	Ionization fitting parameter.
a_e	Approximated impact ionization rates of electrons.
V_{BR}	Breakdown voltage.
N_D	Doping concentration of n-type region.
E_{cr}	Critical electric field.
ε_s	Total permittivity.
w_p	Depletion region in a punch-through design.

I. INTRODUCTION

Wide bandgap (WBG) semiconductors and Silicon Carbide (SiC) in particular, feature advanced electrical characteristics compared to silicon (Si), which means they can induce a step improvement in electrical power conversion [1] [2].

In this paper a comparison is carried out between the hexagonal 4H-SiC and the emerging cubic 3C-SiC technology for their suitability for power diodes. Both SiC polytypes are being researched intensively, however, the 4H-SiC is more prominent, with commercial devices being readily available. Despite its smaller energy bandgap, the cubic SiC polytype features isotropic material characteristics supremely desired for power devices, i.e. isotropic avalanche coefficients. A high electron mobility can also be obtained which is independent to the crystallographic direction [3]. Moreover, the 3C-SiC has the ability to grow directly on large commercially available Si wafers, allowing for the fabrication of WBG devices at lower cost. Nonetheless, the thermal and lattice mismatches between 3C-SiC and Si are the main sources of defects. This has been proved to be a major bottleneck for this technology which, so far, has hindered the commercialisation of 3C-SiC power devices [4]–[6]. Recent advancements though have reported to improve the material quality and in turn that means functional devices might soon be possible [7] [8].

As mentioned earlier, 4H-SiC is already a commercial success for a specific range of voltages and applications. 4H-SiC Junction Barrier Schottky (JBS) diodes have exhibited substantial reduction of power loss in various power conversion systems [9]. The p+ regions within the JBS structure assist in mitigating the negative effects on leakage current, including the reduction of the formed barrier height due to the formation of silicides at the Schottky interface [10] and surface defects [11] [12]. A JBS can be tailored to operate as a unipolar device or as a hybrid (Merged P-i-N Schottky – MPS) by varying the ratio between Schottky and p+ regions. To ensure unipolar behaviour, the p+ implanted to Schottky ratio needs to be small. Bipolar behaviour can be ensured by implanting all active area with p+ to form bipolar P-i-N diodes.

Notable advancements for devices rated less than 2kV include the use of Molybdenum (Mo)-based Schottky metals by Infineon to minimize the on-state power loses of their Generation 5 (G5) and Generation 6 (G6) products [13]. Further, a non-commercial trench SiC JBS rated at 1200V from ROHM demonstrated improved forward characteristics

[14]. In this design the trenches allow for the metal to make contact with the p^+ wells deeper than the surface [15]. 1500V SiC JBS designs have been reported from CREE with 0.5A (low) and 4A (high) on-current while operating in low current densities [16] [17]. An extensive review of wide bandgap devices for automotive industry which includes the introduction of tailored JBS devices of 1.7kV, 10A can be seen in [18].

Significant progress has also been achieved in the area of high voltage. The fabrication of unipolar SiC Schottky diodes rated for 4.9 kV [19] and 6.5 kV [20] [21] have been demonstrated. In addition, test SiC SBD designs capable of blocking up to 15 kV are discussed in [22] for the development of an IGBT/diode module due to their almost negligible reverse recovery charge. Bipolar power diodes are preferred for such high voltage ratings; the boundary between unipolar and bipolar devices is located at 3 kV–6 kV for 4H-SiC technology [23]. Bipolar devices have higher switch on voltage but due to the conductivity modulation they can offer reduced overall voltage drop when very thick and lowly doped epi layers are needed, i.e. for high blocking voltage. In consequence, multiple P-i-N devices have been demonstrated ranging 4.5kV-15kV [19], [24]–[27].

Power diodes from 3C-SiC on cheap Silicon substrates (3C-SiC-on-Si) suffer due to defect-rich grown material. In addition, the challenge in activating implanted acceptors [28] [29], do not currently favor P-i-N diodes for this polytype. As a consequence, all existing 3C-SiC-on-Si devices are currently experimental. Further, due to the aforementioned reasons the physical models of 3C-SiC are underdeveloped. Recent advancements in this field include the development of a comprehensive set of 3C-SiC models [30] [31] and the simulation of power devices [32]–[35]. However, to the best of the authors' knowledge, no reports on the validation of those models with the use of measurements of 3C-SiC power structures exist, a necessary step to ensure the valid use of FEM for the design of 3C-SiC devices.

In this work, for the first time TCAD physical and device models of 3C-SiC are validated with device measurements. A similar validation is performed for the existing 4H-SiC device models. The validated models are then used with scope to compare 3C-SiC diodes to the market preferred, 4H-SiC [36]. To investigate whether there exists a power diode material technology better suited for different applications and to aid the comparison, trade-off maps have been created, for devices with blocking capabilities ranging from 200 V up to 6 kV.

The remaining part of this work is organized as follows. In Section II, the key material parameters of both the 3C-SiC and 4H-SiC for TCAD tools are discussed. In Section III, the methodology for the acquisition of the measurements for commercial 4H-SiC JBS diodes is presented. In Section IV, the physical model of the 3C-SiC is validated by utilizing measurements from a vertical 3C-SiC-on-Si SBD. Moreover, a device level validation of the 4H-SiC physical model is performed utilizing a commercial JBS diode. In Section V, a FEM simulation study has been carried out, which makes use of the validated models, to compare the 3C-SiC and 4H-SiC JBS and P-i-N diodes. Finally, in Section VI the conclusions of this work are presented.

II. 3C- AND 4H-SIC MATERIAL PHYSICAL MODELLING

The authors of this paper developed for the first time a comprehensive set of physical models and their assorted material parameters for the 3C-SiC which is explicitly discussed in [30]. Thereafter, the authors proceed with a thorough validation process, which led to a modified set of coefficient values enabling a wider range of level of accuracy with doping and temperature [31]. The most important physics models to affect the forward and reverse characteristics are discussed below and thereafter used for this work. These therefore, include the models for mobility, at both low and high fields, and for impact ionization. Isothermal room temperature is assumed throughout this work, thus the models' dependency on temperature is neglected. The corresponding coefficient values are also provided and those of 3C-SiC are compared with the 4H-SiC ones.

The carriers' mobility of 3C-SiC mainly depends on the growth process and the doping concentration. The doping dependence of the SiC carriers' mobility values is expressed with the Caughey-Thomas (C-T) (1) model [37]. The corresponding parameter values are shown in Table I. For the 4H-SiC, the given values model the carriers' mobility in the lateral direction at the simulation domain, perpendicular to the main crystallographic (c-) axis. The electrons' mobility in the anisotropic direction, parallel to the c-axis, is 1.2 times greater [38]. The holes' mobility is assumed isotropic [38]. In high electric field conditions, the Canali model (2) [39] utilizes the C-T calculated mobility for low fields and the saturation velocity property of the carriers in SiC as listed in Table I.

$$\mu_{LowFields} = \mu_{min} + (\mu_{max} - \mu_{min}) / \left(1 + \left(N/N_{ref}\right)^{\alpha}\right) \quad (1)$$

$$\mu_{HighFields} = \frac{\mu_{LowFields}}{\left[1 + \left(\frac{\mu_{LowFields} E}{v_{sat}}\right)^{\beta}\right]^{1/\beta}} \quad (2)$$

TABLE I: SIC PARAMETERS FOR LOW AND HIGH FIELD MOBILITY AND COEFFICIENTS USED TO EXPRESS THE DOPING DEPENDENCE.

Parameters Description	**3C-SiC**		**4H-SiC** *[⊥ to c-axis]*	
	Electrons	***Holes***	***Electrons***	***Holes***
μ_{max} *[cm²/Vs]*	*650*	*40*	*950*	*125*
μ_{min} *[cm²/Vs]*	*40*	*15*	*40*	*16*
N_{ref} *[cm⁻³]*	$1.5x10^{17}$	$5.0x10^{19}$	$1.94x10^{17}$	$1.76x10^{19}$
α	*0.8*	*0.3*	*0.61*	*0.34*
β	*0.75*	*0.25*	*1.2*	*1.2*
v_{sat} *[cm/sec]*	$2.5x10^{7}$	$1.63x10^{7}$	$2.2x10^{7}$	$2.2x10^{7}$

For the reverse bias simulations, the impact ionization is modelled for 3C-SiC utilizing the van Overstraeten-de Man formula (3) [40]. In [30], the values of avalanche ionization coefficients were different to those used in this work for 3C-SiC. In [30] the coefficients for electrons were assumed to be the same with those of holes. The reason behind the aforementioned decision was the lack of information regarding

the coefficients of electrons. In this work the parameter set for the electrons used in Table II is adopted. It reflects the values in [41] and yields a critical electric field value at the onset of avalanche breakdown, which is in better agreement with the measurements of 3C-SiC [42] [43]. On the other hand, for the 4H-SiC, the Okuto-Crowell model (4) [44] is used and the coefficients are given in Table III [45]. The biggest contributor to the impact ionization anisotropy, in 4H-SiC, is the anisotropic heating of carriers due to the electron/phonon coupling [46]. Since we model isothermal conditions, the impact ionization is assumed isotropic too.

$$\alpha_{n,p}(E_{ava}) = a_{n,p} \cdot exp\left(-b_{n,p}/E_{ava}\right) \quad (3)$$

$$\alpha_{n,p}(E_{ava}) = a_{n,p} E_{ava}^{\gamma} exp\left[-\left(\frac{b_{n,p}}{E_{ava}}\right)^{\delta_{n,p}}\right] \quad (4)$$

TABLE II: THE 3C-SIC IMPACT IONIZATION COEFFICIENTS.

Parameters Description	Parameter Name	3C-SiC	
		Electrons	***Holes***
Van Overstraeten de Man Ionization coefficients	$a_{n,p}$ *[cm^{-1}]*	*1.28x10^{6}*	*1.07x10^{7}*
	$b_{n,p}$ *[V/cm]*	*5.54x10^{6}*	*1.12x10^{7}*

TABLE III: THE 4H-SIC IMPACT IONIZATION COEFFICIENTS.

Parameters Description	Parameter Name	4H-SiC *[⊥ to c-axis]*	
		Electrons	***Holes***
Okuto-Crowell Ionization coefficients	$a_{n,p}$ *[V^{-1}]*	*1.43x10^{5}*	*3.14x10^{6}*
	$b_{n,p}$ *[V/cm]*	*4.93x10^{6}*	*1.18x10^{7}*
Okuto-Crowell Ionization Parameters	γ	*0*	
	$\delta_{n,p}$	*2.37*	*1.02*

III. MEASUREMENTS METHODOLOGY

For the completeness of this work and to validate the simulation models used, the forward (I_F –V_F) and reverse (I_R-V_R) characteristics of a large number of commercially available 4H-SiC JBS diodes were measured using the Keysight B1505A Power Device Analyzer [47]. The full list of devices measured and characterized is included in Section V Table V. The measurements results are utilized and depicted in sections IV and V. The Devices Under Test (DUT) were measured at a temperature of 298K, while the authors took great care in verifying the accuracy of the measurements. For the forward characteristics the V_F was increased from 0V to 5V with a step of 100mV. For the reverse characteristics the V_R was increased from 0V to 2000V with a step of 10V. Within the test setup a current condition was set to not exceed 1mA.

To avoid self-heating during measurements, pulsed current/voltages were used. The case temperature of the DUT was continually monitored, every 2 seconds, through the heat sink and an attached thermocouple, and a large period of 2 seconds between measurements was selected. However, it was found that the measurements results were sensitive to the pulse width (duration of ON-pulse). It was also found that the pulse width requirement for each device was different. If care was not taken, local heating would still take place, the junction temperature (TJ) would increase momentarily and localized increment of the resistance, due to a reduced carriers' mobility value [30], would occur. This self-heating phenomenon can remain largely untraced, mainly because of its short duration and because of the large resting time in between each pulse (which allows for the temperature to return to the room temperature). However, it affects the measurements results and it needs to be addressed appropriately. To choose and to validate the ON-pulse width, the B1505A oscilloscope view was used. It allows to choose the smallest possible pulse widths and to avoid the measurements overshoots.

IV. SIC DEVICE LEVEL VALIDATION

A. *Validation of the 3C-SiC physical model*

In this section, the validation of the utilized materials in a device level is presented. Fig. 1 depicts the schematic representation of an unterminated vertical 3C-SiC-on-Si SBD fabricated and characterized in [48]. The Schottky metal for the contact is Platinum (Pt) and a punch through design is implemented with a buffer layer. The formed thin Platimum Silicide (PtSi) at the Schottky interface delimits the Schottky barrier height (SBH) as $q\Phi_{PtSi} = 4.98\ eV$ [49], a value lower than the $q\Phi_{Pt}$ for utilizing Pt.

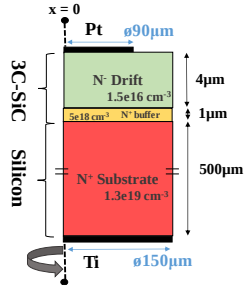


Fig. 1. The TCAD simulated cylindrical asymmetric SBD structure based on an isotype 3C-SiC-on-Si hetero-interface. This structure corresponds to a fabricated SBD characterized in [48].

The 3C-SiC-on-Si SBD structure contains a hetero-junction between the Si substrate and 3C-SiC epitaxial layer. The band offsets formed, mainly the one at the conduction band, restrain the majority carriers transport because of the presence of a small barrier. Nonetheless, the isotype nature of this junction enunciates that the resulted barrier is very small. Consequently, the impact on the I-V characteristics of the power device is negligible.

Furthermore, a high density of defects characterizes the region where the 3C-SiC/Si interface is, due to inherent lattice (20%) mismatch and differences in the thermal expansion coefficients [7], [50] between the two materials. For a representative device model of vertical diodes, the inclusion of these 3C-SiC deep levels is required. That is because these deep levels contribute to the conduction paths which in turn impact the device characteristics.

In [51], the trap profiles affecting the carrier transport mechanisms responsible for the sub-threshold current of the 3C-SiC-on-Si SBD shown in Fig. 1, were characterized. In this work we further improved the characterization achieved to ensure correct matching, both at the sub-threshold but the forward on state region as well. The traps identified are

presented in Table IV and the corresponding effect they induce in the performance of the device is shown in Fig. 2. Considering all above mentioned physical and structural factors enables simulations that can accurately predict electrical performance, both at the sub-threshold (inset of Fig. 2) and the forward on region. Although the SiC devices operate at higher current densities, the current density of 100A/cm^2 is pointed out in Fig. 2 as it is typically used to set the continuous current ratings [52]. Due to the semi-log representation (logI-V) of the forward IV measurements in [48], a level of uncertainty might have been introduced by the data extraction method. To mitigate for such uncertainties, error bars have also been calculated and included in the linear plot.

TABLE IV: MODELLED TRAP PROFILES FOR THE SIMULATED 3C-SIC-ON-SI SBD.

Trap specification	Type	Concentration	Activation Energy
Schottky interface defects	Acceptor	5x10^{12} *cm*$^{-2}$	Band of energies separated by the neutrality level at $E_V + 1.6eV$
	Donor	6x10^{12} *cm*$^{-2}$	
Bulk deep levels due to 3C-SiC/Si	Acceptor	1.5x10^{16} *cm*$^{-3}$	Single level at $E_V + 0.5$eV

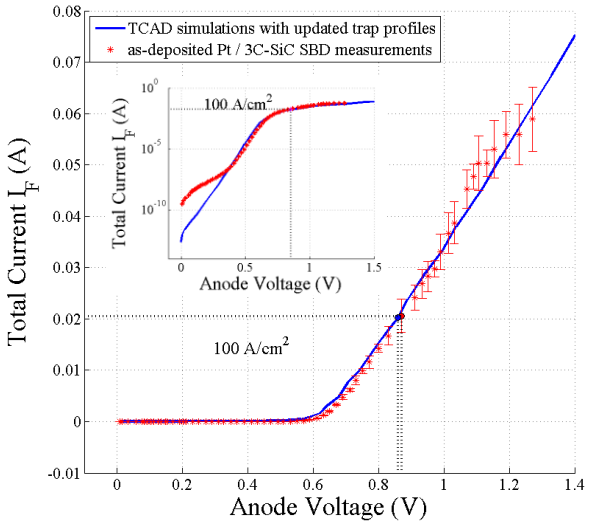


Fig. 2. The incorporation of the updated trap profiles, as presented in Table IV, in the bulk material model developed by the authors in [31], result in accurate simulations of the investigated vertical 3C-SiC-on-Si cylindrical SBD. For the validation of the model, the measurements are acquired from [48]. The inset highlights in detail the sub-threshold region in log-scale.

This fabricated 3C-SiC-on-Si SBD did not feature termination [48]. Therefore, these reverse bias measurements were not useful for the simulation and validation of the physical mechanisms responsible for breakdown.

An alternative validation process was chosen instead. It is based on the material dependent critical electric field value. For unipolar SiC power devices, the primary conductivity carrier type is the one to initiate avalanche. The generated holes have a strong contribution just before the onset of the breakdown [53]. This leads to a condition where both type carriers initiate this physical process in the simulations. According to [54], the analytical model in (3), that describes the impact ionization rates of electrons as a function of the applied electric field in reverse, can be approximated by (5).

$$a_e^{3C-SiC}(E) \approx 2.6 \cdot 10^{-39} E^7 \quad (5)$$

Utilizing (5) and considering the ionization integral for the electrons equal to unity, an expression for the calculation of the device breakdown voltage as a function of the doping concentration (N_D) is derived in (6). This corresponds to a condition where all the 3C-SiC epitaxial layer is depleted (w_p). Further, a similar expression can be derived from (6) and (7) for the critical electric field (E_{cr}^{3C-SiC}) value of the material in (8).

$$V_{BR}^{3C-SiC} \approx 4.16 \cdot 10^{14} N_D^{-3/4} \quad (6)$$

$$E_{cr} = \sqrt{\frac{2qN_D V_{BR}}{\varepsilon_s}} \quad (7)$$

$$E_{cr}^{3C-SiC} \approx 1.24 \cdot 10^4 N_D^{1/8} \quad (8)$$

Following, for the design in Fig. 1, the critical field value calculated is $E_{cr}^{3C-SiC} \approx 1.3MV/cm$. This obtained value is in agreement with the breakdown field measurements of the 3C-SiC for this specific level of doping concentration [42]. Therefore, it is safe to argue that the analytical impact ionization model used for simulations describes well the breakdown mechanism of the material.

$$V_{BR} = E_{cr} w_p - \frac{qN_D w_p^2}{2\varepsilon_s} \quad (9)$$

Finally, the breakdown voltage of the examined 3C-SiC-on-Si SBD with $N_D = 1.5x10^{16} cm^{-3}$ nitrogen (N) doped drift layer, is assessed from (9), $V_{BR}^{3C-SiC} \approx 297V$. This is the maximum breakdown voltage that could be delivered by this punch through 3C-SiC diode structure, assuming a proper termination.

B. Validation of the 4H-SiC physical model for the case of a commercial 1.2kV / 10A JBS from Infineon's G5

To evaluate the physical model of the 4H-SiC, a fifth generation (G5) Infineon JBS has been characterized with measurements and thereafter, modelled and simulated with desired accuracy. The device chosen for measurements is the Infineon IDH10G120C5XKSA1 rated 1.2kV, 10A. The cell structure can be seen in Fig. 3.

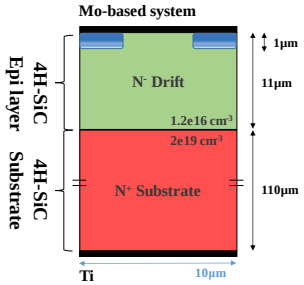


Fig. 3. The JBS cell design in a rectangular geometry considered for simulations.

The cell width is 10 μm, the p+ islands are highly doped with $2x10^{19}cm^{-3}$ aluminium (Al) and the Schottky to implanted area ratio is equal to 50%-50%. This is in good agreement with the layout in [55] and Infineon patents e.g. in [56].

The Mo-based Schottky metal system, used in Infineon's G5 power diodes, attributes a SBH value of 0.9-1.1eV which is desired for JBS rated for medium voltage applications [57]. Therefore, the Mo-based Schottky metal work function is defined $q\Phi_{Mo-system} = 4.53\ eV$ [49], which results in a SBH value for electrons similar to measured ones [58]. The blocking voltage layer is 11μm thick and of $1.2x10^{16}cm^{-3}$ nitrogen (N) doping density [59]. The substrate thickness was defined 110μm which corresponds to Infineon's thinQ!™ design [60]. The active area of the device was calculated to be 0.029 cm^2. The calculation makes use of the Current density – Voltage measurements (J-V) of a similar 1.2kV power diode with 10A rated available in [59], which in turn can be correlated with information from [60] and our own measurements. It also assumes a honeycomb layout design [61].

To accurately reproduce the forward performance, it is necessary to take into account the impact of traps and acceptor deep levels. These traps are typically present in the bulk of 4H-SiC. Lifetime killing defects Z_1/Z_2 and $EH_{6/7}$ have been reported as the dominant type of deep levels in as-grown SiC [62]. These centres are related to carbon vacancies (V_C), and demonstrate an acceptor-like behaviour [63], [64]. Their concentration depends on the growth rate and the C/Si ratio in the gas phase during SiC epitaxy [65]. The Z_1/Z_2 and $EH_{6/7}$ deep-lying electron traps have proven to be very stable against annealing temperatures that reach 1300°C [62]. The concentration of Z_1/Z_2 and $EH_{6/7}$ can be further enhanced by the process of ion implantation, resulting in levels of 10^{14}-$10^{15}cm^{-3}$ magnitude [66]. Methods like thermal oxidation have been applied successfully to eliminate the Z_1/Z_2 centre up to a specific depth from the surface depending on the oxidation duration [67]. In this case, the emitted C interstitials from the SiO_2/SiC interface, during thermal oxidation, diffuse in the bulk material and annihilate the V_C via recombination [68]. In consequence, the traps in the simulation domain are modelled to have a uniform spatial distribution and to cover the deeper half of the drift layer. The density of the bulk acceptor traps was determined $6x10^{15}cm^{-3}$. The top half of the drift layer is assumed to be free from defects, i.e. because of the aforementioned possible treatments.

The result of the adopted advanced modelling approach can be seen in Fig. 4 and Fig. 5. As it can be observed, a very good prediction is achieved for the forward and reverse characteristics. The measurements suggest a blocking voltage for the 4H-SiC JBS of 1410V, whereas the prediction from simulations is 1505V. This observed discrepancy can be attributed in part to the termination of the actual device. The simulation model assumes 100% efficiency for the termination, hence the blocking predicted is nearly ideal. In contrast, the typical SiC termination has efficiency of 80-95%.

To enhance the confidence towards the avalanche models used for the 4H-SiC, and therefore the accuracy of simulations, measurements from [69] and [70] are plotted in Fig. 6 and compared with the carriers' ionization rates predicted from the Okuto-Crowell model (3) used in our TCAD device simulations. It can be seen that the model used and the parameters adopted in Table III are accurate. In particular, those depicting the impact ionization rates of holes are in excellent agreement with the measurements. With the holes dominating the impact ionization process in SiC devices [69], the confidence in the predicting ability of the models is high.

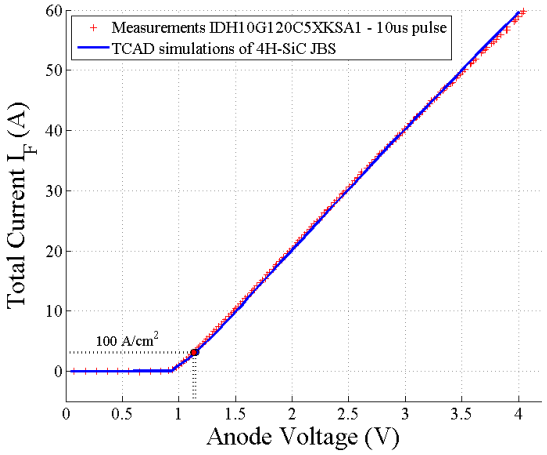


Fig. 4. Forward measurements of a commercial 4H-SiC JBS in comparison with simulation results highlight the potential of the advanced modelling carried out in this work. The forward voltage drop at the typical current density of $100A/cm^2$ is also shown.

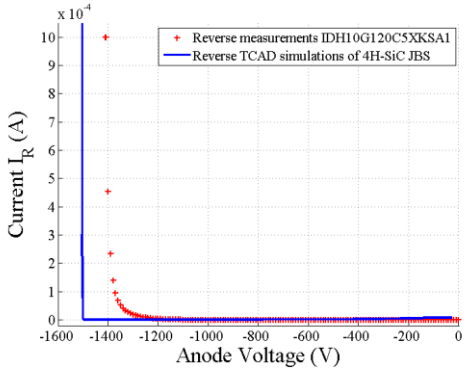


Fig. 5. The simulated reverse characteristics are in line with the measurements of a commercial 4H-SiC JBS, as a result of advanced modelling carried out in this work.

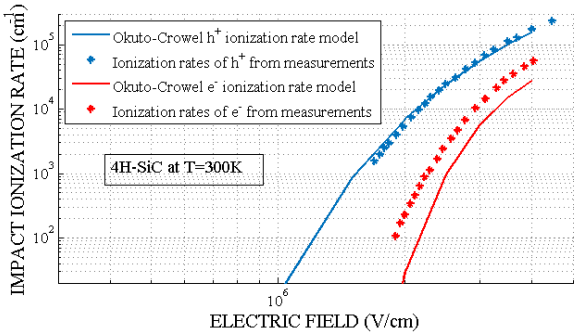


Fig. 6. The dependence of impact ionization rates of both electrons and holes in 4H-SiC on electric field, utilizing the Okuto-Crowell model and the coefficients in Table III. For accurate TCAD simulations, this dependence was evaluated with corresponding measurements for both carrier types [69] [70].

V. 3C-SiC Vs 4H-SiC Power Diodes Comparison

In this section, a study for vertical power diodes between 3C-SiC and 4H-SiC is performed. Results from multiple FEM simulations are compared to obtain performance trade-off maps (on-state voltage drop vs their equivalent blocking capability). These can indicate which voltage class range and therefore which applications might be better served by each material technology. They can also help to identify which applications are to benefit from the ongoing developments on 3C-SiC technology.

A. On the comparison of 3C and 4H-SiC considering JBS diodes

The punch through JBS device structure used for simulations is shown in Fig. 3 for both the 3C- and 4H-SiC. The Schottky:PiN ratio is 50%-50%. Both device technologies are assumed to have the same density of traps in the epi-layers forming the drift. Though this is not the case currently – 3C-SiC as demonstrated in the validation stage earlier has higher density of defects – it is expected to be the case when the material technology matures to the current level of 4H-SiC. The deep acceptor levels considered still cover the deeper half of the drift layer uniformly. In addition, for each simulated device, the ratio between drift doping and defects' concentration is kept unaltered to the one utilized for the validation of the 4H-SiC 1.2kV/10A JBS.

For 3C-SiC JBS the substrate is Silicon, 110μm thick, $2x10^{19}cm^{-3}$ n- doped. For the 4H-SiC JBS the substrate is 4H-SiC, 110μm thick, $2x10^{19}cm^{-3}$ n-doped.

For 3C-SiC JBS, Schottky contact is modelled PtSi. For 4H-SiC JBS, the Schottky contact is modelled to be equivalent of a Mo-based metal system. This is the key differentiation between the otherwise almost common cell structures simulated for the two technologies. The Mo-based Schottky metal system utilized in commercial 4H-SiC power diodes cannot be adopted for the case of 3C-SiC. The large electron affinity value of 3C-SiC, forms a small SBH when in contact with Mo and thus does not form an effective Schottky contact. As a consequence, an ohmic contact behaviour is very likely to be exhibited, which is enhanced by the increased leakage current due to surface defects. The introduction of Al can solve issues sourcing from the formation of the equivalent silicide ($MoSi_2$) [58] [71], but this alone does not change the expected ohmic behaviour of a Mo/3C-SiC junction. Therefore, PtSi is considered for the 3C-SiC-on-Si JBS modelled in this section.

The SiC epitaxial layer thickness considered for the simulated designs, is in the range of 2 - 110 μm. The current state-of-the-art technology does not allow very low concentrations of SiC drift regions. The drift doping concentrations considered for the simulations in this work, range from $9 \times 10^{14}\ cm^{-3}$ up to $5 \times 10^{16}\ cm^{-3}$. This is consistent with the range of values reported in the literature [72].

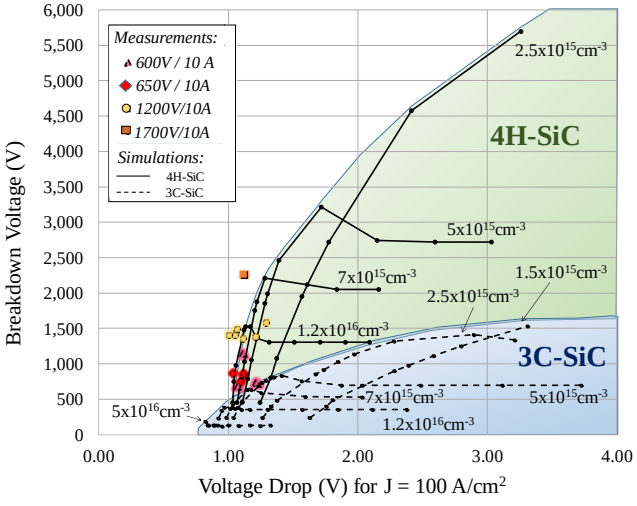
Fig. 7 depicts the breakdown voltage of 3C-SiC and 4H-SiC JBS diodes as a function of voltage drop at $100A/cm^2$ i.e. at typical load conditions. The figure consists of equi-doping lines, which resemble the V_{BR} vs V_{on} at constant doping concentration for various values of drift layer thickness. For thin drift layers and for low doping, the electric field demonstrates a trapezoidal distribution when its critical value is reached, whereas at either very thick layers of high doping, this distribution becomes of triangular shape. Once the critical electric field is reached whilst the shape of electric field is still triangular, any further increase in the drift length does not improve the breakdown capability, but it adds resistance. This explains why the equi-doping lines in the figure stay flat after a certain thickness is reached. The solid lines in Fig. 7 depict the simulation results for 4H-SiC, whilst the dashed lines depict the simulation results for 3C-SiC. Fig. 7 also contains measurement results which enhance the validity of the simulations conducted.

In particular, the forward and reverse characteristics of a selection of commercially available 4H-SiC JBS diodes from leading vendors, shown in Table V, where obtained. The current rating of I_F=10A, is chosen to be the same, which indicates similar active area and therefore enables meaningful comparison. The breakdown voltage for each device is determined at a leakage current of 50μA. The measurements are incorporated into Fig. 7 grouped upon their reverse voltage ratings.

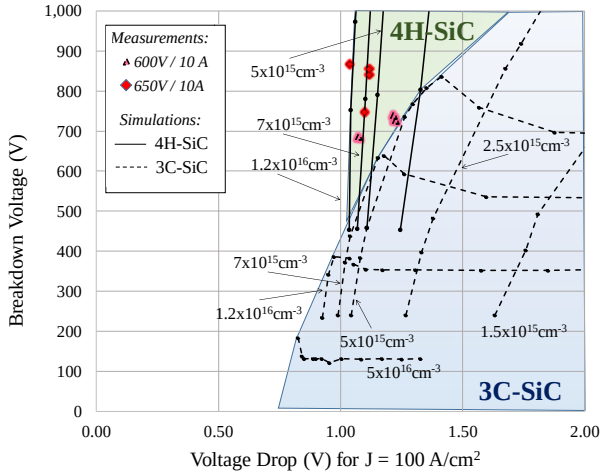
TABLE V: The 4H-SiC commercial power diodes characterized with measurements in this work.

Manufacturer	Product Number	Technology	Rated V_{BR} / I_F
Infineon	IDH10SG60CXKSA1	G3 thinQ!™ SiC	600V / 10A
Infineon	IDD10SG60C	G3 thinQ!™ SiC	600V / 10A
CREE	C3D10060A	Z-Rec SiC	600V / 10A
STMicro-electronics	STPSC1006D	SiC	600V / 10A
Infineon	IDW10G65C5FKSA1	G5 thinQ!™ SiC	650V / 10A
ROHM	SCS310APC9	3rd Gen SiC	650V / 10A
STMicro-electronics	STPSC10065D	SiC	650V / 10A
Toshiba	TRS10E65C,S1AQ(S	SiC	650V / 10A
Infineon	IDH10G120C5XKSA1	G5 coolSiC™	1200V / 10A
Infineon	IDW10G120C5BFKSA1	G5 coolSiC™	1200V / 10A
ROHM	SCS210KE2HR	SiC	1200V / 10A
GeneSiC	GB10SLT12-220	SiC	1200V / 10A
STMicro-electronics	STPSC10H12WL	SiC	1200V / 10A
STMicro-electronics	STPSC10H12D	SiC	1200V / 10A
STMicro-electronics	STPSC10H12DY	SiC	1200V / 10A
CREE	C3D10170H	Z-Rec SiC	1700V / 10A

As shown in Fig. 7, the limits of each SiC technology can be determined by joining the points that correspond to the maximum achieved breakdown voltage for the minimum forward voltage drop. By utilizing these limits, we observe that 3C-SiC JBS can deliver improved performance for breakdown voltage application requirements up to approximately 600V. For higher blocking voltage, 4H-SiC JBS diodes demonstrate lower voltage drop.



(a)



(b)

Fig 7. Areas in which applications can benefit from the utilization of each SiC technology are highlighted. (a) Breakdown voltage of 3C-SiC and 4H-SiC JBS PT power diodes as a function of voltage drop at 100A/cm^2. (b) A magnified interval for the low voltages region. The equi-doping lines resemble a constant doping concentration for various values of thickness. The left most point in each equi-doping line corresponds to lower drift region thickness value whereas the right most point denotes increased thickness.

B. On the comparison of 3C and 4H-SiC considering ideal material for P-i-N diodes

In this section freestanding punch through P-i-N diodes are analysed. The material for both SiC polytypes investigated, is considered ideal, i.e. with low defects density. The design variable of drift region doping concentration ranges from $10^{14}\ cm^{-3}$ up to $5 \times 10^{16}\ cm^{-3}$. The investigated drift region thickness considered ranges from 2μm up to 100μm. The simulations include typical and higher loading conditions, at 100A/cm^2 and 250A/cm^2. Due to the relatively high junction voltage of WBG devices, a P-i-N structure would make sense only at high voltage or high current conditions. Hence, the comparison at 100A/cm^2 primarily serves as a good comparison to the results of the previous sub-section when the JBS was considered.

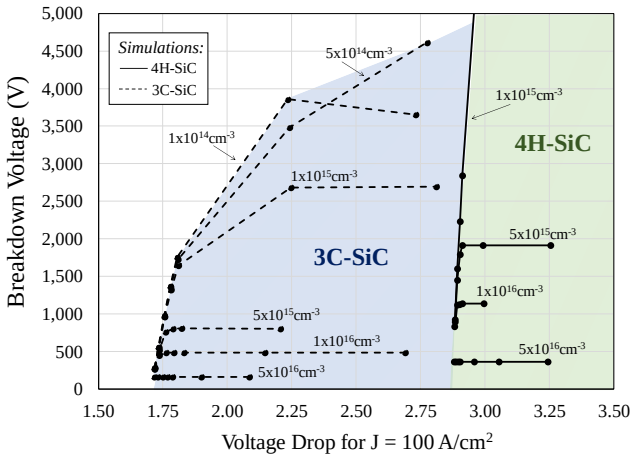


Fig. 8. Breakdown voltage of 3C-SiC and 4H-SiC P-i-N PT power diodes as a function of voltage drop at 100A/cm^2. The equi-doping lines resemble a constant doping concentration for various values of increasing thickness, displayed as filled cycles, beginning from the left most side towards the right most side of each line.

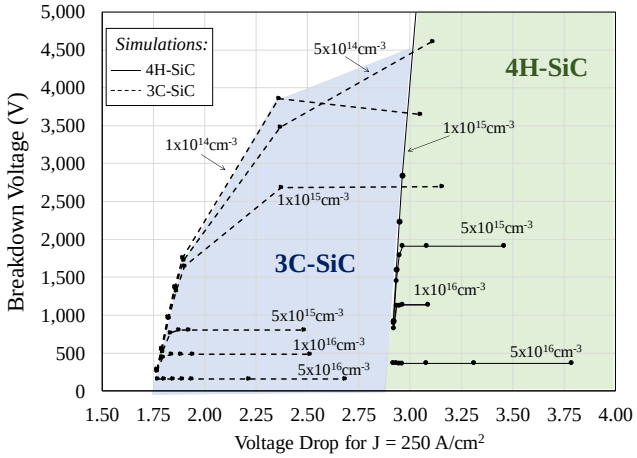


Fig. 9. Breakdown voltage of 3C-SiC and 4H-SiC P-i-N PT power diodes as a function of voltage drop at 250A/cm^2. The equi-doping lines resemble a constant doping concentration for various values of increasing thickness, displayed as filled cycles, beginning from the left most side towards the right most side of each line.

The simulation results for 100A/cm^2 load conditions are shown in Fig. 8. In this case, the 3C-SiC has a clear advantage over 4H-SiC for a wider range of rated voltage values, from 200V-4.5kV. On the other hand, the 4H-SiC P-i-N offers greater blocking capabilities for the same device dimensions in the cost of increased voltage drop during on-state. The same

behaviour is observed for medium application loads in Fig. 9. Assuming that the value of $10^{15}\,cm^{-3}$ is the normally achievable minimum doping concentration for the drift region, devices with blocking capabilities of more than 2.5kV should not be fabricated with 3C-SiC material. Hence, applications requiring more than 2.5kV should be accommodated by utilizing 4H-SiC power diodes.

VI. Conclusions and Discussion

In this work the isotropic polytype of SiC, the 3C-SiC is compared to the market dominant 4H-SiC. An accurate physical representation of the material has been utilized for a TCAD-based simulation study considering ambient temperature conditions. For the first time a device level validation has been carried out for 3C-SiC. This has been achieved by exploiting measurements of a vertical 3C-SiC-on-Si SBD test structure available in the literature. Measurements from off-the-shelf 4H-SiC JBS diodes allowed for the validation of our 4H-SiC device models. The validation procedure revealed that in order to match the measurements, deep levels of acceptor type should be introduced in the drift layer of the simulated structures. It has also been shown that 3C-SiC can feature almost double the defects' density compared to 4H-SiC in the epi-layers of power diodes. This is mainly attributed to the contribution of the hetero-interface of 3C-SiC-on-Si during growth. On the other hand, the growth of 4H-SiC on more expensive SiC substrates allows for a reduced trap density. The deep levels have been recognised from the literature to be Z1/Z2 and $EH_{6/7}$ for the case of 4H-SiC, directly linked to V_C. In contrast, V_{Si} acts as acceptor trap in 3C-SiC, due to the Si atoms leaving the substrate to contribute in the formation of the 3C-SiC.

The validated physical and device models of both SiC polytypes were used to identify the operational regions in which each technology performs better. Assuming similar material quality for 3C-SiC-on-Si and 4H-SiC, and thus the same defect density, TCAD simulations of JBS power diodes were performed with the thickness of the epi-layer and the doping concentration as the design variables. The simulation results were co-plotted with measurements of commercial 4H-SiC JBS diodes. This work indicates that vertical 3C-SiC JBS diodes with blocking capabilities up to 600V could offer improved performance than 4H-SiC for medium load conditions. In particular, for such blocking voltages, the obtained trade-off maps highlight lower on-state voltage drop for the 3C-SiC diodes. The true potential of unipolar 3C-SiC devices is somehow overshadowed by the requirement for an appropriate selection of Schottky metal. A Mo-based metal system is an optimised solution for 4H-SiC Schottky contacts demonstrating low forward voltage drop. On the contrary, due to a larger electron affinity value, Pt is more appropriate for 3C-SiC, due to the formation of high SBH, but it has an inevitable negative impact on the on voltage drop.

Vertical P-i-N diodes were also investigated with simulations to assess the potential for bipolar operation. The performed comparison highlighted that 3C-SiC could win over the 4H-SiC for blocking voltages less than 2.5kV, in both typical (100A/cm^2) and medium load conditions (250A/cm^2). This follows the assumption of a $10^{15}\,cm^{-3}$ achievable minimum doping for the blocking voltage layer.

The results of this work therefore allow to argue that good quality of 3C-SiC-on-Si could have the potential to directly compete with 4H-SiC, not only because of lower cost but because of performance as well. It should be the material of choice for high performance unipolar vertical devices rated up to about 600V and for bipolar devices for the voltage range of 1.2kV to 5kV. Finally, the boundary between unipolar and bipolar power diodes for the 3C-SiC-on-Si could be defined at 1kV – 1.2kV. Applications likely to benefit from this include power electronics for electric vehicles and more electrified power trains, which is the main area of growth for power electronics.

An increased value in using 3C-SiC rather than 4H-SiC for lateral devices (e.g. for power integrated circuits) could also be implied from the analysis of this paper. Due to the anisotropy (1.2 times less electron mobility in the lateral coordinate compared to the vertical one), 4H-SiC has reduced performance when used in lateral diodes. Hence, the 3C-SiC can have a wider range of performance advantage in this latter case.

Summarizing, the results presented in this work suggest that 3C-SiC could be indeed an emerging technology for power diodes. The inclusion of dynamic conditions and the impact of temperature is also required for the complete picture to be obtained regarding these two SiC polytypes.

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