Silicon Carbide n-IGBTs: Structure Optimization for Ruggedness Enhancement

Ioannis Almpanis, Marina Antoniou, Paul Evans, Lee Empringham, Peter Gammon, Florin Undrea, Philip Mawby, and Neophytos Lophitis

***Abstract*—In recent years, silicon carbide (SiC) based devices are increasingly replacing their silicon counterparts in power conversion applications due to their performance superiority. SiC insulated-gate bipolar transistors are particularly interesting as they appear to be the most appropriate for medium and high voltage applications due to their low on-state voltage drop for devices rated at 10kV or higher. However, the widespread adoption of SiC IGBT requires rugged devices capable of surviving in harsh conditions. By using Sentaurus TCAD and validated models based on published experimental results, the short-circuit, unintentional turn-on and dV/dt ruggedness of SiC IGBTs are comprehensively explored and the impact of device parameters on the overall IGBT ruggedness were identified. This paper aims to propose the most efficient methods for IGBT ruggedness enhancement on the device level.**

***Index Terms*—Silicon carbide (SiC), insulated-gate bipolar transistor (IGBT), ruggedness, unintentional turn-on, short circuit, dV/dt, TCAD simulation.**

I. INTRODUCTION

Silicon-based bipolar devices, such as IGBTs and thyristors, are widely used in high-power conversion applications, including HVDC transmission systems and circuit breakers. However, the emergence of silicon carbide (SiC) devices, with their ability to operate at much higher voltages, has made it possible to simplify the converter design, by requiring fewer levels in multilevel topologies [1], to improve the efficiency [2] and to promote the electrification of more applications toward the goal of decarbonization.

The silicon carbide MOSFET is the most studied SiC device structure, and it is currently commercially available from various vendors, with breakdown voltages up to 3.3kV. Additionally, engineering samples rated up to 15kV have been produced proving the suitability of SiC devices in medium and high voltage applications [3]–[6]. However, the on-state resistance of unipolar devices increases dramatically for voltages over 10kV, due to the thick epitaxial drift layer. Therefore, SiC bipolar devices appear to be more appropriate for high-voltage and high-current applications and have attracted significant interest in recent years [7].

Silicon carbide IGBTs combine the ease of voltage control of MOS devices with the low on-state loss of bipolar devices achieved by the conductivity modulation of the drift region. Devices with breakdown voltages up to 27kV have been demonstrated to achieve improved on-state performance [8]–[11]. However, this on-state performance improvement comes at the cost of higher switching losses because of the time required for minority carriers to be injected and removed during the turn-on and turn-off transients. This trade-off relationship has been extensively studied in silicon bipolar devices, and various methods have been proposed for SiC IGBTs to achieve the optimum trade-off for a particular application.

However, efficiency is not the only characteristic that needs to be optimized. The reliability and ruggedness of SiC devices and SiC-based converters also need to be equivalent, or even better, than the currently available silicon-based converters and devices. Despite the increasing attention that SiC devices have attracted, their operation, particularly those achieving blocking voltages above 10kV, comes with certain challenges which have not been fully tackled or understood. In particular, the high dV/dt produced during switching transients can cause EMI issues, voltage spikes, and difficulties in the design of gate drivers [12]. Furthermore, achieving equivalent short-circuit robustness to silicon devices is challenging due to the high current density and smaller heat capacity, which cause fast temperature rise and eventually device destruction [13]. This paper aims to provide a comprehensive view of the ruggedness of SiC IGBTs, including potential failure mechanisms and methods for ruggedness enhancement.

This paper will initially present the conventional IGBT structure and the validation of the models used for TCAD simulations, based on experimental results. It will then describe the most important ruggedness reduction phenomena, their root causes, and methods for improving them for SiC IGBTs rated at voltages higher than 10kV on the device level. The inter-dependencies of these failure phenomena will be discussed in

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Section VIII, and guidelines for ruggedness enhancement will be summarized. Finally, section IX will conclude the paper.

II. IGBT STRUCTURE, MODELLING AND SIMULATION

The structure of the n-type insulated-gate bipolar transistor (IGBT), shown in Fig 1(a), is similar to that of the n-type metal-oxide-semiconductor field-effect transistor (MOSFET), with the addition of a heavily doped p region on the backside, called collector or injector. To reduce the drift region width and accelerate the IGBT's switching speed, an n+ type buffer layer is used. In silicon MOS devices, the p-well is formed by diffusion and can be made deep to ensure good latch-up immunity and blocking characteristics, while at the same time, the surface doping levels can be adjusted to control the threshold voltage. However, in SiC MOS devices the p-well is created by ion implantation of aluminium due to the poor diffusivity of ions, and therefore the p-well cannot be made deep. Even so, with the use of a p-well with a retrograde profile the latch-up immunity and breakdown characteristics are improved, and the threshold voltage and oxide thickness can be controlled independently [14]–[16]. The peak doping concentration of a p-well with the retrograde profile is at a depth of around 0.5 μm and the doping is lower at the surface and bottom of the well (Fig. 1(b)). Additionally, using a higher doping concentration for the JFET region (charge storage layer) increases the electron injection from the emitter and improves the IGBT's on-state performance [17].

In this paper, the technology computer-aided design (TCAD) software Synopsis Sentaurus was used to simulate the device fabrication and operational characteristics of the IGBT cells. This software solves various differential equations, such as continuity, drift-diffusion and Poisson equations, accurately predicting the performance of different IGBT designs, providing insights into the internal regions of the IGBT during operation and identifying weak areas for improvement. It is a powerful tool that provides a fast and economical way of device optimization. However, it is important to note that the complexity and variety of analytical and empirical models used in this software require validation based on experimental results.

Figure 1(a) shows a 2D IGBT cell produced by the Sentaurus process simulator. Typical doping concentrations and thicknesses of the different epitaxial layers are shown in Table I based on data from demonstrated devices. Figure 1(b) shows the p-well doping profile across the C-C' cutline.

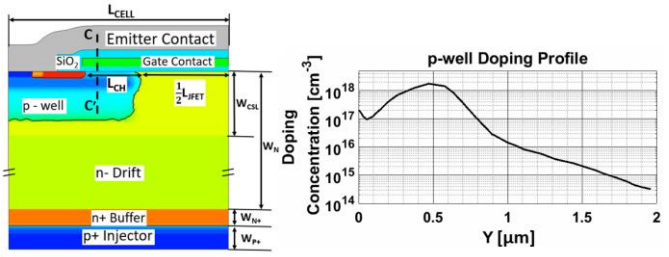

Fig. 1. (a) IGBT cell and (b) p-well doping profile across cutline C-C'.

TABLE I
TYPICAL DOPING CONCENTRATIONS AND THICKNESSES OF DEMONSTRATED DEVICES. (n.a. = not available)

	BV [kV]	W_N [μm]	N_N [cm^{-3}]	W_{N+} [μm]	N_{N+} [cm^{-3}]	W_{CSL} [μm]
[18]	16	150	$4x10^{14}$	1-2	n.a.	2
[19]	15	150	$2x10^{14}$	1	$3x10^{17}$	n.a.
[11]	26.8	230	$2x10^{14}$	n.a.	n.a.	n.a.
[20]	16	170	$3x10^{14}$	1-2	n.a.	2
[9]	22.6	180	$2x10^{14}$	1-2	$1\text{-}5x10^{16}$	n.a.
[10]	27	210	$1x10^{14}$	1-2	n.a.	n.a.
[21]	13	100	$3x10^{14}$	n.a.	n.a.	n.a.

Additionally, the oxide thickness between the gate contact and semiconductor is normally 50-100 nm, and between the gate and source contact is 0.1-1 μm. The above values will be used as inputs for the validation process. The dynamic performance of the devices was simulated using the chopper circuit topology shown in Fig 2(a), while the performance under short-circuit conditions was simulated using the topology shown in Fig 2(b). Parasitic inductances, resistances and capacitances are added in the wiring elements and between the nodes of those circuits to model the nonidealities of the topologies when required.

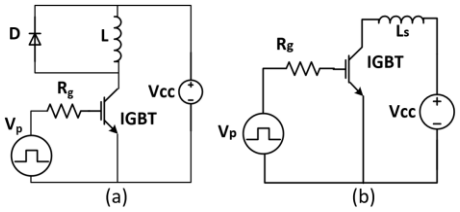

Fig. 2. Circuits used for dynamic simulations: (a) chopper circuit topology for characterization under normal switching conditions and (b) circuit for short-circuit characterization. Details of parasitic inductances and capacitances are not shown.

III. TCAD MODEL VALIDATION

The TCAD device models of this work rely on SiC material physics models derived and validated independently and known to be largely consistent across device structures and fabrication processes. Their accuracy is shown in the appendix at the end of the paper. Through the addition of a small number of experimental results from the scarcity of SiC n-IGBT devices ever fabricated, further fine-tuning of the physics parameters has been achieved so that the final SiC n-IGBT TCAD model can achieve good predictive ability.

The fine-tuning process followed a systematic approach in which the influence of specific parameters and models is known to vary depending on the operational context and the characteristics being analysed. For instance, the channel mobility strongly affects the on-state performance but is less critical for the turn-off switching transient. Therefore, by using simulation results under static and dynamic conditions, various trials can help in understanding the effects of different

parameters under different operating conditions. The best fit between simulation and experimental curves was achieved by using the models presented in Table II and following the iteration process shown in Fig. 3. More details about the models and parameters used can be found in the Sentaurus device user guide [22] and [23].

TABLE II
MODELS AND PARAMETERS USED IN SENTAURUS TCAD SIMULATIONS

Physical phenomenon		Model
Recombination	SRH	
	Doping dependence	$\tau_{dop} = \frac{\tau_{max}}{1 + \left(\frac{N_{A,0} + N_{D,0}}{3 \times 10^{17}}\right)^{\gamma}}$
	Temperature dependence	$\tau = \tau_{300K}\left(\frac{T}{300K}\right)^{\alpha}$
	Constant carrier generation	G = 1x10^{8} cm^{-3}s^{-1}
Mobility	Phonon scattering	$\mu_{const} = \mu_{300K}\left(\frac{T}{300K}\right)^{-\zeta}$
	Doping dependence	$\mu_{dop} = \mu_{min} + \frac{\mu_{const} - \mu_{min}}{1 + \left(\frac{N_{A,0} + N_{D,0}}{N_{REF}}\right)^{\alpha}}$
	High field saturation	**Canali model**
	Reduction at the channel due to the high traverse electric field	**Lombardi model**
	Carrier-carrier scattering	**Conwell–Weisskopf model**
Intrinsic density	Bandgap narrowing	**Slotboom model**
Incomplete Ionisation		
Oxide/SiC interface	Fixed charge	4.1x10^{12} cm^{-2}
	Traps	2.1x10^{13} cm^{-2} eV^{-1}

The TCAD simulation models were validated using experimental data presented in [9], [10], [24]. Figure 4(a) shows that simulation results of the I_c-V_{ge} curve are in good agreement with the results presented in [9] when using the following parameters: effective oxide charge of 4.1x10^{12} cm^{-2}, density of interface traps of 2.1x10^{13} cm^{-2} eV^{-1}, electron and hole maximum mobility of 800 and 70 cm^2/Vs respectively, and surface doping concentration of the p-well of 7.4x10^{17} cm^{-3}. It should be noted that although the simulation and experimental results are almost identical for gate voltages above the threshold voltage, there is a difference for gate voltages in the range of 2-4 V. The same inability of the TCAD simulations to perfectly capture the transfer characteristics in the sub-threshold voltages has also been presented in other studies such as in [24]. Additionally, more fundamental studies, such as [25] and [26], showed that coulomb scattering in the channel region due to the high density of interface states at the SiC bandgap edges is the dominant mobility limitation mechanism for low gate voltages. As a result, more accurate modelling of the interface traps within the SiC bandgap can lead to a perfect match between the transfer characteristics in the whole gate voltage range. However, this difference between the simulation and the experimental data for the gate voltage range 2-4 V is not critical for the simulation results presented in this paper.

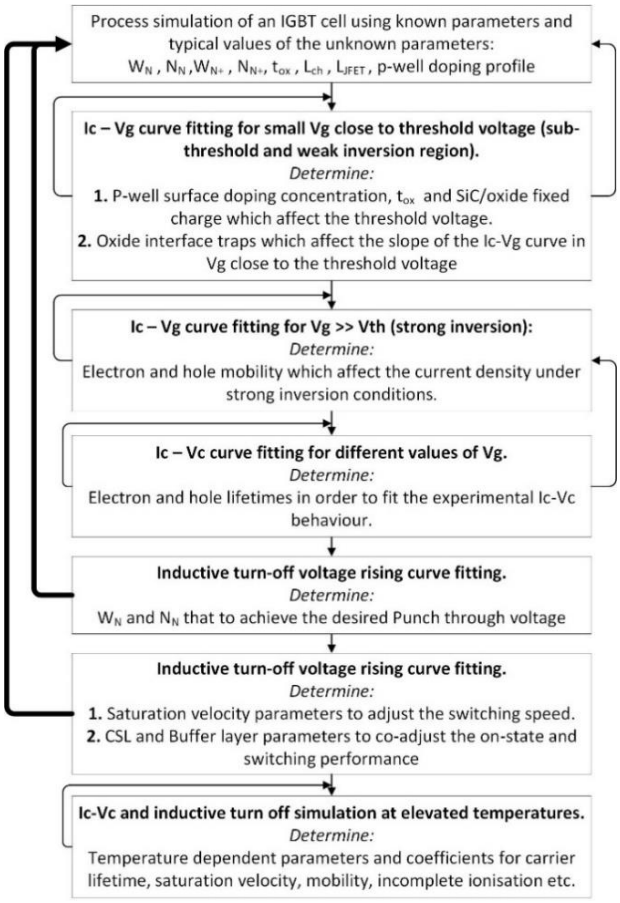

Fig. 3. Flowchart diagram followed for the model validation.

Furthermore, by using the previously mentioned parameters and electron and hole lifetimes of τ_e = 1.8 μs and $\tau_h = \tau_e/5$ = 0.36 μs, the I_c-V_c characteristics of the simulated device were in good agreement with the experimental data in [9] under gate voltages in the range of 5-20V as shown in Fig 4(b). Additionally, the simulated breakdown voltage was 23.7kV, slightly higher than the experimental 22.6kV, as expected because the edge termination of the IGBT was not considered in the simulations.

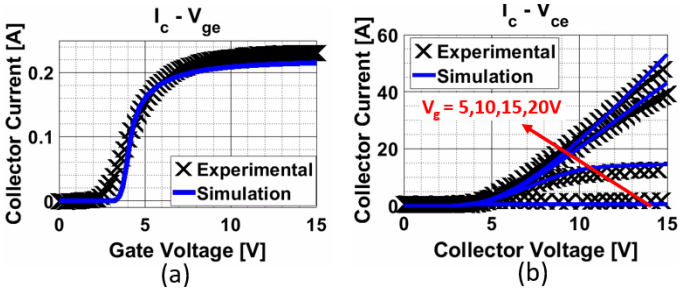

Fig. 4. TCAD model validation results of (a) I_c-V_{ge} and (b) I_c-V_c characteristics using experimental data from [9].

The next step is to validate the dynamic performance of the IGBT, which is more challenging, especially when considering

the device's operation at higher temperatures. The experimental results from [10] were used, and the simulated IGBT had a breakdown voltage of 27kV. A chopper circuit topology was used in [10] for the dynamic performance characterisation, using an air-core inductor of 13.8 mH, to avoid core saturation problems, two series connected 10 kV-rated Schottky diodes as freewheeling devices, and a low impedance gate drive to switch the device as quickly as possible. The chopper circuit topology of Fig. 2 models the experimental conditions, by using a small gate resistance of 10 mΩ and a Schottky diode with a capacitance of 34 pF to fit the current fall observed during the fast collector voltage rising periods of the IGBT. Finally, since there is no voltage overshoot observed in the experimental inductive turn-off waveforms, only a small stray inductance of 4 nH was used in the topology of Fig. 2.

It should be noted that the diode type selection has a negligible impact on the inductive turn-off waveforms and losses of the SiC IGBT but determines the turn-on switching waveforms and losses. As a result, the IGBT and the diode can be independently analysed and optimized to minimise the losses during the turn-off and turn-on transients, respectively. Additionally, in contrast to power MOSFETs where its parasitic PiN diode is usually used as a freewheeling device and should be considered during the device optimisation, an external diode should always be used as a freewheeling device of an IGBT-based converter. For these reasons, only the IGBT turn-off is studied in the following sections because the diode optimisation is beyond the scope of this paper.

By using the validated parameters of the previous 22 kV-rated IGBT as initial parameters, the iteration process finished with the results shown in Fig. 5 for the static and dynamic performance. A 210 μm thick drift region with a doping concentration of 1.3×10^{14} cm^{-3} was used to achieve a similar punch-through voltage (V_{PT}) of about 7 kV. Additionally, the values of electron and hole bulk mobilities for this IGBT were 1020 and 118 cm^2/Vs, respectively. Another critical parameter for the inductive turn-off behaviour of the IGBT is the saturation drift velocity of electrons and holes because the carriers are moving with their saturation velocities under the high electric field in the drift region during the voltage-rising period of the turn-off process. This phenomenon was also taken into account in the TCAD simulations. Finally, the static and dynamic behaviour of this IGBT was simulated at elevated temperatures of 150 °C (static) and 125 °C (dynamic). The on-state voltage drop and turn-off switching losses at a collector current of 20A at elevated temperatures were about 16% and 380% higher than at room temperature, respectively, similar to the presented experimental data [10] (approximately 12% and 310%, respectively). The positive temperature coefficient of the turn-off switching losses is explained by the enhanced plasma injection and increased carrier lifetimes at elevated temperatures which increases the time required of the injected plasma to be removed during the voltage rising and current falling phase of the IGBT turn-off process. Additionally, a detailed explanation of the temperature coefficient of the on-state voltage drop is given in Section VII.

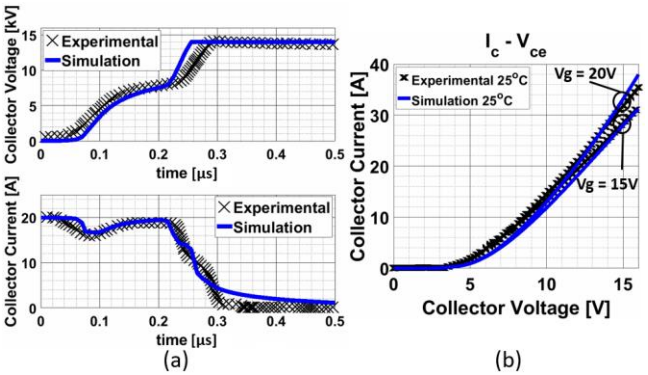

Fig. 5. TCAD model validation results of (a) inductive turn-off switching (b) and Ic-Vc characteristics using experimental data from [10].

IV. Unintentional Turn-On Robustness Improvement by Suppressing the Gate Voltage Spike Produced Due to the High dV/dt

SiC IGBTs have a unique characteristic during their inductive turn-off process in which they exhibit two different voltage rising phases, a slow and a fast, as previously demonstrated in [21], [24], [27], [28]. During the fast voltage rising phase, the voltage can increase as fast as several hundred kV/μs, which can cause long-term reliability issues. Our previous work [29], explained in detail that positive and negative voltage spikes are induced into the gate electrode due to this high dV/dt which can either cause unintentional turn-on of the IGBT or stress the gate oxide. This issue is particularly severe in bridge-leg configurations (Fig. 6(a)), such as DC/DC converters or inverters, where positive and negative gate voltage spikes can be produced in the low-side switch during the switching transient of the high-side switch and vice versa (Fig. 6(b)) leading to short-circuiting of the DC bus.

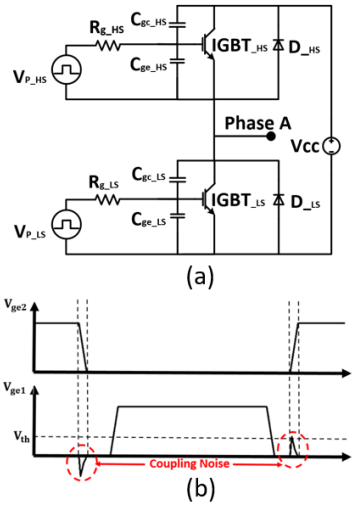

Fig. 6. (a) Bridge-leg configuration and (b) timing diagram showing the coupling noise induced in the gate of the low-side IGBT during the switching transients of the high-side IGBT.

Apart from the traditional ways of improving the unintentional turn-on robustness [7], [30], [31], which is also referred to as crosstalk, false turn-on, self-turn-on, or parasitic

turn-on, the emitter side of the IGBT can be optimised to suppressed it on the device layer. According to the analysis presented in [29], the gate voltage spike amplitude can be linked to the IGBT parasitic capacitances and dV/dt according to Eq. 1, where the capacitances $C_{ge,sp}$ and $C_{gc,sp}$ are the gate-to-emitter and gate-to-collector capacitances respectively, R_g is the gate resistance and $(V_{cc} - V_{PT})/\Delta t$ is the dV/dt during the fast voltage rising phase of the IGBT during the inductive turn-off.

$$V_{spike} = C_{gc,sp} R_g \frac{V_{cc} - V_{PT}}{\Delta t}\left[1 - e^{-\frac{\Delta t}{(C_{gc,sp} + C_{ge,sp})R_g}}\right] \quad (1)$$

Figure 7 shows the unintentional turn-on during the inductive turn-off switching process of the 27kV-rated IGBT by making use of the chopper circuit topology of Fig. 2(a). For the results shown in Fig. 7, a 0 V gate bias is used to turn off the IGBT to clearly present the false turn-on phenomenon. However, a negative gate bias can be used to increase the false turn-on immunity as described in [29]. When the gate voltage increases above the threshold voltage due to the voltage spike (t=2.4µs), the IGBT channel is turned on again, resulting in an increase in electron current and leading to a change in the slope of the collector voltage.

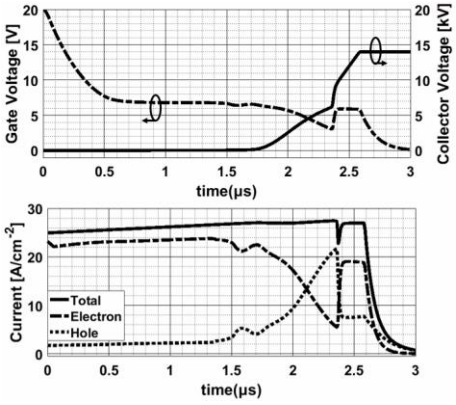

Fig. 7. Gate and Collector voltage (top). Total, Electron and Hole current density (bottom)

It was concluded in [29] that by increasing the gate-to-emitter capacitance, the gate voltage spike can be suppressed without affecting the on-state and switching performance. Figure 8 shows the gate-to-emitter capacitance components of the IGBT structure and Eq. 2 shows that the gate-to-semiconductor oxide thickness (t_{ox}), the intermetal oxide thickness (t_{IE}), the channel length ($L_{channel}$) and the JFET length (L_{JFET}) are the parameters that can be optimized to improve the unintentional turn-on-robustness.

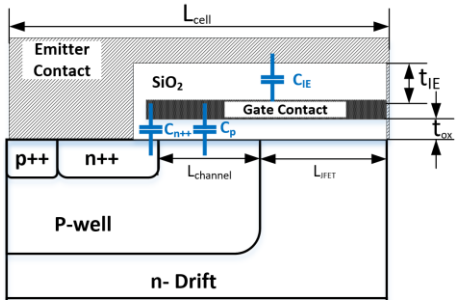

Fig. 8. Capacitance components of C_{ge} in the IGBT structure.

$$C_{ge,sp} = \frac{L_{channel}}{L_{cell}} \cdot \frac{\varepsilon_{SiO_2}}{t_{ox}} + \frac{L_{channel} + L_{JFET}}{L_{cell}} \cdot \frac{\varepsilon_{SiO_2}}{t_{IE}} \quad (2)$$

Figure 9 demonstrates the reduction in gate voltage spike amplitude achieved by increasing the gate-to-emitter capacitance. To do this, the four device variables from Eq. 2 were adjusted sequentially and an almost 80% reduction in the gate voltage spike was achieved. It is worth noting that by reducing the gate-to-semiconductor oxide, the threshold voltage also reduces. However, the retrograde doping profile of the p-well allows for threshold voltage adjustment independently of the oxide thickness by changing the surface doping concentration of the p-well, as previously explained in [14] and [29]. Additionally, the optimisation of these parameters has not had an impact on the switching losses of the IGBT, but they are slightly affecting the on-state voltage drop and turn-off delay time (period until the collector voltage starts increasing) [29].

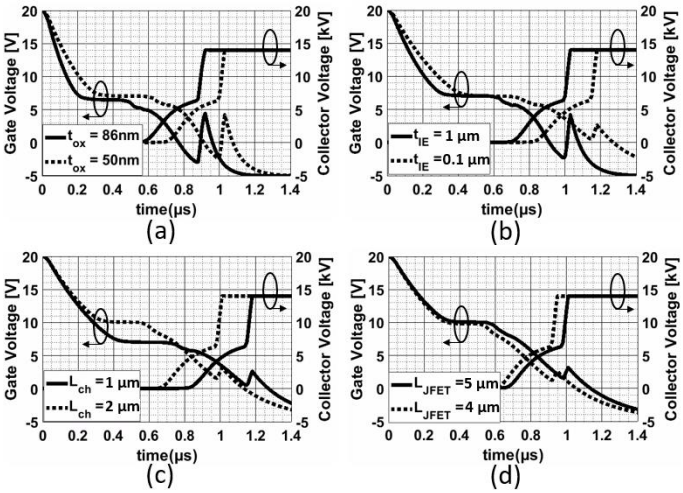

Fig. 9. $V_c(t)$ and $V_{ge}(t)$ during the turn-off of SiC n-IGBTs having (a) different t_{ox}, (b) different t_{IE}, and (c) different $L_{channel}$ and (d) different L_{JFET}.

V. EMI NOISE AND RINGING OSCILLATION REDUCTION, BY REDUCING THE MAXIMUM DV/DT

The previous section demonstrated how the optimization of the emitter side structure of the IGBT can reduce the gate voltage spike generated by high dV/dt and prevent unintentional turn-on and short-circuits. However, high dV/dt also causes EMI noise that can interfere with nearby circuitry, such as microcontrollers, memories, or measurement equipment, indirectly impacting the reliability of SiC IGBTs. It also makes power converter design more complex in various ways as was explained in [32]. Therefore, controlling the dV/dt on the device level will reduce the time and effort required for converter development, improve its ruggedness, and optimize costs.

Our previous work [32] explained that the high dV/dt is caused by the punching through of the electric field into the buffer layer during the voltage-rising phase of the inductive turn-off process. This can be understood by examining the hole density at the beginning and end of the high voltage rising

phase, as shown in Fig. 10(b) and 10(c) with red and black colours, respectively. It can be observed that the space charge region width inside the buffer layer and the number of holes to be removed during this period are small, resulting in a fast voltage transient after the Punch Through.

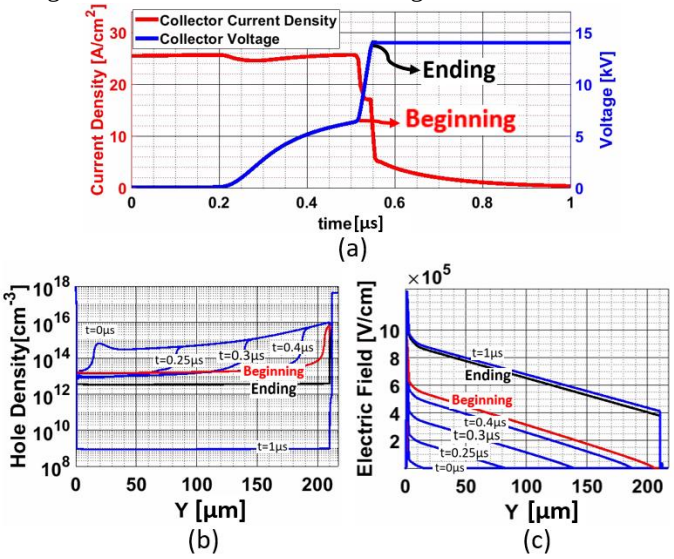

Fig. 10. (a) Typical $I_c(t)$ and $V_c(t)$ curves during inductive turn-off, (b) Hole distribution and (c) Electric field across the IGBT at various instants during the turn-off process.

Although the non-punch-through IGBT structure could solve this issue, it results in dramatically increased switching losses. The novel device structure presented in Fig. 11, addresses this issue, by using a two-step drift region with different doping concentrations. On the collector side, a 10-20µm thick high-doped drift region (HDD) with a doping concentration in the range of 1-5x10^{15} cm^{-3} is used to ensure that the electric field does not punch through to the buffer layer during turn-off and thus controls the maximum dV/dt. Its doping concentration is much lower than that of the buffer layer (typically in the range of 10^{17} cm^{-3}).

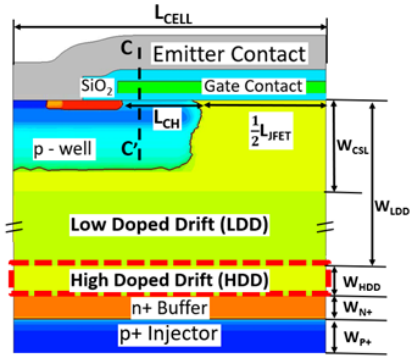

Fig. 11. IGBT structure featuring a novel drift region with a two-step doping profile.

Figure 12 shows that by controlling the doping concentration and width of the high-doped drift region, the slope of the electric field becomes less abrupt and the maximum dV/dt can be effectively adjusted. As a result, the problems caused due to the high dV/dt, such as common mode currents, EMI or voltage spikes, can be addressed by simply adding an extra epitaxial step during the device fabrication.

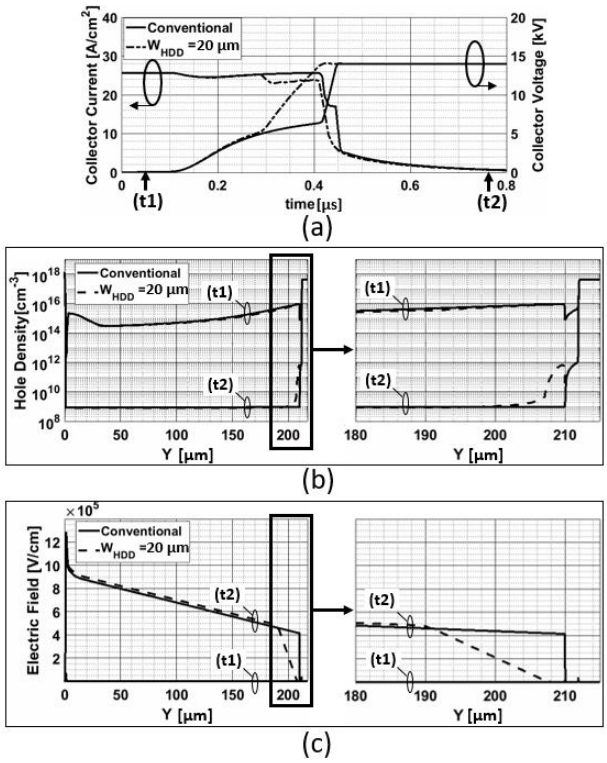

Fig. 12. (a) Comparison of Ic(t) and Vc(t) curves during the turn-off between the conventional IGBT and IGBTs with different High Doped Drift regions (HDD) to reduce the dV/dt during the fast voltage rising phase. Comparison of the (b) hole densities and (c) electric field inside these IGBTs at the beginning and end of the turn-off process.

VI. Short-Circuit Behaviour Optimisation

Failures caused due to high dV/dt or EMI-related issues can lead to an IGBT operating under short-circuit conditions. Short-circuit destruction is a common cause of failure for IGBTs used in motor drives or power conversion applications, with IGBTs accounting for almost 34% of converter design failures [33], [34]. False gate triggering or load short-circuiting can cause permanent destruction of the device due to the simultaneous occurrence of high voltage and high current. This results in high power losses and a temperature rise, which can be especially problematic for SiC devices because of their smaller size and thinner drift layer, leading to a faster temperature rise [35], [36]. However, SiC material has a higher critical temperature than silicon, which means it can withstand higher temperatures before failing [37].

An initial attempt to present the short circuit behaviour of a the conventional structure of a 10 kV-rated IGBT was done in [38] and showed that the device can fail due to parasitic thyristor latching, caused by a positive feedback mechanism that increases temperature and current density, and high leakage current flowing inside the IGBT during the blocking state after the short-circuit has been detected and the device turned off. The latter mechanism can cause the IGBT to fail several

hundred microseconds after it has been turned off, a behaviour that is similar to what has been observed in silicon IGBTs [39] and SiC MOSFETS [40].

Figure 13 shows that the same failure mechanisms exist in the 27 kV validated IGBT during a short circuit event under hard switching at a DC voltage of 14 kV, gate to emitter voltage of 15 V and stray inductance of 100 nH. The end of the simulation is defined as the time at which the parasitic thyristor latches, the current rises uncontrollably and exceeds 3000A/cm^2. In both cases shown in Fig. 13, the parasitic thyristor latching phenomenon happens when the internal IGBT temperature reaches a maximum of about 1750 K on the JFET region. However, the temperature at the boundary between the aluminium emitter contact and the semiconductor exceeds the aluminium melting temperature (933 K) at (t=4 µs) as shown in Fig. 14. Therefore, when aluminium is used as metallisation material, the melting of aluminium contact is the dominant failure mechanism and the short circuit withstand time (SCWT) should be defined according to this. Nevertheless, since other materials with higher melting points (such as silver (1235 K) or gold (1337 K)) can be used for contact metallisation, the simulation results shown in this paper present the whole short circuit behaviour until the parasitic thyristor latch-up.

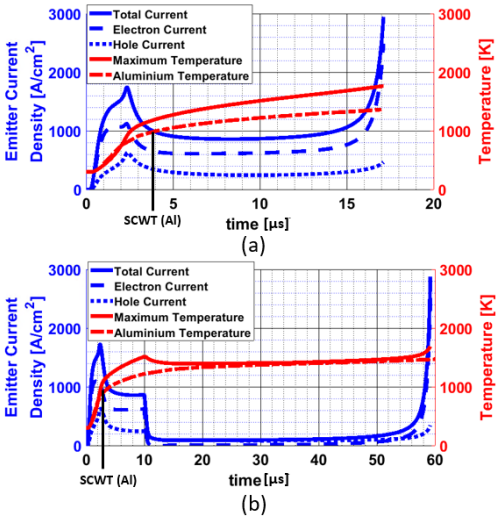

Fig. 13. IGBT short-circuit failure mechanisms. Parasitic thyristor latching (a) during the short circuit phenomenon (b) during the blocking state after IGBT has been turned-off. SCWT (Al) is the short circuit withstand time due to the emitter contact reaching the aluminium melting temperature.

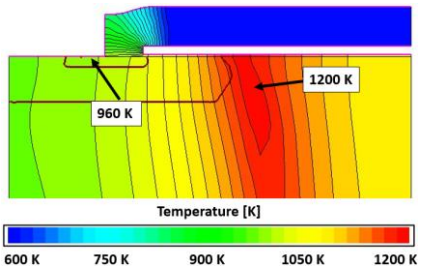

Fig. 14. Temperature distribution within the IGBT structure at t = 4µs (SCWT (Al)) of Fig. 13(a).

Figure 15 shows the impact of the cannel length and the HDD layer on the short circuit behaviour and the SCWT due to the aluminium melting temperature limitation. An increase of the channel length from 2 µm to 3 µm leads to an increase of the SCWT from 4 µs to 6 µs, due to the reduction of the saturation current density and the moving of the hot spot location further away from the aluminium contact. A further increase of the SCWT to 8 µs is achieved with the addition of the HDD layer due to the reduction of the initial current peak. These parameters also increase the time of the parasitic thyristor latch-up which can be exploited by making use of metallisation materials with higher melting temperatures.

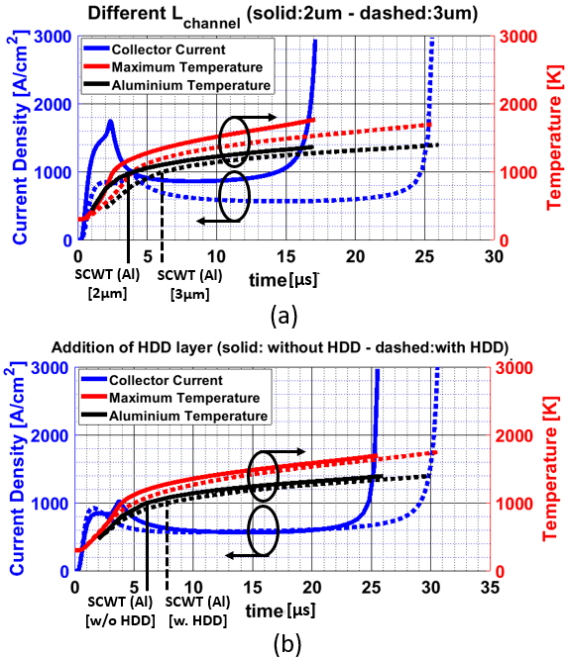

Fig. 15. Short circuit behaviour of the IGBT when (a) varying the channel length and (b) adding the HDD layer. SCWT (Al) is the short circuit withstand time due to the emitter contact reaching the aluminium melting temperature.

Figure 16 shows the impact of other IGBT parameters on the short circuit behaviour. The time for parasitic thyristor latch-up can be increased by controlling the gate-to-semiconductor oxide thickness (Fig. 16(a)), the peak doping concentration of the p-well (Fig. 16(c)) or the buffer width (Fig. 16(f)). Additionally, the intermetal oxide thickness (Fig. 16(b)), the n_{++} region length (Fig. 16(d)) and the JFET region length (Fig. 16(e)) do not significantly affect the parasitic thyristor latch-up time. However, it should be noted that none of the parameters of Fig. 16 have an impact on the SCWT when aluminium is used as metallisation material, because they cannot limit the initial fast temperature rise.

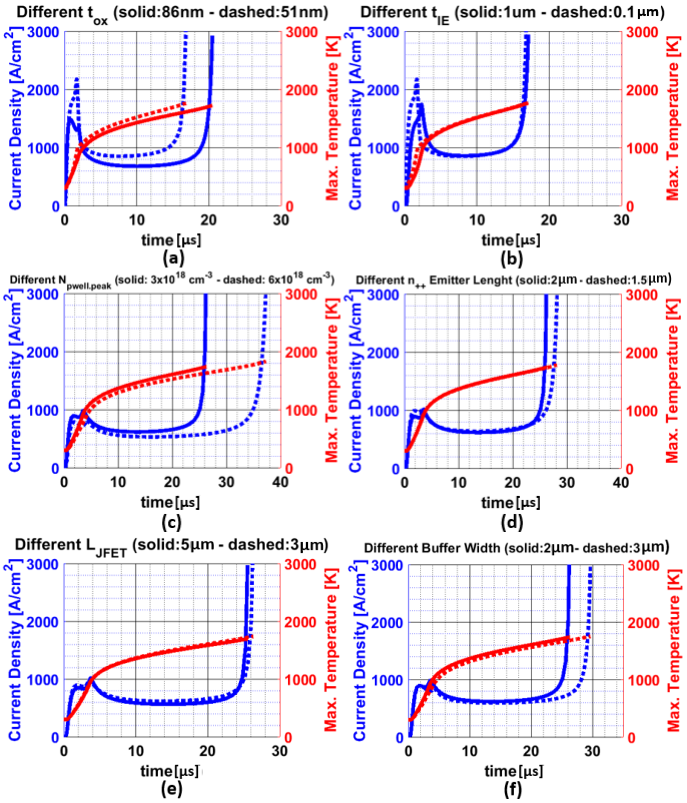

Fig. 16. Short circuit behaviour of the IGBT when varying the (a) gate-to-semiconductor oxide thickness, (b) intermetal oxide thickness, (c) peak doping concentration at the bottom of the p-well, (d) n++ emitter region length, (e) JFET length and (f) buffer layer width.

Finally, Fig. 17 shows the impact of the gate and DC bus voltage on the SCWT. As expected, lower gate and DC bus voltages lead to lower saturation current during the short circuit and eventually higher SCWT.

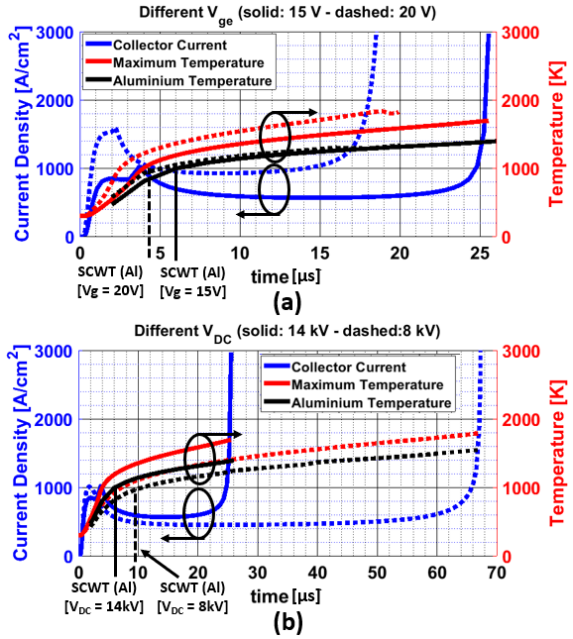

Fig. 17 Short circuit behaviour of the IGBT when varying the (a) DC bus voltage (V_{DC}) and (b) the gate voltage (V_{ge}).

VII. Performance and Ruggedness Prediction of IGBTs Rated at 10-40kV

In order to evaluate the performance of IGBTs rated for a wider voltage spectrum, four drift epitaxial layers were studied with their doping concentrations and thicknesses shown in Table III, in addition to the validated 27kV IGBT. Their breakdown voltages agree with the simulation results and analytical solutions presented in [7].

TABLE III
Doping Concentrations and Widths of Drift Layers for IGBTs Rated at 14-40kV.

BV [kV]	W_N [μm]	N_N [cm^{-3}]
14	100	$3x10^{14}$
20	160	$1.75x10^{14}$
27	210	$1.3x10^{14}$
30	260	$1.5x10^{14}$
40	360	$1.25x10^{14}$

Figure 18 shows the I_c-V_c characteristics of IGBTs rated at 14-40kV at room temperature. The red line in this plot represents the 300W/cm² heat transfer limit of the packaging for the on-state losses which is widely used in power devices. This limit can be increased with the use of novel substrates or packaging methods [43]. However, the 300W/cm² will be used in this study.

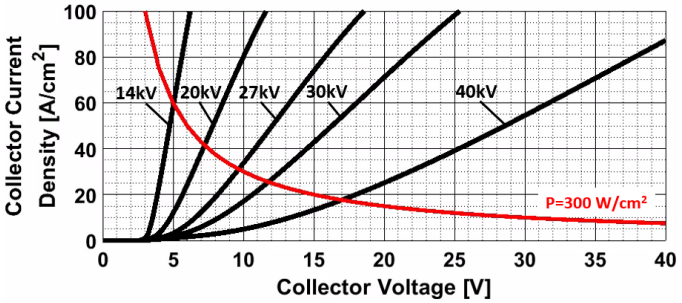

Fig. 18. Ic-Vc characteristics of IGBTs rated at 14-40kV.

It is apparent that as the rated voltage of IGBTs increases by using thicker drift regions with lower doping concentrations to withstand the high electric field, the on-state voltage drop also increases. As a result, the maximum operating current density of the devices is limited due to the heat transfer properties of the packaging and drops from 60A/cm² for 14kV devices to 17A/cm² for 40kV rated devices.

Figure 19 shows the turn-off characteristics of 14-40kV devices at their maximum operational current density for the 300W/cm² limit. The DC bus voltage is 60 per cent of the breakdown voltage for all devices, which is the voltage usually used during normal operation of high-voltage power devices. For all IGBTs, the space charge region reaches the buffer layer before the collector voltage reaches the DC bus voltage, and as a result, a high dV/dt phase exists. Therefore, the analysis presented in [29] can be generalised for all PT-IGBTs rated at

10-40kV. Figure 20 shows the gate voltage spike mitigation achieved for the IGBTs rated at 14kV and 40kV by applying the methods described in section IV to optimise the C_{ge}. Similar voltage spike suppression was observed for all voltage classes. Finally, Figure 21 shows the short circuit behaviour of the 14-40 kV rated IGBTs at 60% of their breakdown voltage through a stray inductance of 100 nH. The lower voltage devices suffer from shorter SCWT due to higher internal PNP transistor current gain, thinner drift region and faster temperature rise.

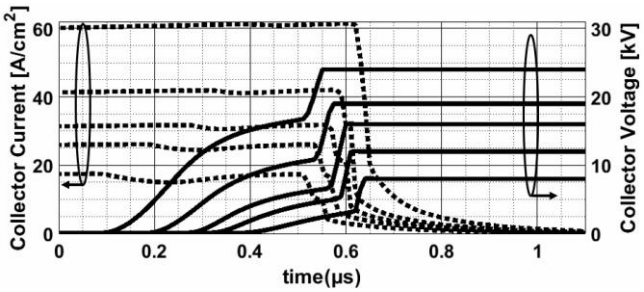

Fig. 19. Collector current and collector voltage during inductive turn-off of IGBTs rated at 14-40kV.

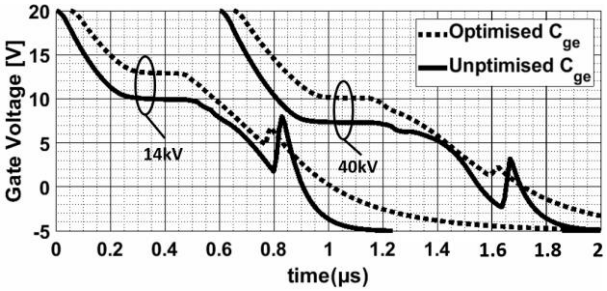

Fig. 20. Gate voltage spike during the fast voltage rising phase of the IGBT turn-off process.

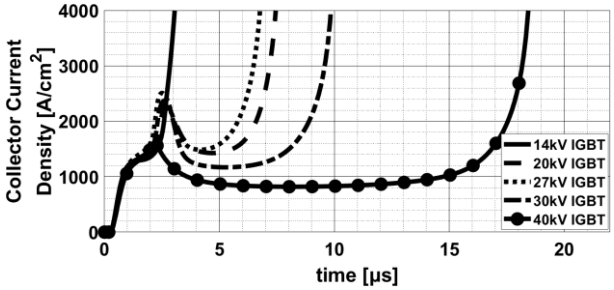

Fig. 21. Short-circuit behaviour of IGBTs rated at 14-40kV.

Figure 22 shows the improvement of the short circuit behaviour achieved with the addition of the HDD layer and optimisation of the remaining parameters as described in Section VI. Only the 14kV and 40kV IGBTs are presented here for clarity, but the results are similar for all voltage classes. For the optimized cases, the emitter side design parameters were adjusted, such as the channel length and the p-well doping profile, to reduce the equivalent p-well base resistance and the saturation current density. It is worth noting that these modifications improve the short circuit behaviour without affecting significantly the on-state and switching losses. Further, improvements can be achieved by modifying the buffer layer or controlling the carrier lifetimes in the drift region to reduce the internal PNP transistor current gain. However, these methods are strongly coupled with the on-state and switching performance of the IGBTs.

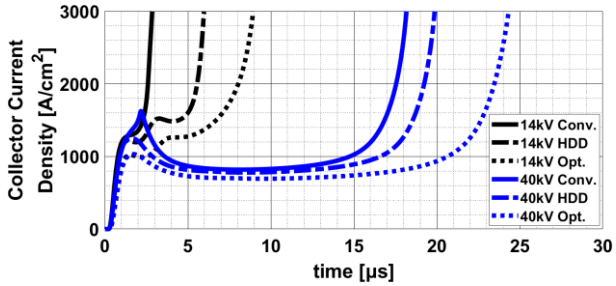

Fig. 22. Short-circuit performance improvement by applying methods described in Section VI.

Moreover, it is important to highlight that in all devices presented above, the same carrier lifetimes were used, τ_e = 5x τ_h = 1.55 µs, which is the outcome of the validation process presented in Section III. However, these carrier lifetimes are not optimum for all voltage classes. Although higher voltage IGBTs might require higher carrier lifetimes in order to modulate the conductivity of their entire drift regions, which are 300-400µm long, for the lower voltage IGBT, a high carrier lifetime can lead to devices with negative temperature coefficient of the on-state voltage drop, as shown in the Ic-Vc characteristics of Fig. 23 for room temperature and at 150 °C. This behaviour has been explained in [44], where test devices were fabricated using 140µm to 240µm thick drift regions. The negative temperature coefficient of the on-state voltage drop can be explained by examining the electron and hole components of the emitter current. On the one hand, the electron current reduces as the temperature increases from RT to 150 °C due to the carrier mobility reduction, similar to what happens in MOSFET devices. On the other hand, the hole current increases at higher temperatures due to the higher plasma injection, owing mainly to the higher ionisation rates of the collector aluminium dopants, and higher carrier lifetimes. As a result, the drift region mobility reduction is the dominant mechanism for thicker drift regions, explaining the positive temperature coefficient of the on-state voltage drop of 27kV-40kV IGBTs, whereas the higher plasma injection and carrier lifetimes are the dominant mechanism for 14kV and 20kV IGBTs.

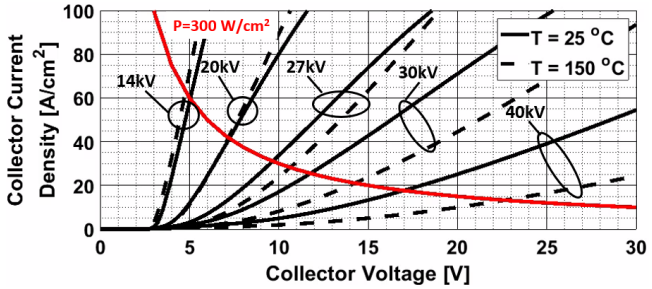

Fig. 23. Ic-Vc characteristics of 14-40kV IGBTs at 25 °C and 150 °C.

Therefore, in order to achieve a positive temperature coefficient of the on-state voltage drop for all devices rated at 10-40 kV, a co-adjustment of carrier lifetimes [23], [45], [46] and carrier injection through the emitter side [17] and the collector side [8], [47], [48] is required. This will improve the ruggedness of IGBT dies and modules because a negative temperature coefficient of the on-state voltage drop can lead to uneven current distribution between parallel dies or even parallel cells within a die.

VIII. Discussion

Sections IV to VII presented some of the most critical ruggedness reduction phenomena and showed some methods of suppressing them. This section aims to discuss the interdependencies between those and summarize the most efficient ways for ruggedness optimization.

Firstly, the addition of the high doped drift (HDD) layer can control effectively the maximum dV/dt for all voltage classes, and thus reduce EMI issues and gate voltage spikes. Additionally, it reduces the peak current density during the short circuit phenomenon and extends the SCWT. It only requires an additional step during the epitaxial growth and does not significantly affect the efficiency of the IGBT. As a result, it is an efficient way to improve the overall IGBT ruggedness.

In regard to the emitter side optimization, the channel length can be adjusted to increase the gate-to-emitter capacitance and reduce the saturation current during the short-circuit and thus suppressing the gate voltage spikes and extending the SCWT. However, it increases the on-state voltage drop due to the higher channel resistance. Especially for the lower voltage SiC IGBTs (rated at 10-20kV), the channel component of the on-state voltage drop is not negligible due to the higher current density during normal operation and the thinner drift regions. For the higher voltage devices though, the drift region component of the on-state voltage drop is the dominant and the operational current density is much lower. Therefore, as the rated voltage of the IGBT increases, the channel length can also be increased to improve its ruggedness without significantly affecting the on-state losses.

Additionally, the oxide thickness and the surface doping concentration of the p-well can adjust independently the gate-to-emitter capacitance and the threshold voltage, improving the unintentional turn-on robustness. This improvement is achieved using thinner oxide between the gate electrode and the semiconductor to reduce the gate voltage spike amplitude and increase the gate voltage margin for unintentional turn-on. However, as the gate driving voltage of the IGBT increases to improve the channel conductivity, the maximum electric field in the oxide increases and therefore the risk for dielectric breakdown is higher. As a result, a minimum oxide thickness of around 50nm should be used to ensure long-term operation.

The reduction of the equivalent p-well resistance can also improve the short circuit behaviour as presented in Fig. 16, by adjusting the peak doping concentration of the p-well and the length of the n_{++} emitter region. The higher peak doping concentration of the p-well does not affect the breakdown characteristics of the IGBT when using a retrograde doping profile with a lower doping concentration at its bottom in order to reduce the field crowding at the p-well corner. Therefore, the optimum values of the peak doping concentration and the n_{++} emitter length can be decided considering the fabrication capabilities for ion implantation.

Moreover, the carrier lifetimes and the doping concentrations and thicknesses of the charge storage layer (CSL), and of the buffer layer can be adjusted to achieve a positive temperature coefficient of the on-state voltage drop for all voltage classes. Apart from the above, they can also increase the SCWT. However, these parameters have a great impact on the on-state and switching losses of the IGBT. As a result, these parameters must mainly be adjusted for specific application requirements, such as for high-frequency or low-frequency applications, in order to achieve optimum efficiency. Fine-tuning of these parameters close to their optimum values can be performed to enhance the ruggedness, but the efficiency sacrifice should always be considered.

IX. Conclusion

The ruggedness of SiC IGBTs rated at voltages between 10kV to 40kV was studied by TCAD simulations using validated models and parameters. The simulation results showed that the cell design can strongly influence the overall ruggedness and that the conventional design compromises the performance significantly. The addition of an extra layer at the drift region, with a doping concentration in the range of 1-5x10^{15}, was found to reduce the maximum dV/dt, suppress the gate voltage spikes and improve the short-circuit ruggedness for all IGBTs independently of the voltage class. Additionally, emitter-side parameters, such as channel length, oxide thickness and p-well doping concentration, were shown to improve the unintentional turn-on robustness and extend the short-circuit withstand time. Finally, carrier lifetimes and the buffer and charge storage layer parameters can further tailor the IGBT ruggedness. Importantly, the large span of simulation results presented in this paper can help decoupling the impact of various device parameters on different phenomena and facilitate the device design and optimization.

Appendix

Figure 24 shows the doping and temperature dependence of the electron and hole mobilities for low electric fields as modelled in TCAD simulations. The experimental data have been taken from [49]–[52], where the authors used simple test structures dedicated to carrier mobility measurements.

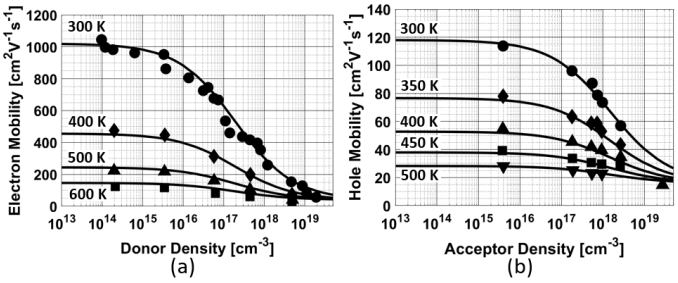

Fig. 24. Low-field electron and hole mobility for different donor and acceptor doping concentrations. Solid lines are the TCAD-modelled mobilities, whereas the discrete experimental points have been taken from [49]–[52].

At low electric fields, the average carrier velocity is proportional to the electric field. However, during the IGBT operation, the carriers are accelerated under high electric fields, and their interaction with optical phonons causes the drift velocity to become saturated [23]. The TCAD models for the drift velocity under high electric fields have been validated based on the experimental results presented in [53] at 296 K (23 °C) and 593 K (320 °C) as shown in Fig. 25.

Additionally, unlike silicon, where most of the dopants can be considered fully ionised at room temperature, the dopants in SiC are relatively deep and incomplete ionisation should be considered. The incomplete ionisation models that are used in Sentaurus TCAD have been calibrated based on the analytical functions presented in [23]. Figure 26 shows with solid lines the ionised aluminium and nitrogen atoms fractions for different doping concentrations and temperatures in the range from 300 K to 600 K. The dashed lines on the same figure show the TCAD-modelled ionized dopant fractions for doping concentrations used for the buffer and collector layer of the SiC IGBT. The simulation results show that 83 per cent of the buffer dopants and only 4 per cent of the collector dopants are activated at room temperature.

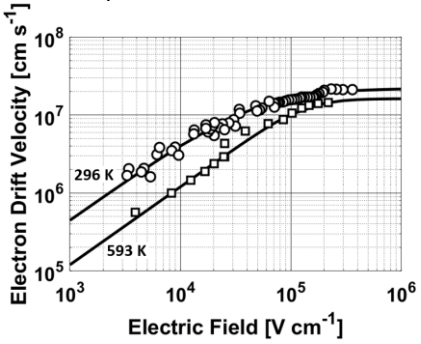

Fig. 25. TCAD modelling and experimental data [53] comparison of drift velocity versus electric field for different temperatures.

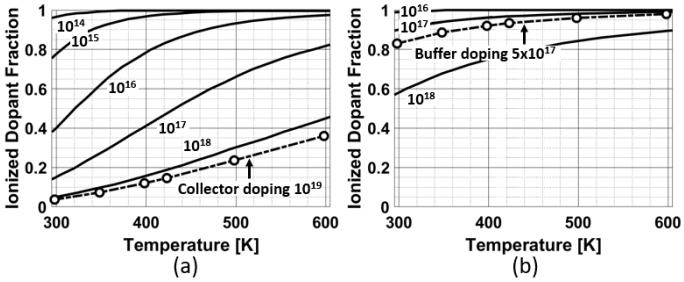

Fig. 26. Ionisation fractions for (a) Aluminium acceptors and (b) Nitrogen donors at different doping concentrations and temperatures. The solid lines are the values calculated by the analytical functions presented in [23] and the dashed lines are the TCAD-modelled results.

Finally, the doping and temperature dependence of minority carrier recombination is also very critical for the IGBT characteristics due to the high levels of injected minority carriers. For the TCAD modelling, the deep-level (or Shockley-Read-Hall) and Auger recombination processes have been considered, since they are the most dominant processes determining the carrier lifetimes for the silicon carbide material [54]. Figure 27 shows the temperature dependence of the minority carrier lifetimes on the drift and the buffer layer for the validated 27kV IGBT TCAD model. These results are in good agreement with what has been already published in the literature [7], [54] and [23].

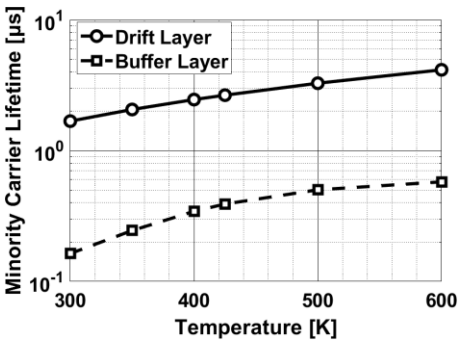

Fig. 27. Temperature dependence of the minority carrier lifetimes on the drift and the buffer layer for the validated 27kV IGBT TCAD model.

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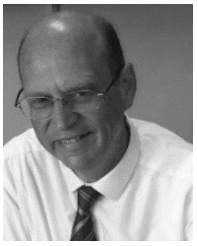

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