A Wideband Single End Fault Location Scheme for Active Untransposed Distribution Systems

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Abstract—This paper presents a single end fault location scheme for distribution networks with distributed generation (DG). The high frequency transients generated when a fault occurs are used to locate the fault point. An equivalent circuit at high frequencies is derived for both inverter based and synchronous DGs. The voltages and currents measured only at the main substation are used in conjunction with the proposed DG model to create the fault location scheme. The distributed parameter line model is employed in the derivation to account for the line characteristics e.g. inductive and capacitive mutual coupling and untransposed lines. The inverter based DG model is validated experimentally on a 400 V, three-phase system. The IEEE 34-bus feeder is simulated and used to evaluate the proposed scheme for different operating conditions e.g. fault resistance and DG conditions. The extensive simulation studies show the accuracy of the proposed scheme with 95.3% of the test cases having an absolute error in estimation of less than 200 m.

Index Terms—Distributed generation, fault location, fault transient, impedance based, single end.

I. INTRODUCTION

THE transmission and distribution system is seeing an increasing penetration of embedded generation especially renewable energy sources (RES) and its resilience will be further challenged by the increasing electrification of transport and heating/air conditioning [1]. RES behave differently to conventional generation systems from both a power system protection and an operation point of view [2]. For instance, RES are often connected to the main grid through power converters to control and maximize the power transfer. Therefore, its operation during abnormal conditions is limited to the thermal capabilities of the converter system which are very different from conventional rotational generation systems [3]. For this reason, embedding RES and its effect on the protection of the electricity system requires further investigation.

Focusing on fault location, the main target of a fault location system is to locate the fault point in order to reduce the repair and restoration time for permanent faults [4]. Fault location techniques for distribution systems can be classified into the following categories: impedance based methods [5]–[11], travelling wave methods [12], [13], computational intelligence methods [14], sparse measurements methods [15]–[17] and integrated methods [18], [19]. The techniques reported in [6]–[12], [15], [16] consider the presence of distributed generation which will feature in future distribution systems.

In [12] travelling wave theory has been used to estimate the fault location based on multiple synchronized measurement units operating at a sampling rate of 1 MHz. The performance of the method may be affected by synchronization errors if synchronization signals such as the global positioning system

(GPS) signals are lost. Also, a high sampling rate will be necessary with short distribution feeders to accurately measure the wave propagation time. Travelling wave based methods are therefore preferred in transmission lines rather than distribution systems [20], where the line lengths are usually longer.

Alternatively, using sparse measurements, the fault can be located by comparing the recoded voltage sag at different points with that calculated by simulating the fault at different nodes of the system in [15], [16]. Sparse measurements methods are applicable to modern distribution systems (not conventional systems) equipped with multiple measurement nodes especially at the DG connection nodes, for instance, in [16], synchronized voltage and current were used. Similar to [12], losing the GPS signal results in synchronization error which is expected to affect the method's performance.

Recent impedance based fault location techniques for distribution systems in the presence of distributed generation have been reported in [6]–[11]. Synchronized measurements at the main substation and DG nodes either for both voltage and current or for current only were used in [6]–[8]. Unsynchronized voltage and current measurements were used in [9] and an iterative load flow algorithm that considers the synchronization angle as unknown has been used to synchronize the measurements. Even though unsynchronized measurements were used in [9], the method still requires a communication network. Methods based on unsynchronized measurements need to be evaluated under conditions when data is lost due to communication failure. In [10], [11], fault location techniques using the measurements at the main substation only were presented. Synchronous based distributed generation (SBDG) has been considered in [11] and modelled as a source behind an impedance at the system nominal frequency. As stated, RES have different characteristics from the SBDGs. The method in [11] will not be valid for a distribution system with RES. Also, it ignored the line capacitance (it uses a short line model). The method in [10] considered the presence of inverter based distributed generation (IBDG) and a steady state DG equivalent circuit at the fundamental frequency was developed. The equivalent circuit is dependent on the DG operating mode during the fault i.e. whether the DG exhibits a current limit mode or tracks the normal pre-fault reference power. A ladder iterative technique was used to estimate the DG current.

Single end impedance based methods are cheap and simple to implement [21]. However, when employed with active distribution systems, a model for the DG is necessary [10]. Considering the increasing use of RES as explained earlier, the representation of IBDG under fault conditions is not a straight forward issue at the system frequency [3]. The IBDG model

at the system frequency depends on the converter operating mode particularly whether or not it exhibits a current limiting mode and also whether or not fault ride through is considered.

In this paper, a wideband single end fault location scheme for active distribution systems is presented. The method has the advantage of using measurements from only one node in the power system. Therefore, the transfer of voltage and current data is not required. The analysis is carried out using the high frequency components generated when a fault occurs. The contributions of this paper are:

1) the use of the distributed parameter line model in the analysis to consider untransposed lines and inductive and capacitive coupling between the phases
2) the presentation of an approximate high frequency equivalent circuit for IBDG which is independent of the DG operating mode
3) the validation of the proposed IBDG model experimentally using a commercial drive system

II. EQUIVALENT CIRCUIT FOR DG

A fault location scheme which uses measurements at one end only requires an equivalent circuit to represent each DG in the system. The derivation of this circuit is presented in this section. Two types of DGs have been considered: inverter based and synchronous generator based distributed generation.

Many types of renewable energy sources such as PV systems produce a DC output that needs to be controlled to maximize the power transfer and to be converted to AC if connected to AC grids. To achieve that, power converters are used. Also, a filter is necessary to prevent the switching frequency harmonics generated by the inverter penetrating into the grid [22]. High order filters such as LCL filters are usually employed instead of simple inductors as they provide better performance with lower inductor values leading to a reduced size and cost [22]. Often, a transformer is needed for interconnection with the grid. This type of generation is known as inverter based distributed generation (IBDG) and a general circuit for the IBDG connected to AC grid at the point of common coupling (PCC) is illustrated in Fig. 1a. The control system and the DC side energy source are not displayed in Fig. 1a. Other DGs can be directly connected to the grid such as synchronous generator based distributed generation (SBDG), see Fig. 1b. In the next subsections, the DG equivalent circuit at the non-fundamental frequencies that will be employed in the fault location process is presented for both IBDG and SBDG types.

A. IBDG approximate equivalent circuit

During healthy operation, the inverter transfers power at the fundamental frequency with some low order and switching harmonics also present. The proposed fault location scheme uses a data window that combines a pre-fault period and a short period during the fault. This window may contain a step variation in the inverter output voltage. Therefore, the frequency spectrum for the output voltage of the inverter over this window would be rich with non-fundamental components not usually seen in the healthy case. As a first stage toward the
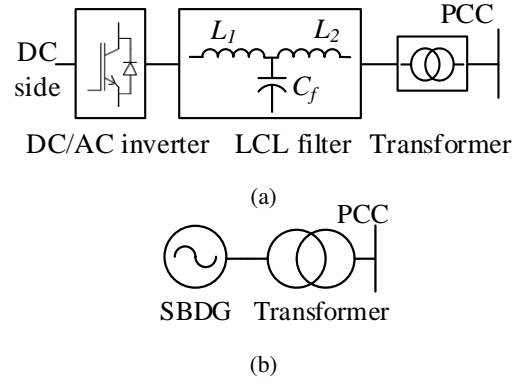

Fig. 1: DG connected to AC grid (a): IBDG (b): SBDG

equivalent circuit, the inverter circuit and the DC side system are approximated to a voltage source (V_{ab}, V_{bc} and V_{ca}) that contains a wideband of frequencies, as shown in Fig. 2a.

The system in Fig. 2a can be reduced to a Thevenin equivalent voltage source V_{th} and impedance Z_{th} connected to the point of common coupling (PCC), see Fig. 2b. Considering the capacitor C_f of the LCL filter is connected in delta, V_{th} can be obtained as (1). For Z_{th}, the inverter voltage source acts as short circuit and Z_{th} is the combination of both filter and transformer impedances when using a transformer, otherwise it will be the filter equivalent impedance.

It is important to emphasize that the IBDG is a non-linear system at the system fundamental frequency and accordingly the Thevenin theorem is not applicable. However, the proposed concept assumes the IBDG system behaves as a linear system at the high frequency components.

$$V_{th\text{-}ij} = V_{ij} Z_C / (Z_C + 3Z_{L1}) \quad (1)$$

where i and j refer to a, b, c, Z_C and Z_{L1} are the impedance of the filter capacitor and inverter side inductor respectively.

In Fig. 2b, the current in different loops can be calculated using mesh analysis. The current in each phase can then be calculated with respect to the loop current. Generally, the current in each phase would satisfy the following:

$$I_{DG} \propto (V_{PCC} - V_{th})/Z_{th} \quad (2)$$

where V_{PCC} is the voltage at PCC.

As the proposed fault location scheme does not use the measurements made at the DGs themselves, V_{th} cannot be calculated. Therefore we must determine under what conditions it is possible to ignore the effect of V_{th} on the equivalent circuit. If V_{th} is ignored, an approximate equivalent circuit as a passive impedance (Z_{th}) will be used for the fault location algorithm. From (1), V_{th} can be calculated as (3).

$$V_{th\text{-}ij} = V_{ij} \times Xf \quad (3)$$

where $Xf = Z_C/(Z_C + 3Z_{L1})$

The magnitude of the factor Xf affects the final magnitude of V_{th} and it is frequency dependent. Substituting for Z_C and Z_{L1} with $1/jwC_f$ and jwL_1 respectively while the resistive elements are ignored and noting w is the angular frequency, Xf can be written as in (4).

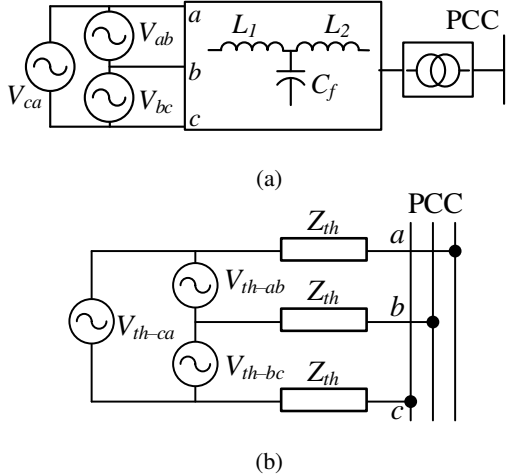$$Xf = 1/(1 - (w/w_r)^2) \quad (4)$$

(a)

(b)

Fig. 2: IBDG equivalent circuit

where $w_r = 1/\sqrt{3L_1 C_f}$

The magnitude of Xf changes with frequency. From (4), increasing the frequency increases Xf until it reaches its maximum at $w = w_r$. Above w_r, increasing the frequency decreases Xf. Therefore, it can be concluded that:

1) Xf has lower magnitudes in the high frequency range and it is better to avoid working at the frequency range surrounding the resonance frequency of filter capacitor and inverter side inductor.

2) In the high frequency range, a filter with a higher $L_1 C_f$ product will have a lower Xf magnitude and accordingly a lower effect from V_{th}.

B. IBDG current and fault location

It is worth noting that, the DG current in the frequency range used by the fault location scheme is also determined by the value of Z_{th} as is clear from (2). Therefore, as Z_{th} increases, the DG current decreases and errors introduced by this current will have a lower impact on the fault location scheme. The magnitude of Z_{th} is minimum at the LCL filter resonance frequency. Below this resonance frequency, Z_{th} has higher magnitudes but also V_{th} cannot be ignored in the fault location algorithm. Therefore, there are two separate factors affecting fault location and which one dominates is not determinable and depend on different conditions. For this reason, even though the approximate circuit is expected to introduce high error compared to the actual circuit in the lower frequency range, the full frequency range will be used for fault location purposes due to the impact of high Z_{th}. A concept to calculate the final estimated distance based on the estimates over the full frequency range will therefore be introduced later in this paper.

C. SBDG equivalent circuit

The SBDG can be simplified to a voltage source (E_{DG}) behind an impedance (Z_{SBDG}) at the system fundamental frequency as shown in Fig. 3a [23]. At non-fundamental frequencies, the voltage source Thevenin equivalent is a short circuit as shown in Fig. 3b. The SBDG exhibits three operating modes during the fault: sub-transient, transient and steady

state [23]. The SBDG impedance Z_{SBDG} increases while transitioning from mode to mode. As the proposed fault location scheme uses data from the first cycle during the fault, the sub-transient impedance is used in modelling the SBDG at non-fundamental frequencies.

Note that the detailed synchronous machine harmonic model is different from a model which uses only the sub-transient impedance of the machine [24]. In [25], a detailed harmonic model was developed and simplified to the simple harmonic model reported in [26]. The approximate simple harmonic model uses the sub-transient impedance to model the machine for the harmonic studies and is employed in this paper to simplify the fault location processing.

(a) fundamental frequency   (b) non-fundamental frequencies

Fig. 3: SBDG equivalent circuit per phase

III. PROPOSED FAULT LOCATION SCHEME

When a fault occurs in a power system, the fault causes a sudden change in the system voltage at the fault point. The fault point can be treated as a voltage source with a step change which is equal and opposite to the pre-fault voltage. This source injects non-fundamental frequency components into the system that are captured and processed to locate the fault. From the previous section, it has been shown that the DG will be represented as a passive impedance at the higher frequencies. Therefore, for a fault with a resistance R_f, the system equivalent circuit at the fundamental frequency and non-fundamental frequencies will be as shown in Fig. 4.

To generalise the analysis for different line conditions, e.g. short/long lines, transposed/untransposed lines, the analysis uses the three-phase distributed parameter line model. A coupled three-phase untransposed system can be decoupled to three independent modes (ground mode and two aerial modes) using the modal transformation [4]. Assuming z_{abc} and y_{abc} are the per unit length three-phase series impedance and shunt admittance of the line respectively in phase domain, transformation between phase domain and modal domain can be carried out as follows [4]:

$$V_{012} = T_v^{-1} V_{abc} \qquad I_{012} = T_i^{-1} I_{abc}$$
$$z_{012} = T_v^{-1} z_{abc} T_i \qquad y_{012} = T_i^{-1} y_{abc} T_v \qquad (5)$$

where $0, 1, 2$ are the ground and the two aerial modes, a, b, c are the phase components, T_v and T_i are the eigenvectors of $z_{abc} y_{abc}$ and $y_{abc} z_{abc}$ respectively.

Also, the propagation constant γ and the characteristic impedance z_c of the line are given by (6).

$$\gamma_{012}^2 = z_{012} y_{012} \ , \qquad z_{c_{012}} = \gamma^{-1} z_{012} \qquad (6)$$

Consider a fault between nodes k and k+1 in the system as shown in Fig. 4, the first step is to reduce the whole system to a single section system as shown in Fig. 5. The system reduction can be done by sweeping the measured voltage and current at

the main substation downstream to node k and calculating the Thevenin equivalent impedance for the system beyond node k+1 (Z_{eq}). This process requires the knowledge of the load data, line data and the DG equivalent impedances which have been discussed in section II.

(a) fundamental frequency
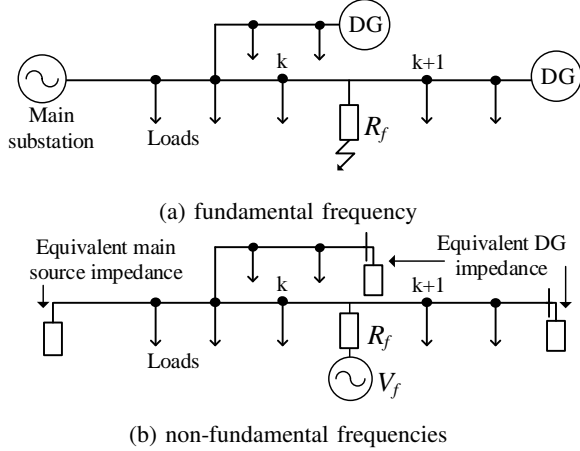
(b) non-fundamental frequencies

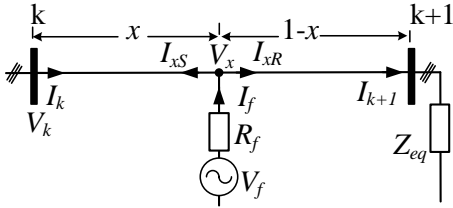Fig. 4: General distribution system with a fault

Fig. 5: Reduced system at non-fundamental frequencies

The virtual step voltage source at the fault point (V_f) is created based on the pre-fault voltage at the fault point ($V_{x_{pre}}$) that can be calculated by (7) in different modes $(0, 1, 2)$ then converted to the phase domain by (5) [27].

$$V_{x_{pre}} = \cosh(\gamma x)V_{k_{pre}} - z_c\sinh(\gamma x)I_{k_{pre}} \tag{7}$$

where $V_{k_{pre}}$ and $I_{k_{pre}}$ are the pre-fault voltage and current calculated at node k from downstream sweeping of the pre-fault measurements at the main substation [4].

The fault current (I_f) can be calculated in the different modes $(0, 1, 2)$ based on the swept voltage and current (V_k and I_k) using (8) to (11) and then converted to the phase domain by (5).

$$\begin{bmatrix} V_x \\ -I_{xS} \end{bmatrix} = \begin{bmatrix} \cosh(\gamma x) & -z_c\sinh(\gamma x) \\ -\sinh(\gamma x)/z_c & \cosh(\gamma x) \end{bmatrix} \begin{bmatrix} V_k \\ I_k \end{bmatrix} \tag{8}$$

$$V_x = \{\cosh(\gamma(1-x))Z_{eq} + z_c\sinh(\gamma(1-x))\}I_{k+1} \tag{9}$$

$$I_{xR} = \{\sinh(\gamma(1-x))Z_{eq}/z_c + \cosh(\gamma(1-x))\}I_{k+1} \tag{10}$$

$$I_f = I_{xS} + I_{xR} \tag{11}$$

The calculation steps from (7) to (11) require a value for the fault distance x which is unknown. Therefore, in the first iteration an initial value of 0.01 pu is used. After creating the fault voltage source (V_f) in the time domain as a step voltage which is equal and opposite to $V_{x_{pre}}$ (7) [27], its frequency

spectrum can be calculated and used in conjunction with the fault current (I_f) to estimate the fault distance x by applying Kirchhoff's voltage law (KVL) on the fault branch based on the fault type.

To estimate the fault distance x, the Taylor expansion for both $\cosh(\gamma x)$ and $\sinh(\gamma x)$ has been used in (8) by considering the first two terms of the series to represent the voltage at the fault point and V_x can be rewritten as (12).

$$V_{x_j} = A_j + B_j x + C_j x^2 + D_j x^3 \tag{12}$$

where j refers to the propagation modes $(0, 1, 2)$ and the values for A_j, B_j, C_j and D_j are given as:

$$A_j = V_{k_j} \qquad B_j = -\gamma_j z_{c_j} I_{k_j}$$
$$C_j = \gamma_j^2 V_{k_j}/2 \qquad D_j = -\gamma_j^3 z_{c_j} I_{k_j}/6$$

The voltage V_x can be expressed in the abc domain by (13) using (5)

$$V_{x_{abc}} = A_{abc} + B_{abc}x + C_{abc}x^2 + D_{abc}x^3$$
$$= [V_{xa};\ V_{xb}; V_{xc}] \tag{13}$$

where $K_{abc} = T_v K_{012}$, $K_{abc} = [K_a;\ K_b;\ K_c]$ and K refers to A, B, C and D.

The following two subsections illustrate the distance estimation by applying KVL on the fault branch using a phase a to ground fault and a phase a to phase b fault as examples.

A. Phase a to ground fault

For a phase a to ground fault as shown in Fig. 6a, applying KVL on the fault branch leads to (14).

$$V_{xa} = V_{fa} - R_{fa}I_{fa} \tag{14}$$

By equating the phase a voltage in (13) to (14), and manipulating assuming the fault impedance is resistive, a 3rd order polynomial can be obtained to calculate the fault distance x (15).

$$A_{N_a} + B_{N_a}x + C_{N_a}x^2 + D_{N_a}x^3 = 0 \tag{15}$$

where $K_{N_a} = im(K_a) - re(K_a)im(I_{fa})/re(I_{fa})$, $re(\ )$ and $im(\ )$ refer to real and imaginary parts respectively, K refers to B, C and D, and for A, $K = A - V_f$.
The solution of (15) leads to three roots at each frequency considered and the correct root should satisfy the conditions:
1) real positive value   2) less than 1 pu.

After extensive simulation studies, it has been found that only one root fulfils the conditions at each frequency. However, in a very few cases, at some frequencies, two roots satisfy the conditions. In these cases, for these frequencies, the estimates were discarded when calculating the final average distance.

The value of x can be used in the next iteration starting from (7) and the fault distance is estimated iteratively. This iterative process terminates when the difference between two iterations is less than a predefined tolerance. In this study, a difference of 50 m between two iterations is used and also the maximum number of possible iterations is set to 10.

B. Phase a to phase b fault

For a fault between phases a and b, the reduced equivalent circuit will be as shown in Fig. 6b and applying KVL to the fault branch results in (16).

$$V_{xab} = V_{fab} - R_{fab}I_{fa} \quad (16)$$

where

$$\begin{aligned} V_{fab} = V_{fa} - V_{fb} \\ V_{xab} = V_{xa} - V_{xb} \end{aligned} \quad (17)$$

As with (15), a 3rd order polynomial that combines both fault phases can be obtained to calculate the fault distance x (18).

$$A_{N_{ab}} + B_{N_{ab}}x + C_{N_{ab}}x^2 + D_{N_{ab}}x^3 = 0 \quad (18)$$

where $K_{N_{ab}} = im(K_a - K_b) - re(K_a - K_b)im(I_{fa})/re(I_{fa})$, K refers to B, C and D, and for A, $K = A - V_f$.

It can be seen from Fig. 4 that the distribution system has multiple lines and sections. The proposed method checks the system section by section starting from the first section next to the measurement node (main substation) until the fault location is identified. This iterative process ends when the estimated distance is less than the total length of the assumed fault section and also the difference between two iterations for the same section is less than a predefined accepted tolerance. The flowchart in Fig. 7 illustrates the procedure of the proposed method.
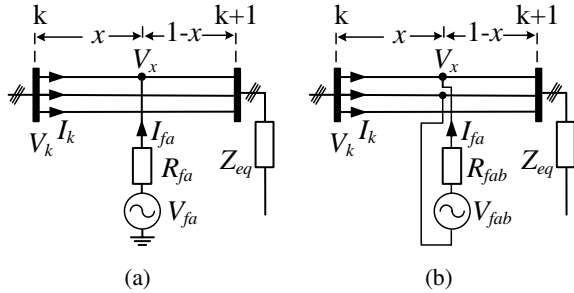

Fig. 6: Reduced system (a) phase a to ground fault (b) phase a to phase b fault

IV. EXPERIMENTAL STUDY

In this section, the proposed IBDG equivalent circuit has been validated experimentally on a 50 Hz, 400 V, three-phase laboratory test system.

A. System description and operation

A commercial drive system has been used to setup the experiment. To emulate an IBDG, the layout in Fig. 8a was used and consists of two Unidrive SP units (classed as a regenerative drive and a motoring drive [28]), a brushless AC servo motor [28], a DC machine, a regen inductor and a switching frequency filter (inductor and capacitor) [28]. This combination is connected to the main power grid at the PCC. Information regarding the system components is provided in Table I. The values for both inductors and the capacitor were selected as close as possible to the recommended values in the
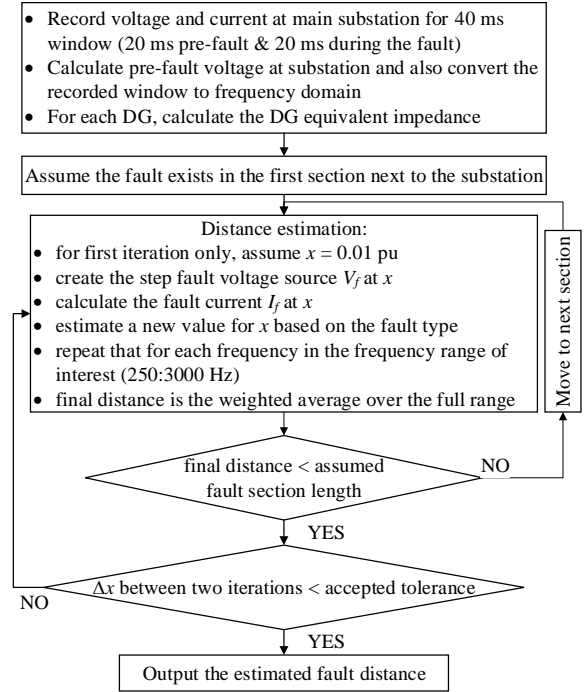

Fig. 7: Procedure for applying the proposed method

drive manual [28] and have been calibrated for the components in the experimental system using an impedance analyzer [29].

The Unidrive SP works in regenerative mode when the power flows from the drive system to the main supply [28]. A control system has been used to run the DC machine which in turns acts as a prime mover for the AC servo motor. By controlling the torque on the DC machine while the speed of the servo motor is controlled by the motoring drive, the sevro motor operates as a generator and the system runs in regenerative mode and the power flows to the main grid. This system emulates a wind turbine. The different components of the experimental system are shown in Fig. 8b.

TABLE I: Parameters of the experimental DG system

regen drive model	SP2403
motoring drive model	SP1406
servo motor model	142UMC300CACAA
regen inductor (L, R)	1.82 mH, 0.8 Ω
switching frequency filter inductor (L, R)	0.75 mH, 0.2 Ω
switching frequency filter capacitor (C, R)	40 µF, 0.5 Ω

B. Equivalent circuit test

A fault of 2 Ω between phase a and phase b has been initiated at the PCC. The line to line voltages and line currents at the terminals of the DG system were measured and filtered with a low pass filter (cutoff frequency of 5 kHz) then captured with a data acquisition system at a sample rate of 20 kHz. The measured voltage between phases a and b and the current in phase a are shown in Fig. 9 where this data window combines pre-fault and during fault periods. The equivalent impedance of the DG as seen from the PCC can be calculated using a data length of 40 ms of the measured voltages and currents (inside the dashed rectangle in Fig. 9). The proposed
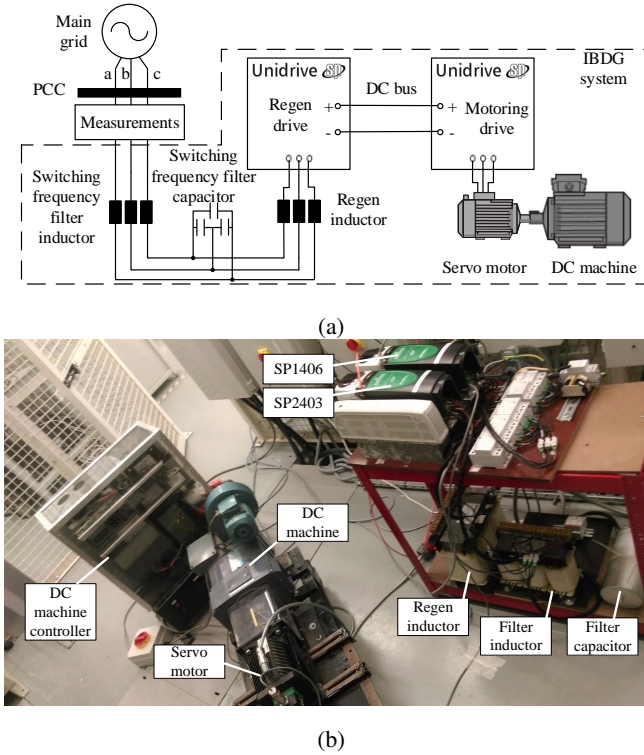
(a)

(b)

Fig. 8: Experimental system (a) layout (b) setup

approximate equivalent circuit is also calculated using the parameters in Table I. The actual measured impedance as well as the approximated equivalent impedance are shown in Fig. 10. There is a high degree of matching between the two impedances in the high frequency range and a high mismatch in the low frequency range which agrees with the proposed concept for the approximate circuit.

It is worth noting that the shape of the current in the healthy state is not a pure sinusoidal wave and has a high value of the 5th and 7th harmonics. This is not only due to non-linear converter effects but also this is due to the presence of 5th and 7th harmonics in the main grid voltage (1.8% and 0.86% respectively of fundamental). These harmonics appear on the switching frequency filter capacitor and that leads to noticeable harmonic current due to lower capacitor impedance at these harmonics. Due to space limitation, this analysis has not been included in the paper.
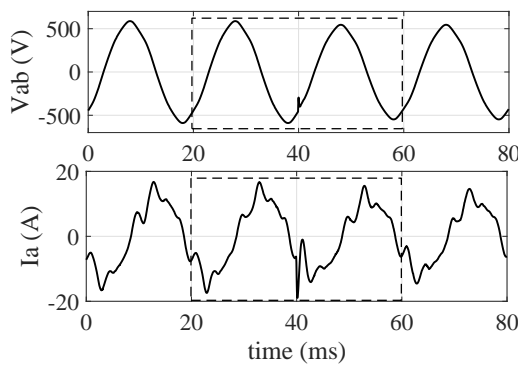

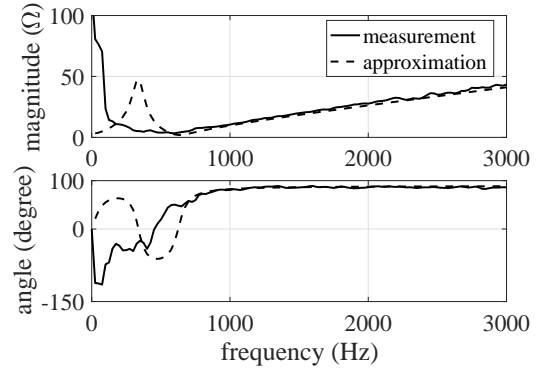Fig. 9: Measured line to line voltage and line current

Fig. 10: Experimentally measured impedance and approximated impedance for the DG system

V. SIMULATION STUDIES

A. Case study

The IEEE-34 bus feeder has been used to verify the proposed concepts and is shown in Fig. 11 [30]. This feeder is a real medium voltage feeder that exhibits asymmetrical non-homogeneous lines, unbalanced loads and single and three-phase laterals. In this study, line asymmetry has been considered in the simulation by using the general distributed line model included in the Matlab/Simulink library. IBDG and SBDG have been connected at different locations along the feeder according to the assessment scenario. A sampling rate of 20 kHz has been used for voltage and current capture at the main substation for a period of 40 ms (20 ms pre-fault and 20 ms during the fault). Regarding the IBDG, it has been simulated as presented in Fig. 1a with a DC source connected at the DC side of the DC/AC inverter. The operating modes considered by the control system of the DG are the PQ control mode and the current limit mode [31]. In the former, the inverter follows a reference for active and reactive power demand. Depending on the fault severity and due to the low thermal inertia of the inverter switches, the current limit mode is activated if the DG current exceeds 2 pu [31]. Therefore, the simulation studies consider two different operation modes for the IBDG. Detailed parameters for the IBDG are given in Table II. The connection of the filter capacitor is delta and a small resistance has been connected in series with the filter inductors to represent the inductor resistance. A standard 250 kVA synchronous generator model has been used as a SBDG.
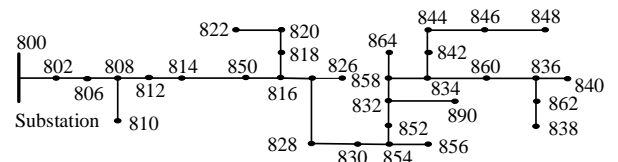

Fig. 11: IEEE 34-bus feeder [30]

B. SBDG equivalent circuit

A SBDG was connected at node 848 and a phase a to phase b fault with a 10 Ω resistance has been imposed at

TABLE II: Parameters of the IBDG

rated power	250 kW	DC side voltage	480 V
line to line AC voltage	250 V	switching frequency	3 kHz
inverter side inductance	0.16 mH	grid side inductance	0.04 mH
filter capacitance	212 μF	damping resistance	0.23 Ω

node 834. The voltages and currents on the medium voltage (MV) side of the DG system were measured and were used to estimate the DG impedance (as seen from the MV side). The measured impedance between phase a and phase b as well as the approximate DG impedance are shown in Fig. 12. It is clear that the approximate model matches the measured impedance in the high frequency range used by the proposed fault location scheme.
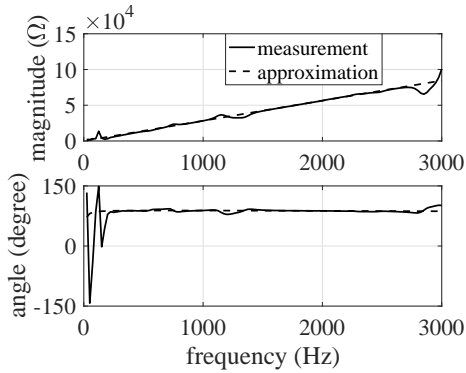

Fig. 12: SBDG measured and approximate impedances

C. Performance of proposed scheme

In this section, the proposed fault location scheme is evaluated considering a variety of factors including fault type, fault point, fault resistance, fault inception angle, noise in measurements and DG conditions. The error in distance estimation is calculated by (19).

$$error = |actual\ distance - estimated\ distance| \quad (19)$$

The fault distance is estimated over a wide frequency range. In this study, the frequency components in the range from 250 Hz to 3 kHz have been used to estimate the fault distance. If necessary, the lower frequency limit may be increased to avoid the effect of possible low order harmonics in the main grid voltage. The upper limit is chosen as it provides a good signal to noise ratio for this system and is suitable with typical instrumentation devices used for this purpose.

To calculate the final estimated distance (considering that the accuracy may be bad for some frequency sub-ranges due to the approximation in the DG circuit representation), the full frequency range has been divided into five equal frequency zones. For each zone, the average distance, standard deviation and number of frequency bins that have a valid estimation are calculated. The final fault distance is calculated as the weighted average for the zones using the standard deviation and number of frequency bins as weighting factors. This is illustrated by (20) to (24).

$$Avg_k = average(dis_k) \quad (20)$$

$$f1_k = 1/std(dis_k) \quad (21)$$

$$f2_k = number\ of\ points(dis_k) \quad (22)$$

$$FZ_k = a1 \times f1_k / \sum_{k=1}^{5} f1_k + a2 \times f2_k / \sum_{k=1}^{5} f2_k \quad (23)$$

$$estimated\ distance = \sum_{k=1}^{5} FZ_k \times Avg_k \quad (24)$$

where dis_k, Avg_k, $f1_k$, $f2_k$ are the vector of estimates, average value, inverse of standard deviation and number of points for zone number k and k has values from 1 to 5, $a1$ and $a2$ are the weights with $a1 + a2 = 1$.

1) Effect of line transposition and capacitance: This section examines the effect of the line transposition and the line capacitance on the accuracy of the fault location. IBDGs have been connected at nodes 840 and 848. Line to line faults have been simulated at different locations (fault resistance is 10 Ω). Even though the line is simulated by its asymmetrical parameters including the line capacitance, the fault distance has been estimated while considering the actual line case (case 1), assuming transposed line (case 2) and ignoring the line capacitance (case 3). The results are presented in Table III. It is clear that ignoring the line transposition increases the error. Also, the line capacitance has a significant effect and must be considered in the fault location algorithm.

TABLE III: Effect of line transposition and capacitance test

distance (km)	0.5	6.2	16.85	27.1	33.3
error (m), case 1	34	80	22	25	31
error (m), case 2	68	149	1063	1404	889
error (m), case 3	11	2165	1783	7357	5612

2) Effect of fault resistance: Fifty fault resistance values between 0.01 Ω and 100 Ω (randomly generated) have been used in this scenario to evaluate the performance of the proposed method. For each fault resistance value, a single line to ground (SLG), a line to line (LL), a line to line to ground (LLG) and a three-phase (3-ph) faults were simulated at seven locations along the feeder. These locations lie at distances of 0.5, 6.2, 16.85, 27.1, 33.3, 47.1 and 57.25 km from the main substation. A fault inception angle of 90° and two IBDGs connected at nodes 848 and 840 were used. For each fault type, 350 fault cases were simulated.

The error in distance estimation for different fault types at location 27.1 km is shown in Fig. 13. Table IV summarizes the test for each fault type where the total average error (avg), the maximum error (max) and the percentage of cases with an error of less than 200 m (referred to 350 cases) are illustrated. The results obtained reflect the accuracy of the proposed scheme against fault resistance. For 1400 fault cases, the average error is 71.3 m and 1352 cases (96.57%) were estimated with an error of less than 200 m.

Even though the proposed scheme assumes the availability of a 20 ms data window during the fault, it has also been evaluated using only 10 ms data window. The evaluation shows an insignificant increase in the error, for instance, the average

error for SLG faults at different resistance values increased from 95 m to 107 m.

The proposed method as well as other single end impedance based methods assume the fault is purely resistive. Violation of this assumption is expected to increase the error in estimation. In an initial study, SLG faults have been simulated with an impedance (resistance and inductance). The error in distance estimation does not exceed 1 km with a fault inductance value of 500 times the line's per unit self-inductance.
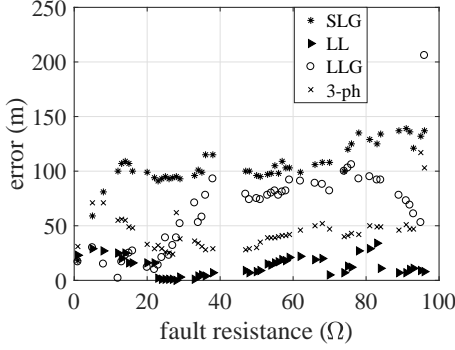

Fig. 13: Error in estimation at different fault resistance values

3) Effect of fault inception angle: To assess the performance of the proposed scheme at different fault inception angles, 50 random values between $0°$ and $180°$ were used to simulate different fault types at the previously described seven locations. A fault resistance of 10 Ω and two IBDGs connected at nodes 848 and 840 were used.

To save space, the test summary is provided in Table IV. The results in Table IV show a high maximum error value and this error occurs when a small fault inception angle is used and the transient magnitude is reduced by this small fault inception angle. The total average error for the 1400 simulated fault cases is 61.3 m with 1363 cases having an error of less than 200 m.

TABLE IV: Summary for fault resistance and inception angle tests

fault	fault resistance			inception angle		
	% cases	error (m)		% cases	error (m)	
		avg	max		avg	max
SLG	94.3	95	336	92	95	794
LL	100	47	199	99.1	49	440
LLG	94	74	476	98.8	56.2	249
3-ph	98	69	229	99.4	45.1	212

4) Noise in measurements: The measured voltage and current are susceptible to error due to surrounding noise and accuracy of the measuring devices. In this section, Gaussian noise is randomly added to the voltage and current signals at the main substation. Also, a 16 bit quantiser is used to represent the analogue to digital converter. Two noise levels have been implemented (2% and 5%). The noise level is calculated as a percentage of the root mean square value of the phase voltage and current. SLG faults with a 10 Ω resistance have been simulated. Two IBDGs were connected at nodes 850 and 848. The results are shown in Fig. 14 with noise and without noise (0%). Even though there is an increase in the error values, the accuracy of the estimation remains very good.
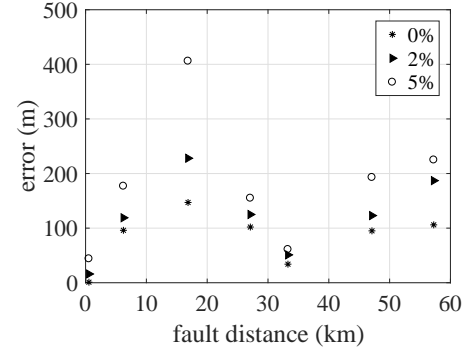

Fig. 14: Error in estimation due to noise in measurements

5) Effect of DG conditions: Both IBDG and SBDG were used in this scenario. SLG faults with a fault inception angle of $90°$ and a resistance of 10 Ω were simulated at different locations. Table V shows the error in the estimated distance for the different cases where for each case, the DG type is mentioned as IB or SB for inverter based and synchronous based respectively followed by the DG connection node(s). The results demonstrate the success of the proposed DG equivalent circuit for the high frequency analysis based fault location method.

TABLE V: Test summary for different DG conditions

DG	error (m) at locations (km)						
	0.5	6.2	16.85	27.1	33.3	47.1	57.25
IB(848, 840)	31	132	66	92	35	73	154
SB(848, 840)	3	36	8	62	37	88	52
IB(848, 850)	1	96	147	102	34	95	106
IB(848, 840) & SB(828)	19	137	60	90	35	68	187

6) Locating faults along a lateral: Impedance based fault location methods have a common drawback—the "multiple estimation problem". Due to existence of laterals in the distribution systems, multiple points along the system may have the same electrical distance from the main substation. In this paper, it has been assumed that fault indicators (FIs) are installed at different laterals such that the FI provides a logic signal indicating the faulted lateral and the proposed fault location method based on measurements at the main substation estimates the fault distance either along the main feeder or along the faulted lateral. The optimal deployment of FIs for fault management in distribution systems has been considered recently [32]. It is worth noting that, if a DG is installed along the lateral, a directional FI will be needed. A Multi-Level Fault-Current Indicator (MLFCI) would be a cost effective alternative to the directional FI as proposed in [33]. To check the performance of the proposed scheme to locate faults along a lateral, SLG faults with a 10 Ω resistance have been simulated at different points along the lateral between nodes 816 and 822. For this test, an IBDG is connected at node 850 and SBDG is connected at node 848. The error in distance estimation is illustrated in Table VI where the fault distance is referred to node 816 (start node of the lateral). The results obtained emphasize the accuracy of the proposed method to locate faults along the lateral.

TABLE VI: Error in estimating faults on lateral

distance (km)	1.25	2	3.5	6.4	7.9	9.3	12.25
error (m)	13	17	43	16	20	16	8

7) Comparison with other methods: The proposed method has been compared to some recently proposed impedance based techniques [6]–[8], [10]. Synchronized measurements were used in [6]–[8], [10]. In [10], single end measurements were used and an operating-condition based IBDG model was derived. For all of [6]–[8], [10] as well as the proposed scheme, the IEEE 34-bus feeder has been used for validation of the method. For comparison in similar operating conditions, the average (avg) and the maximum (max) error values reported in [6]–[8], [10] for a SLG fault with different fault resistance values are compared to the error obtained using the proposed method. The maximum fault resistance value in [6]–[8], [10] is 25, 40, 100 and 100 Ω respectively.

TABLE VII: Comparison between methods

method	[6]	[7]	[8]	[10]	proposed
avg error (m)	29	272	17	450	95
max error (m)	58	580	32	1300	336

It is clear that using synchronized measurements in [6]–[8] provides better performance than the single end method in [10]. The error obtained by the method proposed here is much lower than the error reported in [10] and comparable to methods that use multiple measurement points.

The extensive simulation studies and the comparison with other methods emphasize the improved accuracy of the proposed methodology by considering the DG as a passive circuit and using only single ended measurements. For all simulated fault cases at different conditions, it has been found that 95.3% of cases achieve an error in distance estimation of less than 200 m and the total average error is 67 m—for a feeder with a longest path of 58 km.

VI. Conclusion

A wideband single end fault location scheme suitable for distribution systems with distributed generation has been presented. The proposed method employed the distributed parameter line model. High frequency equivalent models for both IBDG and SBDG have been developed. The IBDG model has been experimentally validated on a 400 V, three-phase system. The DG models have been used in the derived fault location scheme and the method showed a good accuracy in simulation studies. The evaluation of the method on the IEEE 34-bus feeder considered the effect of the fault point, fault type, fault resistance, fault inception angle, noise in measurements and DG operating conditions. Under different test conditions, the total average error is 67 m and 95.3% of cases achieved an error of less than 200 m. This level of accuracy encourages the implementation of the proposed scheme for practical application. The authors are now looking to test these concepts on an appropriate experimental system.

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