High-temperature validated SiC power MOSFET model for flexible robustness analysis of multi-chip structures

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***Abstract*—This paper presents a statistical analysis on the effect of parallel connection of SiC power MOSFETs in high current applications. To this purpose, a reliable temperature-dependent SPICE model is calibrated on static and dynamic experimental curves of 1.2kV-36A commercial SiC MOSFET. The statistical fluctuation of threshold voltage and on-resistance is evaluated on 20 device samples and modeled with Gaussian functions. The proposed analysis, based on SPICE electro-thermal Monte Carlo simulations, is then aimed to improve the design of high current systems with multi-chip devices. Therefore, the study is focused on the evaluation of current and energy unbalance during device switching under inductive load. Results achieved for nominal switching condition and out-of-SOA current levels are discussed.**

***Keywords*—Electro-thermal modeling; Monte Carlo simulation; power MOSFET; silicon carbide (SiC); SPICE.**

I. INTRODUCTION

Silicon carbide (SiC) power MOSFETs are finding widespread adoption in many application areas, such as energy distribution, automotive and aircraft, thanks to many excellent features. In several high power applications there is the need to use parallel devices, since commercial SiC MOSFETs are mostly available for low current ratings. Although for Si MOSFETs and IGBTs paralleling is well known and commonly used in many applications [1], [2], poor information is available in literature for SiC MOSFETs. Compared to commercial SiC modules [3], the use of discrete devices in parallel has some benefits: *(i)* the generated heat could be more evenly distributed over the heatsink (thus reducing temperature peaks); *(ii)* during the design process, flexibility is gained in terms of number of devices to use; *(iii)* lower cost is obtained thanks to the high volume production of discrete parts.

However, when paralleling two or more SiC MOSFETs, their currents may not be balanced due to the statistical fluctuations of the on-state resistance (R_{on}) and threshold voltage (V_{TH}) from sample to sample. This phenomenon can drastically reduce the reliability of the entire power system [4]. Previous works [5], [6] have suggested different feedback techniques for balancing drain currents during switching transients. However, those methods could be applied just for two parallel devices, and increase the overall system cost. In [7] an experimental study on the SiC MOSFET's self-balancing capability without adding any sensing or control circuit is presented. The parameters used to balance paralleled devices are the gate drive voltage and resistance. However, this solution requires a tailored gate drive circuit for each device and could not be applied to modules. Another way to address this problem could be the adoption of design rules to determine the maximum allowed device parameters dispersion and parasitic circuit elements unbalance [8]. To optimize these rules, a valid approach involves a simulation analysis that quantifies the impact of device and circuit mismatches on the application performances. Since SiC MOSFETs often operate under harsh conditions, reliable electro-thermal (ET) simulations are mandatory for design optimization. In the last years, several papers have focused on the modeling of SiC MOSFETs [9]; some of them rely on empirical functions [10], while others are based on physics-based descriptions [11].

In this paper, a temperature-dependent SPICE model for SiC MOSFETs [12] is exploited for dynamic ET simulations of single and paralleled devices, both in SOA and out-of-SOA conditions. An experimental measurement campaign on 20 virtually identical devices is used to characterize the statistical distribution of R_{ON} and V_{TH}. Finally, an analysis based on Monte-Carlo ET simulations of 4 paralleled devices during switching is presented. The impact on the statistical energy dissipation is evaluated during turn-on and turn-off transients. Lastly, the potential unbalance in temperature is discussed.

II. SIC MOSFET COMPACT MODEL

In this paper, an extended formulation of a previously presented SPICE model [13] is reported, which has been experimentally verified on a broad range of operating conditions. The schematic representation of a planar SiC MOSFET structure is depicted in Fig. 1.

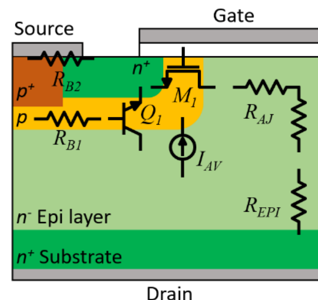


Fig. 1 Structure of a planar SiC power MOSFET and main equivalent circuit components.

$$R_D\left(V_{GS},V_{drift},T\right)=R_{AJ}\left(V_{GS},V_{drift},T\right)+R_{EPI}\left(T\right)$$

$$R_{AJ}\left(V_{GS},V_{drift},T\right)=\frac{V_{drift}}{V_1+V_{drift}}\cdot\left[R_{AJ1}\left(T\right)+R_{AJ2}\left(T\right)\left(1+\frac{V_{GS}}{V_2}\right)^{-\eta}\right]$$

$$V_{TH}\left(T\right)=\left[V_{TH}\left(T_0\right)-\beta_{TH}\right]e^{-\varphi_{TH}\left(T-T_0\right)}+\beta_{TH}$$

$$M=1+a_{II}\tan\left[f_I\left(I_D\right)\frac{\pi}{2}\left(\frac{V_{DS}}{BV_{DS}\left(T\right)}\right)^{b_{II}}\right]$$

$$I_{Therm}=A_{Therm}n_i\left(T\right)^{\alpha_{Therm}}V_{DS}^{\gamma}$$

$$I_{AV}=\left(M-1\right)I_{D(M_1)}+M\cdot I_{Therm}$$

$$\mu_n\left(T\right)=\mu_n\left(T_0\right)\left(\frac{T}{T_0}\right)^{-m(T)}$$

$$m\left(T\right)=-a_m+\left(a_m+b_m\right)\left[1-c_m\exp\left(-d_m\frac{T}{T_0}\right)\right]$$

$$I_{MOS}=\frac{I\left(V_{SENS}\right)\cdot f_\mu\left(T\right)}{\left[1+\theta_1\left(V_{GS}-V_{TH}\left(T\right)\right)\right]\left(1+\theta_2\cdot V_{DS}\right)}\left(1+\lambda\cdot V_{DS}\right)$$

$$C_{DS}\left(V_{ds}\right)=\frac{C_{DS0}\left[\frac{\pi}{2}+\arctan\left(-\frac{V_{ds}}{V_{ds}^*}\right)\right]}{\pi/2}+C_{DSMIN}$$

$$C_{GD}\left(V_{gd}\right)=\left(C_{GD0}-C_{GDMIN}\right)\left[1+\frac{2}{\pi}\arctan\left(\frac{V_{gd}}{V_{gd}^*}\right)\right]$$

Fig. 2 Most relevant equations for compact elements in the SPICE sub-circuit of Fig. 3.

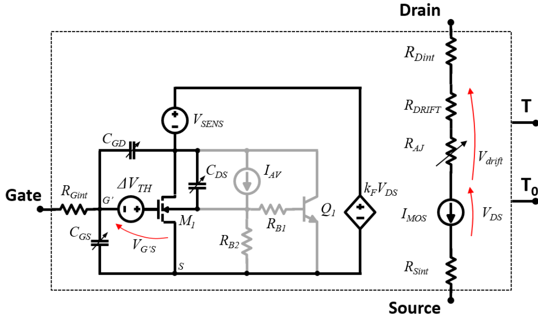


Fig. 3 Developed SPICE sub-circuit, with electrical and thermal nodes. Elements in gray model the out-of-SOA operation.

The model is based on the partitioning of the device into an 'intrinsic' (channel) MOSFET, a bias-dependent resistance for the accumulation and JFET regions, and a constant resistance for the epitaxial drift region. The influence of SiO_2/SiC interface traps on threshold voltage and channel mobility, impact ionization and capacitance nonlinearity are accounted for. The most relevant model equations are reported in Fig. 2, while the related SPICE sub-circuit is depicted in Fig. 3.

The parameters require a simple optimization procedure based on experimental data; the details are given in [12].

A. Model calibration and verification

The device under test (DUT) selected as a case-study is an 80 mΩ 1.2kV–36A 4H-SiC power MOSFET. The model parameters were calibrated on measurements performed at different baseplate temperatures under pulsed (isothermal) conditions. Fig. 4 and Fig. 5 show the transfer and output characteristics at 300 and 400 K.

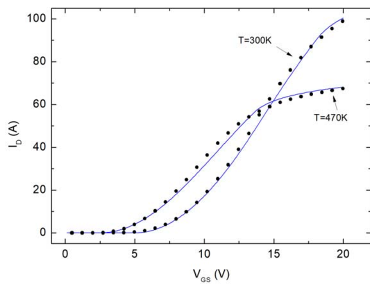
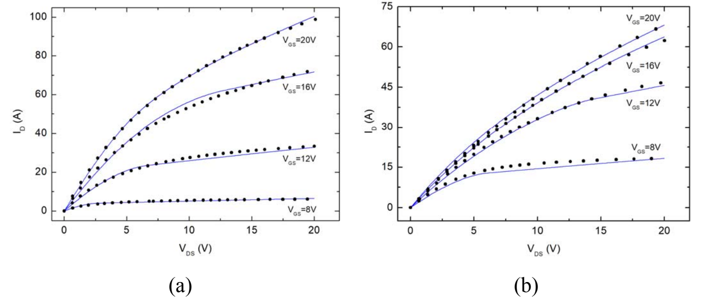


Fig. 4 I_D-V_{GS} curves at T=300 K, T=470 K. Solid lines are SPICE results; symbols are measurements.



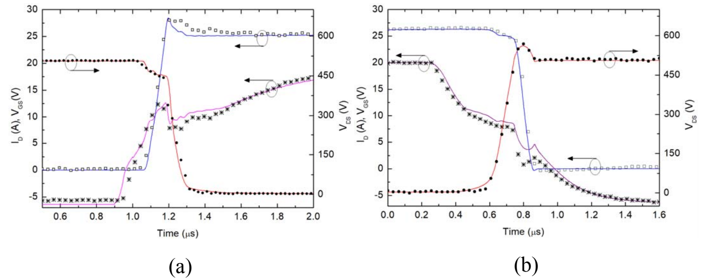
(a) (b)

Fig. 5 I_D-V_{DS} curves at (a) T=300K and (b) T=470K. Solid lines are SPICE results; symbols are measurements.

Excellent agreement was obtained with the experimental dc characteristics despite the smooth triode-saturation transition occurring in SiC transistors. A double-pulse test was used to verify the model accuracy under dynamic conditions. Both turn-on and turn-off current and voltage evolutions are well predicted, as reported in Fig. 6.

III. STATISTICAL ANALYSIS

In order to perform the Monte Carlo analysis, a statistical description of the device parameters fluctuation (R_{on} and V_{TH}) is needed. To this purpose, the MOSFET current factor K and the threshold voltage V_{TH} for all the 20 devices were directly extracted from the highest-slope portion (medium V_{GS}) of the isothermal I_D-V_{GS} transfer characteristics measured at various baseplate temperatures using the quadratic extrapolation method (QEM). The on-state resistance was evaluated on the output I_D-V_{DS} curve for V_{GS}=20 V.



(a) (b)

Fig. 6 Inductive switching waveforms (I_D, V_{DS}, V_{GS}): (a) turn-on; (b) turn-off. Solid lines are SPICE numerical results; symbols refer to the experiment. V_{BATT}=500 V, L_{LOAD}=1.9 mH, R_G=50 Ω.

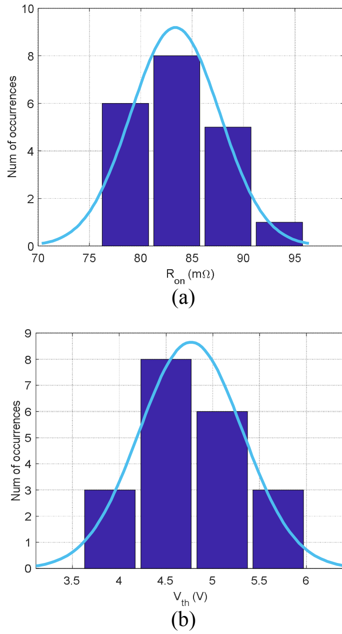


Fig. 7 Histograms of statistical distribution for both V_{TH} and R_{on}, measured on 20 DUT samples at T=27°C, and fitting Gaussian functions (light blue lines).

Fig. 7 shows the histograms of statistical distribution for both V_{TH} and R_{ON} at room temperature. The on-resistance exhibits a spread of about 20 mΩ for the analyzed devices, while the spread for the threshold voltage (evaluated with the QEM) is ≤3.5 V. Optimized Gaussian functions are used to describe the parameters variation in the following Monte Carlo analysis. In particular, the expected value μ and variance σ of the current factor and threshold voltage are properly included in the SPICE sub-circuit.

A. Monte Carlo ET simulations

The proposed Monte Carlo analysis was based on the paralleling of 4 SiC MOSFETs in a double-pulse test. The circuit is shown in Fig. 8 along with parasitic elements and test parameters. An example of the impact of devices mismatches is reported in Fig. 9, which confirms that the individual transistor with lower R_{on} (MOSFET 4) conducts an higher current, while the current sharing during turn-off transient is affected by the V_{TH} unbalance. In particular, the MOSFET with the lower V_{TH} will switch-on earlier and switch-off later than the higher-V_{TH} others. As a consequence, a nonuniform temperature increase takes place. As a relevant result, the MC analysis also allowed quantifying the statistical distribution of the energy dissipation during turn-on and turn-off transients as dictated by the V_{TH} and R_{on} variation. The first analyzed case was for nominal device current I_D=20 A, involving a total load current of 80 A. In this analysis, 1500 MC ET simulation were carried out and the histograms of the dissipated energy evaluated during turn-off and turn-on for each of the 4 MOSFETs are reported in Figs. 10 and 11, respectively. The resulting shape of statistical energy distributions were almost Gaussian with expected E_{off} and E_{on} values of about 580 μJ and 1.3 mJ, respectively. The most useful finding is the considerable switching loss spreading in real applications. For example, derating rules for SiC MOSFETs can be extracted using these data. Another critical point regards the energy unbalance within the same multi-chip structure. Fig. 12 reports the maximum energy unbalances for each Monte Carlo simulation run, evaluated as:

$$\Delta E_{off} = \max\left(E_{off1}, E_{off2}, E_{off3}, E_{off4}\right) - \min\left(E_{off1}, E_{off2}, E_{off3}, E_{off4}\right) \quad (1)$$

$$\Delta E_{on} = \max\left(E_{on1}, E_{on2}, E_{on3}, E_{on4}\right) - \min\left(E_{on1}, E_{on2}, E_{on3}, E_{on4}\right) \quad (2)$$

Pointing the attention only on the switching power loss, the unbalance in temperature rise ΔT can be estimated as:

$$\Delta P_{sw} = \left(\Delta E_{on} + \Delta E_{off}\right) \cdot f_{sw} \quad (3)$$

$$\Delta T_{sw} = \Delta P_{sw} \cdot R_{th} \quad (4)$$

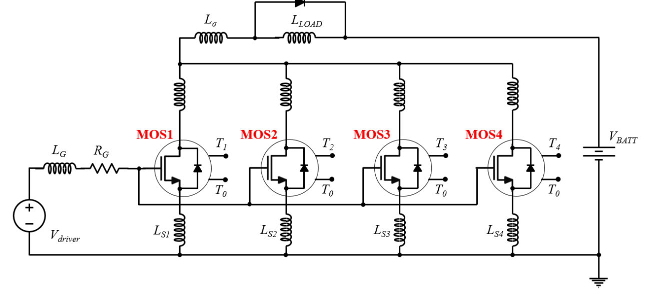


Fig. 8 Circuit model of the four paralleled SiC MOSFET. For each MOSFET, an equivalent thermal network (provided by manufacturer) was used to enable fully coupled ET simulations. V_{BATT}=800 V, I_{LOAD}=80 A, L_{LOAD}=142 μH, R_G=2.5Ω.

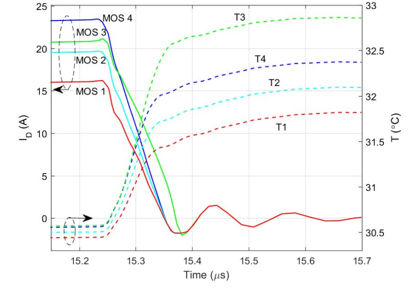


Fig. 9 Paralleled 4 SiC MOSFETs inductive turn-off: currents and device temperatures.

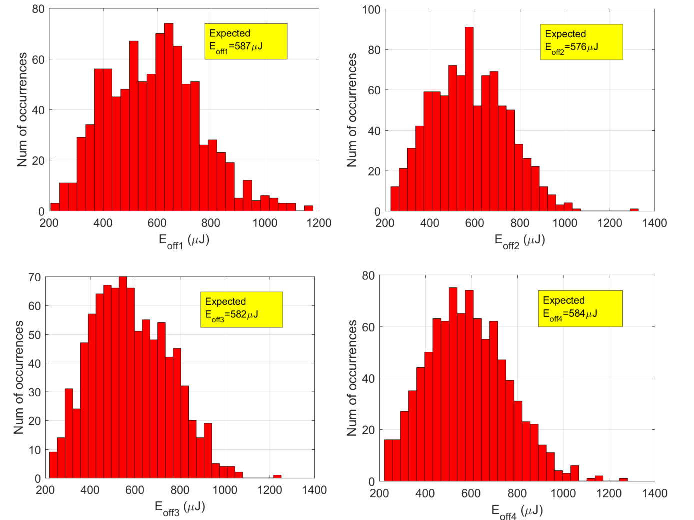


Fig. 10 Histograms of the turn-off dissipated energy evaluated over 1500 MC ET simulations for the 4 MOSFETs at I_{LOAD}=80 A.

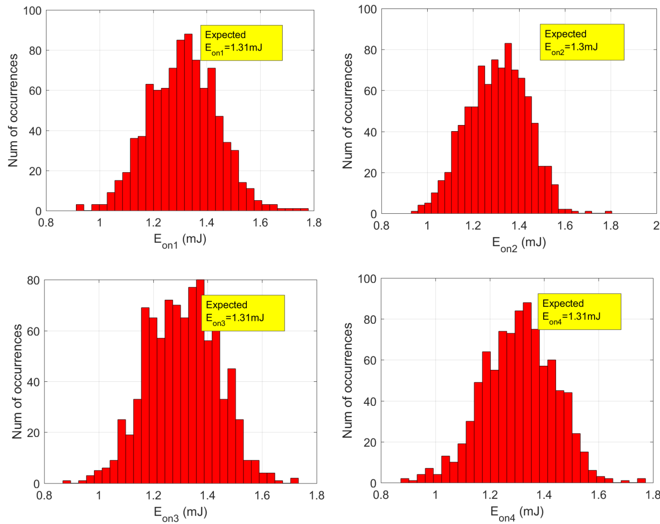


Fig. 11 Histograms of the turn-on dissipated energy evaluated over 1500 MC ET simulations for the 4 MOSFETs at I_{LOAD}=80 A.

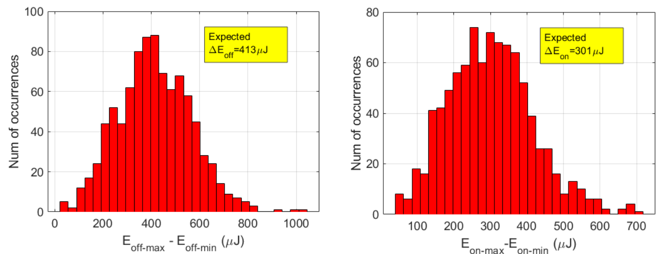


Fig. 12 Histograms of the difference between the maximum and minimum dissipated energy evaluated during (a) turn-off and (b) turn-on over 1500 MC ET simulations at I_{LOAD}=80 A.

Considering the thermal resistance R_{th} of the SiC MOSFET used in this paper (R_{th}=0.6 K/W), with a switching frequency of 80 kHz the above expressions provide a maximum temperature difference $\Delta T \approx 34$ K. However, (4) just gives an indication for the design of a power system. In fact, due to the negative temperature coefficient of V_{TH} [12], the switching loss difference will increase due to ET effects, and then a positive feedback can arise. On the other hand, the R_{on} increase with temperature is expected to partially compensate such temperature difference. It is desired and important to minimize the switching loss difference caused by threshold voltage variance, since the switching loss difference turns into difference in temperatures of the paralleled devices.

Lastly, in Fig. 13 a first attempt to the out-of-SOA analysis is given with the evaluation of switching loss unbalance for a total load current of 160 A (40 A × 4 MOSFETs). The results in terms of ΔE_{off} and ΔE_{on} can be used to analyze the impact of device mismatches on the reliability of the entire power multichip module.

IV. Conclusion

In this work, a statistical analysis on the effect of parallel connection of SiC power MOSFETs in high-current applications has been presented. The analysis relies on a temperature-dependent SPICE model calibrated on dc and transient experimental curves of a 1.2 kV–36 A commercial SiC MOSFET. The statistical fluctuations of threshold voltage and on-resistance have been evaluated on 20 devices, and a Gaussian fitting was used to perform SPICE electro-thermal Monte Carlo simulations. The study, focused on the evaluation of current and energy unbalance during switching under inductive load, gives helpful indication on the impact of V_{TH} and R_{on} statistical fluctuation in real applications.

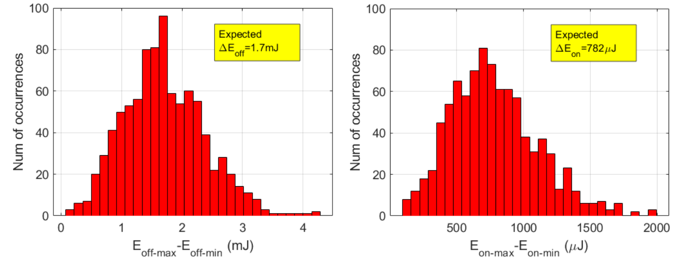


Fig. 13 Histograms of the difference between the maximum and minimum dissipated energy evaluated during (a) turn-off and (b) turn-on over 1500 MC ET simulations at nominal I_{LOAD}=160 A.

V. References

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