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Ultrasonic attenuation measurements at very high SNR: Correlation, information theory and performance.

Richard Challis, Vladimir Ivchenko and Raied Al-Lashi

Electrical Systems and Optics Division, Faculty of Engineering
University of Nottingham, Nottingham NG7 2RD

E-mail: richard.challis@nottingham.ac.uk

Abstract. This paper describes a system for ultrasonic wave attenuation measurements which is based on pseudo-random binary codes as transmission signals combined with on-the-fly correlation for received signal detection. The apparatus can receive signals in the nanovolt range against a noise background in the order of hundreds of microvolts and an analogue to digital convertor (ADC) bit-step also in the order of hundreds of microvolts. Very high signal to noise ratios (SNRs) are achieved without recourse to coherent averaging with its associated requirement for high sampling times. The system works by a process of *dithering* – in which very low amplitude received signals enter the dynamic range of the ADC by 'riding' on electronic noise at the system input. The amplitude of this 'useful noise' has to be chosen with care for an optimised design. The process of optimisation is explained on the basis of classical information theory and is achieved through a simple noise model. The performance of the system is examined for different transmitted code lengths and gain settings in the receiver chain. Experimental results are shown to verify the expected operation when the system is applied to a very highly attenuating material – an aerated slurry.

1. Introduction

This paper describes an ultrasonic spectrometer for measurements of compression wave attenuation and phase speed as functions of frequency at very much higher signal to noise ratios (SNRs) than would be expected from a conventional system based on a high voltage pulser-receiver. The motivation was a requirement to make attenuation measurements in aerated slurries contained in pipework with diameters up to 150mm. The expected ultrasonic propagation path loss was of the order of 400dB. We have shown [1] that the ideal path loss which maximizes SNR in attenuation data is 1Np, equivalent to 8.68dB, a factor of 46 below the stated 400dB. A further constraint was that the test slurries would be flowing along the pipe with the likelihood that the physical properties of the material between the interrogating transducers would not be stationary. This implies that insufficient time would be available to apply coherent averaging to the received signal in order to improve the SNR. In addition, the physical environment in which the test system might be located could be subject to fire or explosion hazards, and this set a further requirement that the electrical signals used to excite the transmitting transducer should have a peak amplitude in the order of 1V.

The solution we have adopted to this combination of adverse SNR conditions and measurement constraints is a spectrometer device in which a code in the form of a low voltage pseudo random binary sequence (PRBS) is used as the transducer excitation signal, and the received signal is extracted

by a correlation operation. In the following sections we outline the basic operation of the system and demonstrate its performance. A number of details in relation to the design of the system are to be found in [2].

2. System operation

Codes and correlation have been used successfully for system identification for many years [3-11]. We have established that although many different types of code, or indeed analogue noise signals, could be used as transmission signals [12] in correlation spectrometers, that which gives the best performance is the Golay code [13]; this is a digital code and broad band in nature. Figure 1 shows the basic system arrangement.

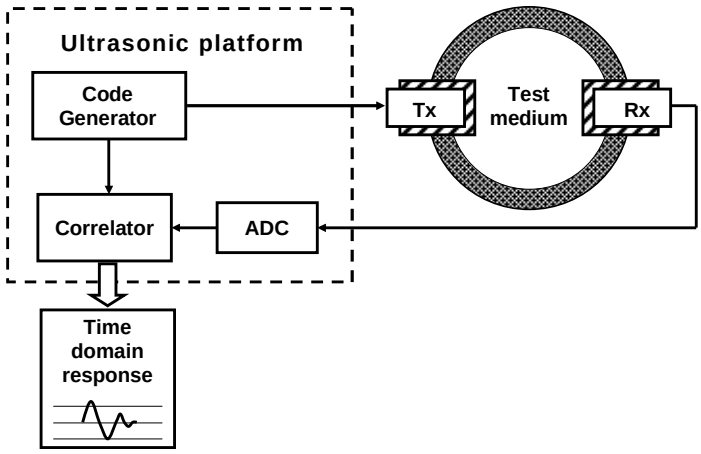

Figure1. The basic system arrangement; Tx and Rx are the transmitting and receiving transducers mounted on either side of the pipe containing the test medium.

The Golay code excites the transmitting transducer and a corresponding acoustic signal passes through the test medium and is received by a second transducer, the output of which is digitized (quantised) by an analogue to digital converter (ADC). It is then cross-correlated with a copy of the transmitted code to produce the impulse response of the whole signal path limited by the bandwidth of the transmitted code. In practice this operation is done twice with two Golay codes (A and B) which are complementary to each other in a binary sense. The auto-correlation functions (ACFs) of the two codes both feature a peak at zero lag as would be expected on the basis that they are both random. However, they are not ideally random due to their finite length, and this results in so-called self noise in their ACFs after the principal peaks at zero lag. The special feature of Golay codes is that the self noise in code A is in antiphase with that of code B. Thus if the ACFs of the two codes are added together the principal peaks add constructively whilst the two self noise components cancel each other. This feature of self noise cancellation usefully follows through to the cross-correlation process – the self noise components in the two cross-correlation functions (CCFs) cancelling in summation. The double transmit-receive-correlate process is illustrated in figure 2.

The resulting output is equivalent to the pulse signal which would have been received using a conventional pulser-receiver system, except that the SNR is far superior. If the raw SNR of either of the received signals (A or B) is SNR_1, then the SNR after the correlation and addition process [2] is

$$SNR_2 = SNR_1\sqrt{2NR} \quad (1),$$

where N is the length of the Golay code expressed as the number of binary state changes, and

$$R = \frac{f_s}{f_{ex}} \quad (2),$$

where f_s is the ADC sampling frequency and f_{ex} is the average frequency of clock state changes associated with the code.

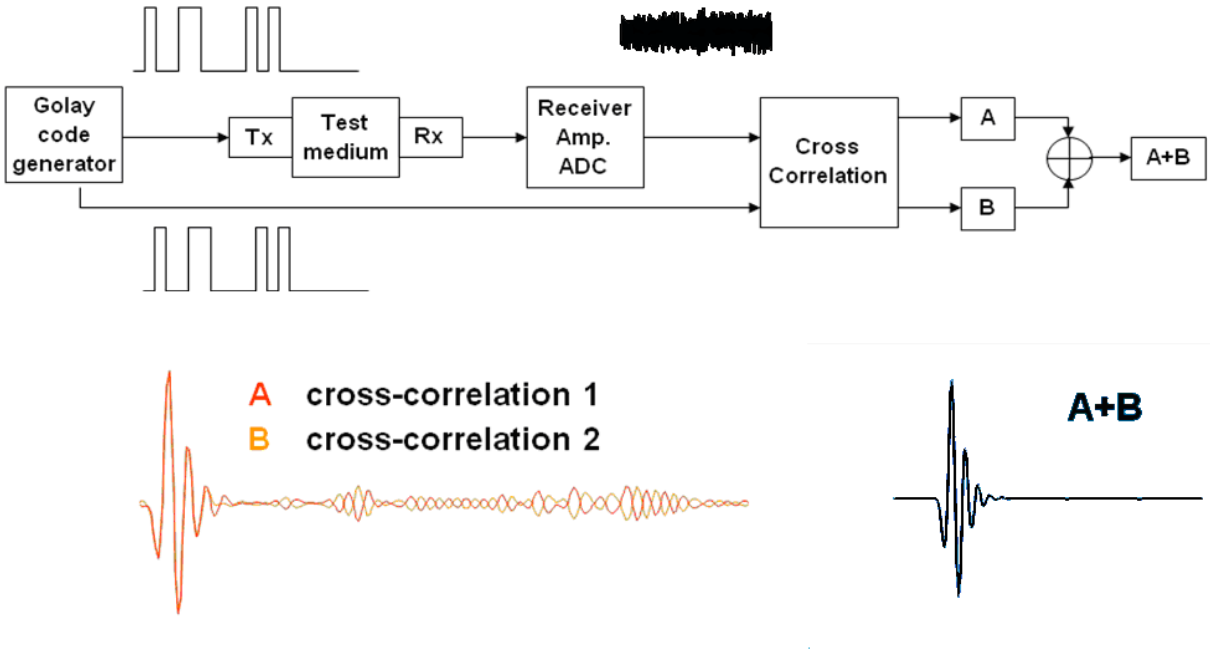

Figure 2. (Top) The double transmit-receive-correlate process. (Bottom) The two cross-correlograms, A and B, showing (left) their self noise components after the initial peaks at zero lag, and (right) the sum of the two with the self noise components cancelled.

3. Initial assessment of performance

The system was implemented in hardware based on a field programmable gate array (FPGA) and applied to measurement of the highly attenuating slurries. The SNR performance was excellent – the system was able to capture a received signal with an amplitude of 70nV against a noise level of 335μV rms and an ADC bit-step equivalent to 488μV, see figure 3. We now describe the implicit signal manipulations that yield this performance and the implications of these on system design.

4. Implicit signal manipulations

The first consideration is how such a small signal can be digitised successfully with a large bit-step in relation to its amplitude. The central phenomenon is that the signal at the input of the ADC adds to the system noise and effectively rides on this noise as it is digitised. This enables signal samples to enter the dynamic range of the ADC, a process known as *dithering* [14-16]. The integration process implicit in the cross-correlation operation (accumulation in digital terms) reduces this noise considerably, leaving the required signal component expressed over several bits of the ADC output, even though its initial amplitude was very much less than a single ADC bit-step.

A central issue which impinges on the design of this type of system is the optimum amplitude for the system noise at the ADC input – the noise on which the input signal rides. Here, if the noise were too great then the processed signal would be contaminated by that noise. Conversely, if the noise were too small the dithering process would be compromised, with distortion and excessive noise at the ADC

output. This problem has been addressed in a number of early works in information theory [17- 20], the principal results of which we will now summarise.

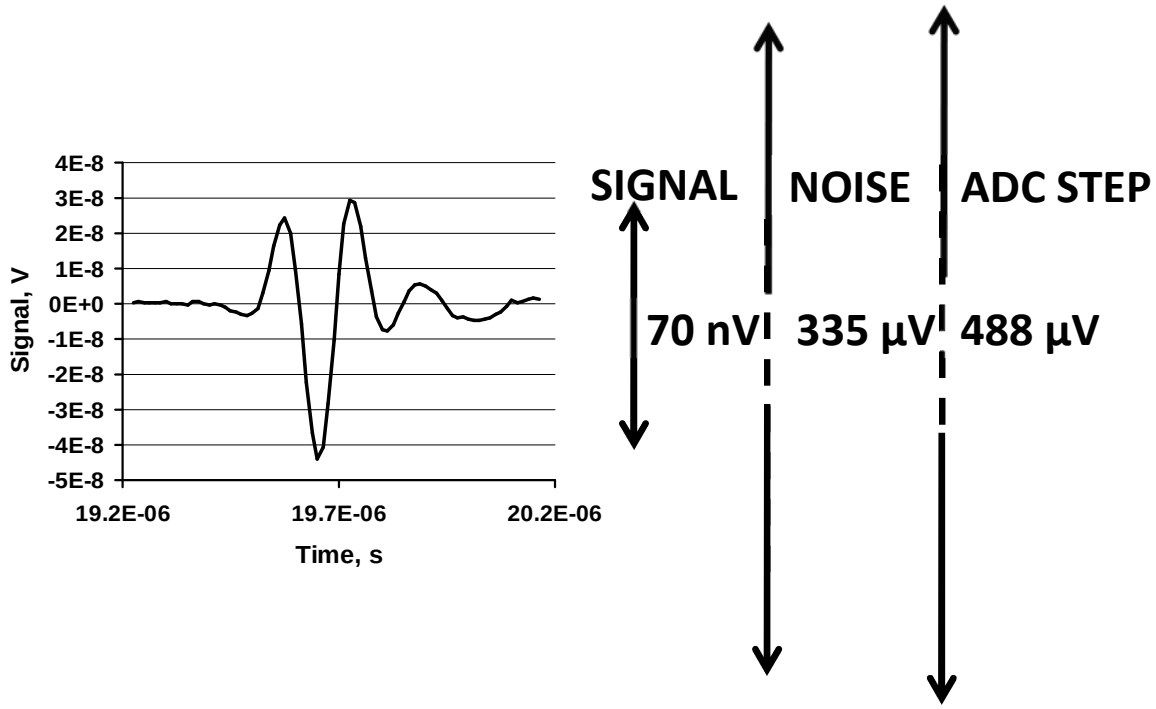

Figure 3. Illustration of a received signal of very low amplitude compared to the noise level at the ADC input and the ADC bit-step.

5. Optimum noise level

Figure 4 illustrates the quantisation process that underpins the operation of the ADC; the horizontal axis represents the input signal amplitude and the vertical axis represents the digitised result. The step amplitude corresponding to one ADC bit is Δ. Figure 5 shows a typical probability density function (PDF) for Gaussian noise with vertical arrows representing the ADC quantisation steps. Expressing the quantisation process in this way leads to the idea that it can be considered as a sampling operation in the amplitude domain. If the noise standard deviation σ were small then the digitised version would be under sampled, and vice-versa. The relationship between the ADC bit resolution and the noise amplitude can be usefully considered by taking the Fourier transform of the amplitude samples on Fig. 5. Here, the input domain to the transform is *amplitude*, and the transformed result is a domain in *reciprocal amplitude*. The Fourier transform of the PDF $p(x)$ is its characteristic function (CF) given by

$$\Phi(u) = \int_{-\infty}^{\infty} p(x) e^{iux} dx \qquad (3)$$

There is a fundamental quantising theorem [18, 19] which states that if $\Phi(u)$ is band limited in the reciprocal amplitude (u)-domain such that

$$\Phi(u) = 0 \quad \text{for } |u| \quad \rangle \quad \frac{\pi}{\Delta} = \frac{\Psi}{2} \qquad (4),$$

where Ψ is the sampling rate in the amplitude domain, then the CF and PDF of x_A can be derived from the corresponding digitized data. This statement is equivalent to the Nyquist theorem for time to frequency transforms.

Figure 6 shows the transformed result (eq. (3)) for Gaussian noise with three different noise amplitudes σ, each normalised to the quantisation step Δ. On figure 6 the ideal sampling condition in the amplitude domain is when the quantisation step is equal to the noise standard deviation,

$$\frac{\sigma}{\Delta} = 1 \qquad (5)$$

The curve for $\sigma/\Delta = 0.5$ is under sampled and that for $\sigma/\Delta = 10$ is over sampled. We have simulated this digitising process [2] in order to assess the extent to which the input noise passes through the ADC to produced digitised *output* noise of the same amplitude for different Golay sequence lengths *N*. Figure 7 shows the result.

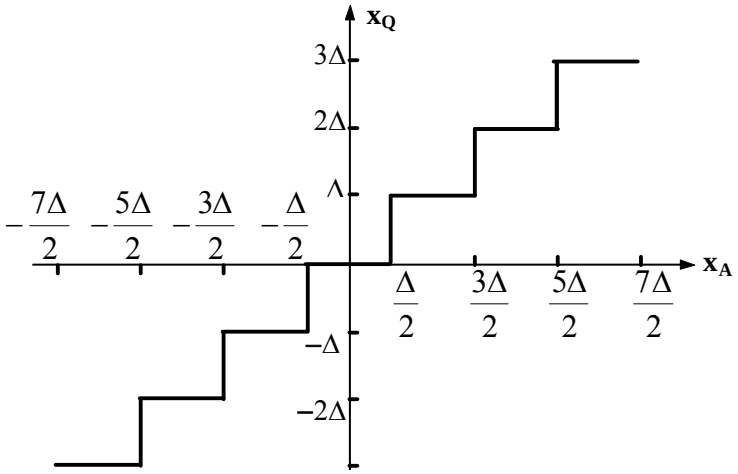

Figure 4. The quantisation process. The horizontal axis represents the input signal amplitude and the vertical axis represents the digitised result.

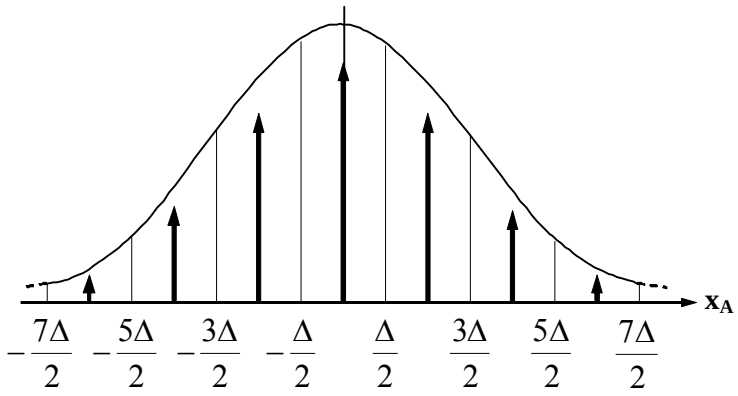

Figure 5. PDF of Gaussian noise showing amplitude samples at intervals of the ADC bit step Δ.

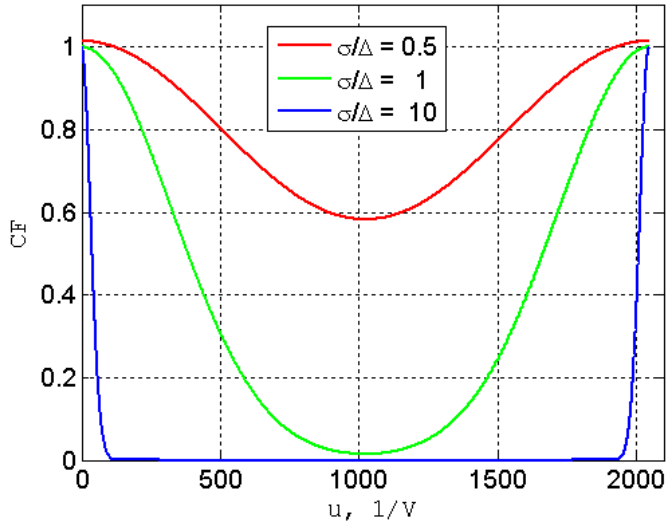

Figure 6. CF of the quantised noise on figure 5 in the inverse-amplitude (u) domain, showing the result for three quantisation rates.

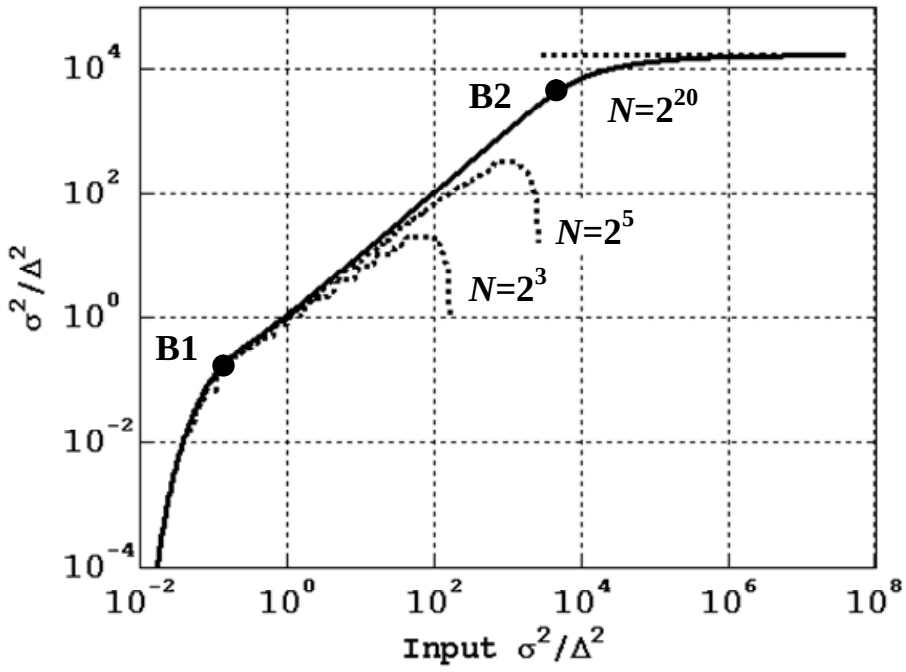

Figure 7. Relationship between the analogue input noise amplitude (horizontal axis) and the digitised noise amplitude (vertical axis), both normalised to the ADC bit step Δ. The results for three sequence lengths N are shown.

The principal curve between break points B1 and B2 matches a result derived many years ago by Brown [17]. At the low amplitude end B1 is the point below which the input noise amplitude is so low that the probability of any sample of it entering the ADC range is negligible. At the higher amplitude,

break point B2 corresponds to a significant probability that samples of the input noise will exceed the dynamic range of the ADC. It is also clear from the figure that to achieve the 'ideal' characteristic between B1 and B2 high sequence lengths N are required. For short sequences, successful transmission through the ADC is possible only for a limited range of noise amplitudes – with σ/Δ around 6 for $N = 2^3$, and around 30 for $N = 2^5$. We established earlier that the optimum noise level was around $\sigma/\Delta = 1$, which when referred to figure 7 would provide for successful operation with short sequences. We would expect that results related to these would arise when a deterministic (information) signal passed through the system, added to the noise in the dithering process.

6. Signal transmission

The same simulation tool as was used to analyse noise transmission was employed to simulate information signal transmission through the system for various levels of noise at the input to the ADC, and for different Golay sequence lengths. The results on figure 8 show that, for input noise amplitudes below around 0.5Δ, signal transmission falls dramatically; this is because the noise amplitude is not sufficient to project enough samples on the input signal into the dynamic range of the ADC. For noise levels above this the signal transmission is unity up until a limiting noise amplitude which increases with Golay sequence length. At this limit the implicit integration in the correlation process is insufficient to reduce the noise to the required insignificant level; only an increase in sequence length can overcome this, with the disadvantage that longer data acquisition times would result.

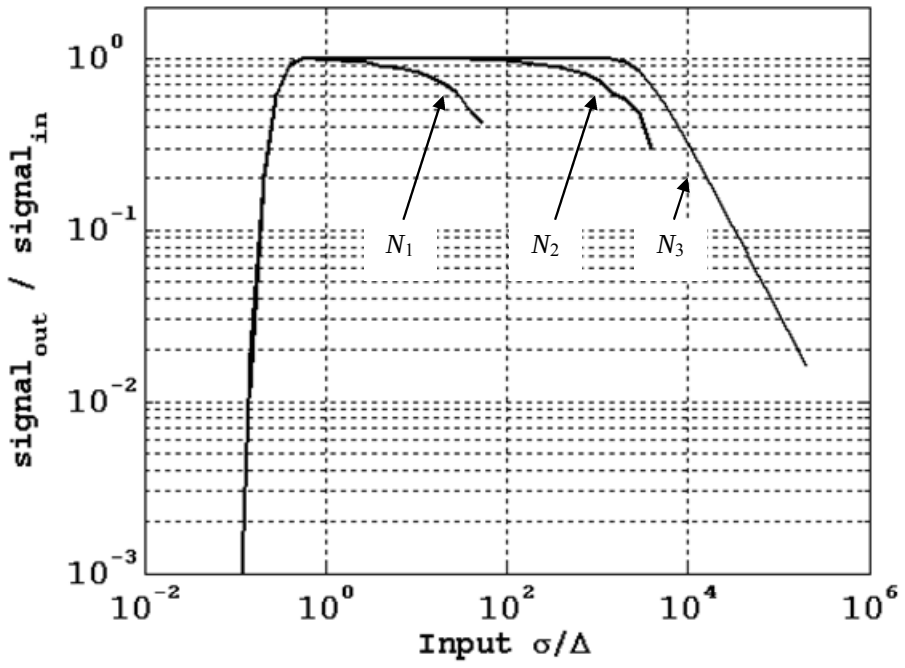

Figure 8. Information signal transmission through the system: The ratio of the amplitudes of the digitised signal and the input analogue signal versus normalised noise amplitude σ/Δ for various sequence lengths $N_1 = 2^{12}$, $N_2 = 2^{18}$, and $N_3 = 2^{30}$.

7. Choice of input noise amplitude

We have seen that the input noise together with the sequence length determine the transmission of both noise and signal through the ADC. If the noise amplitude is too low both signal and noise will be degraded; excessively high noise amplitude has two adverse effects: (i) The dynamic range limit of the ADC is exceeded with consequent distortion, and (ii) Longer sequence lengths will be required so as to improve the SNR in the correlation. In order to check our earlier decision on an optimum noise level we have simulated the SNR performance of the system and figure 9 shows the result. We see the highest SNR is achieved for $\sigma/\Delta = 0.3$, and that lower noise levels bring about a rapid fall in SNR. The SNR also decreases at higher noise levels, but at a lower rate. In relation to system design it therefore makes sense to err on the side of safety and to set the noise level just above 0.3 in order to protect against an unforeseen reduction in noise level in the physical electronic hardware. We have therefore maintained the noise level such that its standard deviation is equal to one ADC bit-step, $\sigma = \Delta$. The source of this required noise will be discussed in a later section.

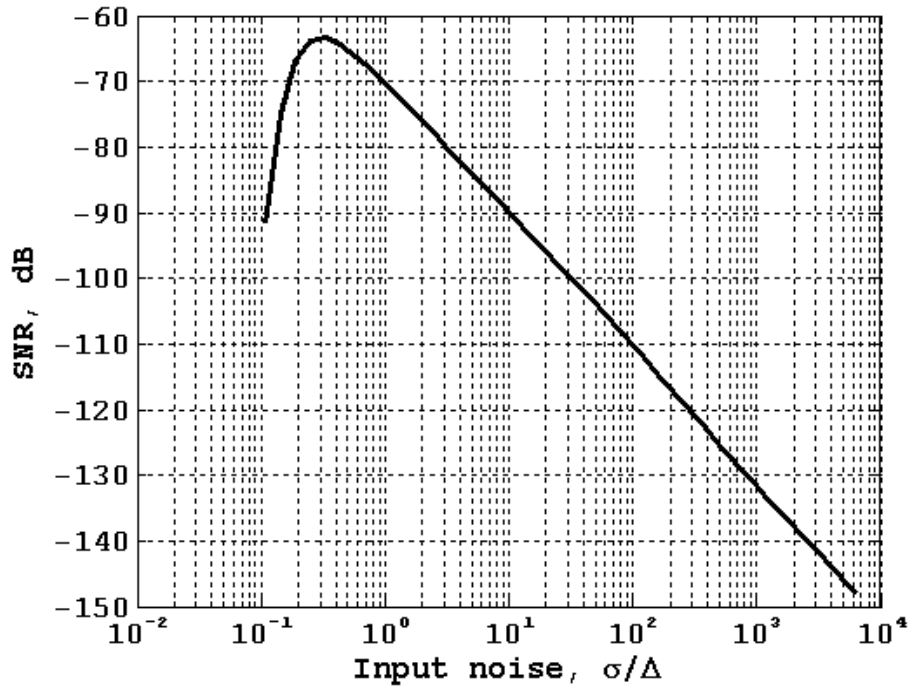

Figure 9. SNR for an input signal of 5 μV amplitude versus input noise normalised to the quantisation step for a sequence length $N=2^{30}$.

8. Minimum input signal

The performance observed for very low signal levels was illustrated in figure 3. It is to be expected that, given an appropriate level of dithering noise, the minimum signal level that is receivable will reduce as the sequence length is increased. We have used the simulation to establish the form of this relationship, and figure 10 shows that this is linear; the cross on the figure indicates the operating conditions of figure 3. It is also clear from the figure that even smaller signals would be receivable with increased lengths – indeed, if the sequence length tended to infinity then the minimum receivable signal would tend to zero. However, high sequence lengths imply long acquisition times, so there is a practical limit which will derive from a combination of the time available for measurement and the stationarity of the physical properties of the test medium.

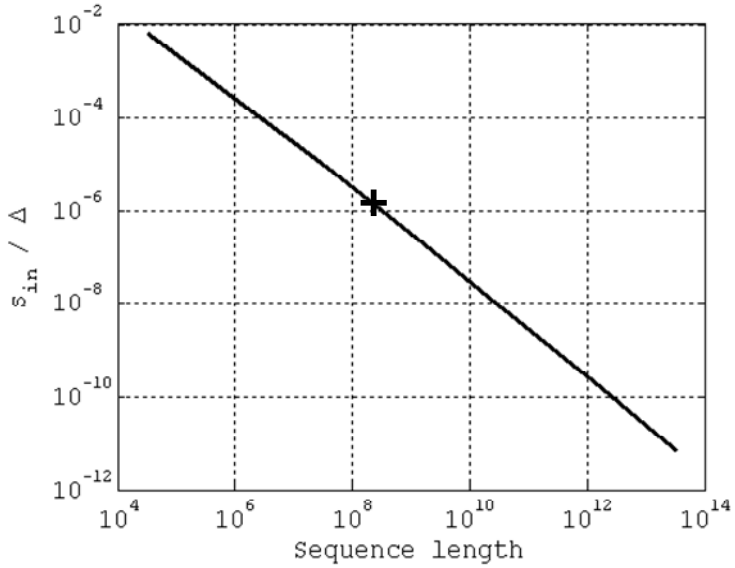

Figure 10. Minimum receivable signal level versus sequence length *N*. The cross indicates the operating conditions of figure 3.

9. Practical considerations in relation to input noise

The ADC bit-step in the current system is 488μV and so for $\sigma = \Delta$ we would require noise at the ADC of this amplitude. In most practical radio frequency electronic systems the commonly used interconnection impedance is 50Ω□□, and with an operating bandwidth of 40MHz this would result in a Johnson noise amplitude of 5.75μV, clearly not enough. Other extraneous noise sources would be expected to exist, and in the current system we have measured the actual noise level at 14.6μV, still very much below the required value. Whilst input amplifiers are normally used to improve SNR, we have used an amplifier/filter combination as a source of dithering noise, figure 11.

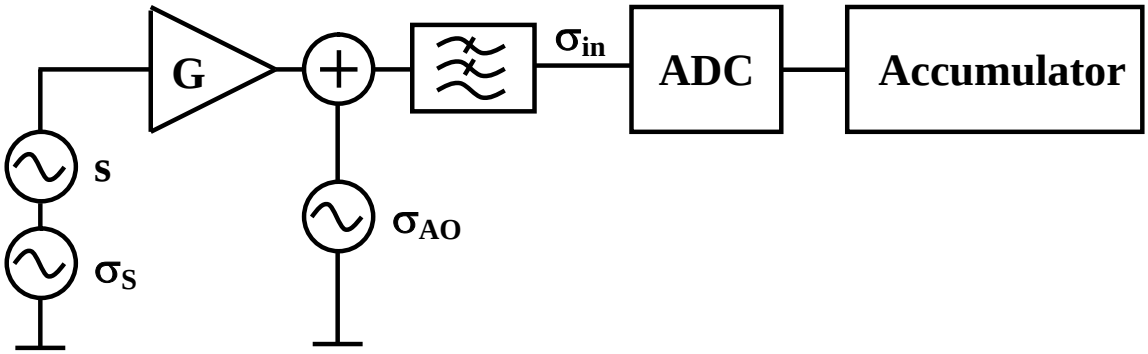

Figure 11. Overall system model. **G** is the gain block (amplifier) which is followed by the filter (insertion loss 10.4dB), the ADC, and the accumulator which represents the integration associated with the cross correlation process. The signal source is **s** and σ_s is the noise at the input; σ_{AO} is the intrinsic noise of the amplifier and σ_{in} represents the noise at the input to the ADC.

The filter insertion loss was 10.4dB, corresponding to factor 0.3. To achieve σ = 488μV we would thus require 1627μV of noise at the filter input. In the arrangement of figure 11 the intrinsic noise of

the amplifier was measured as σ_{AO} = 335μV over the 40MHz bandwidth. The source noise at the input of the amplifier was σ_s = 14.6μV. The noise at the filter input is

$$\sigma_{\text{inf}}^2 = G^2\sigma_s^2 + \sigma_{AO}^2 \quad (5)$$

Re-arranging this we get the amplifier gain as

$$G^2 = \frac{\sigma_{\text{inf}}^2 - \sigma_{AO}^2}{\sigma_s^2} \quad (6)$$

Setting σ_{inf} = 1627μV, σ_{AO} = 335μV and σ_s = 14.6μV yields G = 40.7dB. The amplifier will also magnify the signal at its input, s, giving further advantage in terms of the overall SNR, but only up to a gain limit of

$$G = \frac{\sigma_{AO}}{\sigma_s} \quad (7)$$

Beyond this point the SNR at the output will be dominated by the signal and noise amplitudes at the input of the amplifier. If an amplifier gain setting lower than the required 40.7dB were to be used, the noise input to the ADC would be inadequate for successful dithering, resulting in diminished overall SNR, as established in figure 9.

10. Overall system SNR

We required to establish the noise performance of the system for various combinations of transmission voltage, V_{PRBS}, sequence length N and factor R in eq. (2); we defined a 'quality factor' thus

$$Q_1 = 10\log(2NRV_{PRBS}^2) \quad (8)$$

In order to compare the performance with that of a conventional pulser-receiver system we defined a second quality factor as

$$Q_2 = 10\log(V_P^2 M) \quad (9),$$

where V_P is the transmission pulse amplitude and M is the number of coherent averages applied to the received signal before the SNR calculation. The maximum values for the pulser output and M were 100V and 1000 respectively, representing typical operating conditions and giving a maximum value of Q_2 = 70 dB. For the PRBS system the settings were V_{PRBS} = 2V, R = 2, and a maximum value for N = 2^{33}. The input signal level was 260nV and measurements were done for various amplifier gains in the range 5dB to 43.5dB, the maximum attainable for the device used. The results of these measurements are shown on figure 12 from which we note that the SNRs achievable with the coded system set to a transmitter voltage of 2V are far superior to those of the pulsed system with a transmitter voltage of 100V. The figure also shows the effect of the amplifier gain, the SNR increasing as gain is increased and maximising when G was around 40dB, as expected from eq. (6).

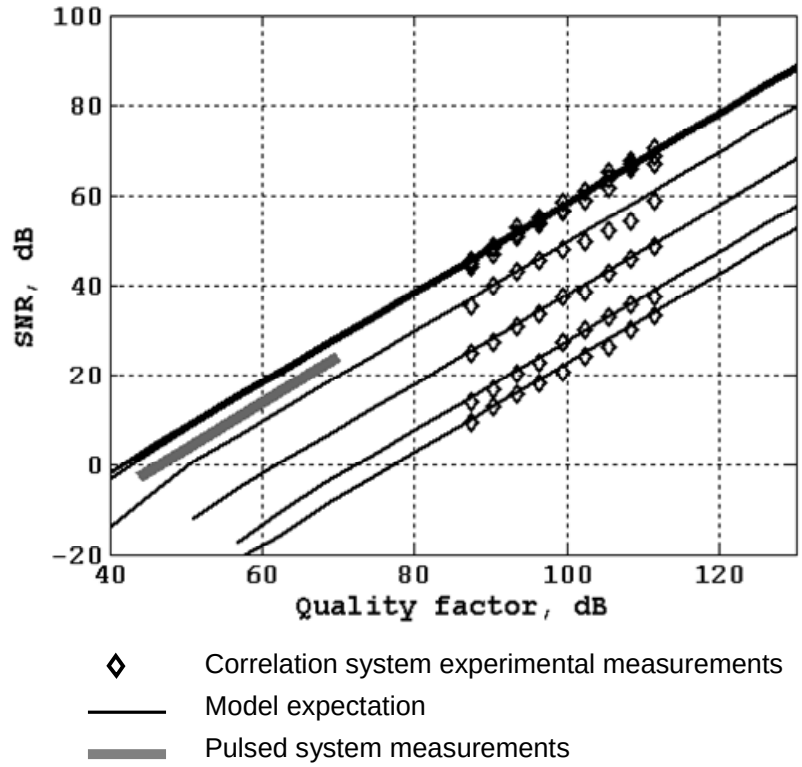

Figure 12. Overall system SNR plotted versus factor $QI = 10\log_{10} V_{PRBS}^2 \times 2NR$ for amplifier gains of (bottom to top) 0, 5, 15, 25, 36, 40 and 43.5 dB. The lines are expectation from the system model and the symbols are experimental measurements. The lines for the three highest gains are approximately coincident. The emboldened solid line is the result for the conventional pulser-receiver system.

11. Concluding remarks

We have discussed the theory and performance of a coded sequence ultrasonic spectrometer and have demonstrated that it can receive signals which are very much lower in amplitude than both the noise at the input of the system and the ADC bit-step. This performance was achieved by a process of dithering whereby the input signal rides on the input noise to reach into the dynamic range of the ADC. The setting of the amplitude of this noise was crucial to the effective operation of the system and necessitated an input amplifier to supply noise of the appropriate amplitude – the standard deviation being equal to the ADC bit-step. In relation to system design, it is necessary to consider all of the noise sources at the ADC input – Johnson noise associated with the input impedance, extraneous input noise, and the intrinsic noise associated with the amplifier.

It should be noted that the dithering concept could also be applied to pulser-receiver systems, in combination with coherent averaging of the received signal to improve SNR. Whilst such a strategy may seem easier than the complexities of coded systems, it has the disadvantage that very long data capture times would be required on account of the necessary delays between successive acquisitions to allow time for acoustic reverberations between the transducers to decay to an acceptable level.

Finally, this outline has not considered the details of the underpinning electronic circuit design, the reason being confidentiality arrangements associated with its commercial exploitation. However, we

can disclose that the FPGA, the programmable gain amplifier, filter and ADC were all off-the-shelf components. The ADC clock runs at 80MHz and the code clock is synchronised to this and runs at 40MHz; The system can be programmed to operate more slowly by successive binary division of both clocks. The Golay code length can be programmed in the range 2^8 to 2^{33}**.** For the future we aim to miniaturise the system and to provide a multiple channel facility for studies of chemical substances that are both flowing and undergoing chemical reaction.

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