Design Optimization of Quasi-Active Gate Control for Series Connected Power Devices

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Abstract

This paper presents a new gate drive circuit for driving a series string of IGBTs. The proposed quasi active gate control (QAGC) circuit is simple to implement as it composes of only a few passive components in addition to a standard gate driver. No separate isolation power supply is required for the upper devices in the stack. The proposed QAGC circuit provides an effective way to drive the power devices and control static and dynamic voltage sharing to the devices at the same time. The theoretical switching operation and the oscillation stability analysis allow criteria for component selection to be established. Limitations of the QAGC circuit is also identified. The modification of the circuit to support more power devices in the series stack is discussed with the aid of the simulation results. The switching operation of the circuit is validated from the experimental results using 2 IGBTs connected in series. The circuit shows a satisfied switching operation with well-controlled dynamic and static voltage sharing and comparable gate voltage between the coupled devices.

Index Terms

Active gate control, power devices, series connection, gate driver, voltage balancing circuit.

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I. Introduction

Power electronic systems are accepted as the key technology to convert and control electrical power flow from one form to another efficiently. A scale of applications could range from a fraction of watt found in consumer products to a giga-watt scale found in utility applications. In some high power applications, there may be case where a power switch used in the converter is in a form of multiple power semiconductor devices combined in series or parallel configuration in order to create a higher voltage or higher current switch respectively. For example, the 150-kV VSC-based HVDC transmission system presented in [1] utilises more than 20 IGBTs in one stack of the switches and connect up to 10 stacks in series to achieve the rated voltage. A high voltage Marx generator in [2] is another example where twelve IGBTs are connected in series to form a single switch with 10 kV and 300 A ratings. In some cases, using low-voltage semiconductor devices as a building block to achieve higher voltage switches is preferred over using a single high voltage device for the better switching performance like the scalable power semiconductor switch (SPSS) developed in [3].

However, the process to assure that no particular device exposes to a higher voltage than the other is difficult in practice as even a slight deviation of the gate signal delay or switching speeds can result in unbalanced voltage distribution across the devices in series connection. Therefore, it is one of the key challenges for the designer to provide voltage balancing methods to the series string to prevent the power devices from a subsequent failure due to an overvoltage and excessive losses.

The static voltage balancing under blocking condition is usually achieved by placing a voltage-divider resistor in parallel with the power device to compensate for device leakage current. However, it is more difficult to balance the voltage during the dynamic period. There are many methods that have been introduced to ensure an equal dynamic voltage sharing. Use of a passive snubber network whether RC or RCD circuits on the power-side of power devices to slow down the switching seems to be the most popular and simplest method to implement as suggested by [4]. However, this method delivers additional losses in bulky passive devices. Therefore, another approach utilizing gate driver control appears to be more attractive due to low power components used in its circuit.

The active gate control (AGC) technique is suitable for non-latching power semiconductor devices like MOSFET and IGBT [5]. It requires the power device to operate in its active region and utilises the relationship between gate and device voltages to control the device switching transient. Active voltage clamping [6], [7] and the auxiliary circuit [8], [9] are among the examples of a simple AGC circuit. Both methods provide additional gate charge fed back to the gate terminal to slightly turn on the device when a voltage overshoot occurs. This results in the device voltage being clamped at the designated level, set either by zener diodes or capacitors. A hybrid circuit of the

RCD snubber and active clamping has been demonstrated in [10] to optimize the total losses. More complicated active control methods may employ feedback control loops [5], [11], [12]. An active voltage control method (AVC) includes feedback control loops to control both dV/dt and overvoltage level of the power devices so that every device follows the same switching trajectory defined from the voltage reference profile [11]. Similarly, the active voltage balancing circuit in [5] involves device voltage control loops to adjust the delay time of each gate signal according to the overvoltage level of the device. Nevertheless, the major drawback of theses methods is complexity and additional cost of control circuits to the gate driver.

A simple technique, quasi active gate control (QAGC), has been proposed in [13]. The proposed method is for series operation of voltage driven power devices. It provides dynamic and static voltage sharing by using a simple RC balancing network and a single gate driver. This paper aims to elaborate on the procedure of parameter design and optimization of the proposed QAGC circuit by taking into account switching transient and stability criteria. In addition, a modified QAGC circuit is proposed in order to support the extension of the QAGC series string. The operation of the QAGC circuit is discussed first in section II. Then, the circuit design criteria are established in section III. A modified circuit is presented in section IV. The circuit is finally validated by the experimental results which are given and discussed in section V.

II. Concept of QAGC Circuit

In Fig. 1, the proposed QAGC circuit drives two IGBTs connected in series to perform as a single switch. Actually, the QAGC circuit is equally good for driving the series string of other voltage-driven devices such as power MOSFETs and JFETs as shown in [13]. The circuit composes of only a standard gate driver and passive devices so it is very simple to implement. The component count is obviously an advantage over the other active control methods considering that those methods require a separate gate drive unit for every power device. The RC balancing network induces the switching operation of the upper switch and acts as a dV/dt snubber of the power devices at the same time. The zener diodes Z_{d1} and Z_{d2} are included to protect the gate from overvoltages and provide paths for device leakage currents while Z_{d3} allows a level shift to prevent static conduction from the gate circuit to the drain circuit.

The proposed QAGC circuit may be put in the same category as the circuits proposed by [14] and [15] in the sense that all circuits switch the series-connected power devices on and off by using the dV/dt action of the lower device to induce the switching of the device above it. Having said that, the QAGC circuit still differs from those mentioned circuits in many ways. The main differences are that initial turn off delay which normally causes sequential switching in these configurations can be diminished by an interdependent mechanism between RC network (R_s and C_s) and the power devices. The circuit also provides more control over dV/dt and static voltage sharing. The resulted turn off voltage transients therefore appear more concurrently. The effects of parameter mismatch such as gate delay time, dV/dt, and leakage currents are handled by the QAGC circuit so that the voltage unbalance level is restricted. The following section discusses the operation principles of the circuit.

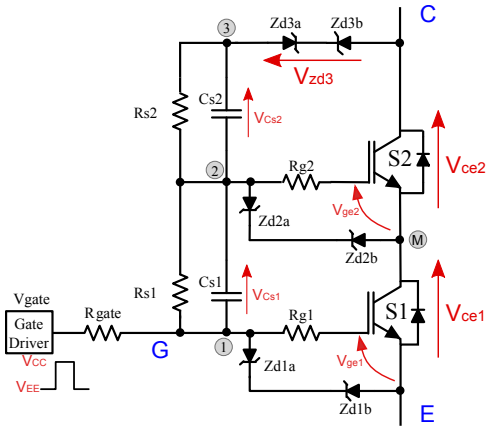


Fig. 1. QAGC circuit for two devices connected in series

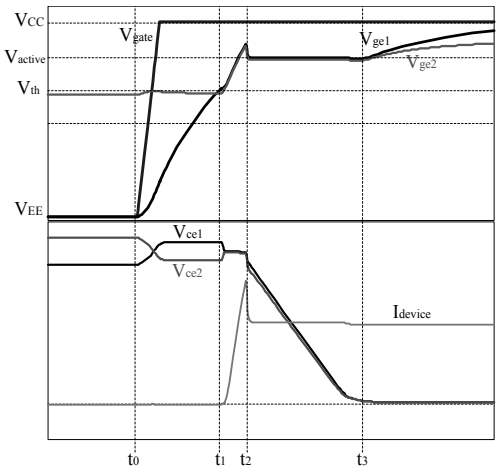


Fig. 2. Waveforms during the turn-on sequence

A. *Turn-On Operation*

The operation of the circuit during turn-on process can be described by a sketch of simulated waveforms in Fig. 2 and by the circuit voltage relationships in (1) and (2).

$$V_{1E} + V_{Cs1} = V_{2M} + V_{ce1} \tag{1}$$

$$V_{2M} + V_{Cs2} = V_{Zd3} + V_{ce2} \tag{2}$$

Initially, V_{ce1}, V_{ce2}, and V_{ge2} stay at their steady state voltages which are determined by the voltage divider network (R_{s1},R_{s2}) and balance of device leakage currents. Both devices are assumed to have identical leakage current for simplicity. The voltage V_{ge2} is considered to stay just below the threshold voltage (V_{th}) (this will be shown later in the section).

The turn-on switching sequence begins at the moment t_0 when the gate drive signal (V_{gate}) changes from V_{EE}

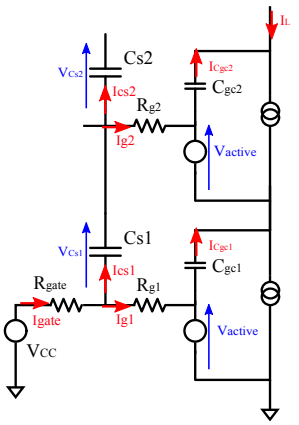


Fig. 3. Gate current flow during turn-on dV/dt

to V_{CC} shifting up the voltage potential V_{1E} by nearly the same amount. According to voltage relationship in (1) and (2), voltage balancing mechanism forces an V_{ce1} to increase which is countered by a drop in V_{ce2} to maintain the level of DC bus voltage (V_{dc}) as suggested in the waveforms during t_0 to t_1. During this period, V_{ge1} continues to charge up and yet to reach V_{th} while V_{ge2} remains just above the threshold voltage.

When V_{ge1} reaches V_{th} at t_1, the impedance of S1 starts to drop thus allowing V_{ce1} to fall. This action is again countered by an increase in V_{2M} ; therefore, V_{ge2} can be raised up above V_{th} as well as V_{ge1} automatically. During t_1 to t_2 , the load current starts to commutate to the devices following the device transfer characteristics.

At the time t_2 when current commutation is completed, both devices are entering the active region; V_{ge1} and V_{ge2} reach the plateau voltage which is determined by device transconductance (g_m) and load current (I_L). The voltages V_{ce1} and V_{ce2} start to fall almost simultaneously so that no voltage overshoot occurs. It is during t_2 to t_3 that the capacitors C_{s1} and C_{s2} play an important role. The gate charge required for the upper device is extracted from the discharging currents of C_{s1} and C_{s2}. The voltage transition speed dV/dt of the power devices are controlled by these capacitors and the gate resistors as expressed in (3) which is derived from the current flow in Fig. 3 under the assumption that dV_{ce1}/dt is approximately equal to dV_{Cs1}/dt.

$$\frac{dV_{ce1}}{dt}, on = \frac{V_{th} + \frac{I_L}{g_m} - V_{CC}}{R_{gate}(C_{s1} + C_{gc1}) + R_{g1}C_{gc1}} \tag{3}$$

Turn-on transient is finished at the end of the active region. After t_3, V_{ge1} and V_{ge2} continue rising further and eventually bring the devices into the saturation region subject to their available gate charge. There is no concern over V_{ge1} as the gate charge is supplied directly from the power supply. However, the required gate charge for S2 to bring V_{ge2} out of the Miller plateau is limited. Though the gate driver supplies the charging current to S2 through R_{s1} during this period, the time constant to increase V_{ge2} to its full gate voltage is too long due to a big value of R_{s1} so it is insufficient in a normal PWM operation. Therefore, it is better to provide the required gate charge just right after t_3 by other means. The further discussion on improving the gate turn on voltage will be given in the next section. The turn-on process ends when both devices are operated in the saturation region indicated by low

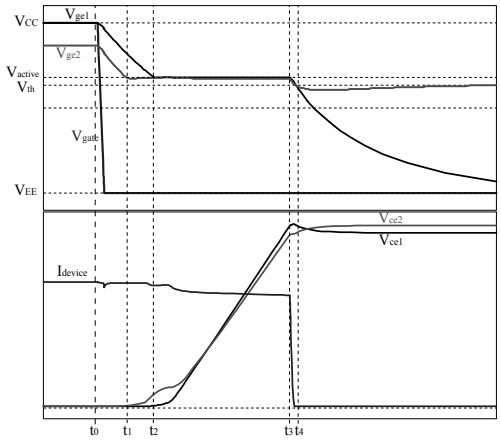


Fig. 4. Waveforms during the turn-off sequence

device on-state voltages.

B. Turn-Off Operation

The process of turn-off operation can be described with the help of the diagram in Fig. 4. The relation ships in (1) and (2) are still applicable.

Initially, both devices are in the saturation region. The gate voltage V_{ge1} is equal to the gate drive power supply V_{CC} while V_{ge2} is lower. Turn-off sequence starts at t_0 when V_{gate} changes from V_{CC} to V_{EE} causing a sudden drop in both V_{1E} and V_{2M}. The gate capacitances of both IGBTs are discharged simultaneously. At the time t_1, V_{ge2} falls to the Miller plateau before V_{ge1} due to a lower gate voltage so that V_{ce2} starts rising first while V_{ce1} remains constant. The QAGC circuit takes action by increasing V_{2M} to balance a rise in V_{ce2}. Discharging current of the upper device is then restricted causing V_{ce2} to slows down as can be noticed in the waveforms.

After some delay, the voltage V_{ge1} reach the Miller plateau t_2 and both devices are in the active region. V_{ce1} and V_{ce2} start to ramp up together. From t_2 to t_3, the balancing capacitors C_{s1} and C_{s2} take full dynamic control of the series string. The voltage slope dV/dt can be determined from the charging rate of C_{s1} and C_{s2} as expressed in (4).

$$\frac{dV_{ce1}}{dt}, \textit{off} = \frac{V_{th} + \frac{I_L}{g_m} - V_{EE}}{R_{gate}(C_{s1} + C_{gc1}) + R_{g1}C_{gc1}} \tag{4}$$

At the end of the dV/dt period (t_3), the whole series string take up the bus voltage V_{DC}. Both devices share reasonably equal voltage. The load current can now be transferred from the devices to the free-wheeling diodes. The current falls sharply and reaches zero current at t_4 while V_{ge1} and V_{ge2} drop to the threshold voltages. The load current is completely commutated to the free-wheeling diode and turn-off transient is considered completed.

After t_4, V_{ge1} continues to drop further to the gate turn-off voltage V_{EE} while V_{ge2} stays nearly constant below its threshold voltage due to slow gate discharging through the high value resistance R_{s1}. For a normal PWM operation where a switching period is much shorter than discharging time constant, V_{ge2} could then appear to be just under

V_{th} during turn off period. Nevertheless, if we allow enough time, the voltage V_{ge2} will fall to the negative value clamped by Z_{d2}. The voltages V_{ce1} and V_{ce2} also move to their steady state values. If the device leakage currents are balanced, then V_{ce1} and V_{ce2} will be determined from the following relationship which is derived from (1) and (2).

$$V_{ce1} - V_{ce2} = (V_{Cs1} - V_{Cs2}) - V_{Zd3} + V_{1E} - 2V_{2M} \tag{5}$$

In many cases, V_{2M} will stay just below V_{th} after dV/dt and the mismatched voltage can be estimated by (6) given that the typical gate voltage swing is ± 15 V.

$$V_{ce1} - V_{ce2} = (V_{Cs1} - V_{Cs2}) - 30 - 2V_{th} \tag{6}$$

It is clear that using the QAGC circuit to drive the series string gives rise to a controlled voltage sharing between the devices during the whole switching stages. The voltages across the power devices are contained within the envelope placed by the voltage divider. The following gives more details of the QAGC operation when the devices have difference leakage current characteristics.

C. Effect of Leakage Current on Voltage Sharing

Practically, leakage currents of individual devices are always unmatched due to manufacturing process. This deviation contributes to unbalanced voltage sharing between the devices and the QAGC circuit handles this unbalanced condition in the following ways.

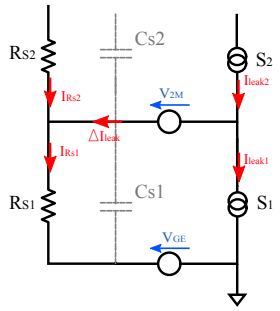


Fig. 5. Simplified QAGC circuit during turn-off steady state

Fig. 5 shows a simplified circuit during turn-off steady state. The upper device has a higher leakage current than the lower one. The circuit will try to balance the leakage current by lower V_{ce2} and raise V_{ce1} until they reach the limit set by V_{Cs2} and V_{Cs1} respectively. Then, the unbalanced leakage current flows through Z_{d3} to the RC network which results in a higher voltage of V_{Cs1}. Also, V_{2M} drops to the negative voltage which is clamped by

the zener diode at the same level as V_{1E}. In this condition, (5) becomes

$$\begin{aligned} V_{ce1} - V_{ce2} &= V_{Cs1} - V_{Cs2} \\ &= \frac{V_{DC}}{(R_{s1} + R_{s2})}(R_{s1} - R_{s2}) \\ &\quad +2\Delta I_{leak}\frac{R_{s1}R_{s2}}{(R_{s1} + R_{s2})} \end{aligned} \tag{7}$$

where ΔI_{leak} is the difference between S2 leakage current and S1 leakage current. We can see that unmatched leakage currents contribute to a higher degree of unbalanced voltage sharing.

However, if the leakage current of S1 is higher, the QAGC circuit would response differently. It will lower V_{ce1} which allows V_{ge2} to increase slightly just to allow more leakage current to flow through S2; hence, balancing the leakage current for both IGBTs. In this circumstance, ΔI_{leak} is zero and it has no effect on the voltage sharing. Therefore, it is preferred to operate the QAGC circuit in this condition to ensure that the voltage balancing mechanism is still effective as intended. The next section provides the circuit design criteria to achieve a successful switching operation as discussed in this section.

III. Design Considerations

A. Circuit Parameter Calculations

Firstly, it is recommended to add a shunt resistor to the lowermost power device to ensure that it has the highest leakage current so that the upper device can react to balance the leakage current as mentioned earlier. Its value should be selected such that its current is at least equal to the maximum specified leakage current of the devices.

Then, there are four parameters of the QAGC circuit (R_{gate}, R_g, C_s and R_s) whose values must be chosen properly to ensure that the top device can be turned on properly and the DC bus voltage distributes between the coupled devices evenly during turn off. A good starting point is to establish the steady state voltage sharing of the power devices. From (6), we obtain the following relationship that yields an equal voltage sharing in steady state.

$$V_{Cs1} - V_{Cs2} = 30 + 2V_{th} \tag{8}$$

As a result, we can select the values of static balancing resistors R_{s1} and R_{s2} to form a voltage divider that satisfies (8). It is noted that a voltage difference between the balancing capacitors provides twofold benefits: firstly, it forces an equal static voltage sharing of the power devices and, secondly, it assists the switching-on operation of the upper device. Current flowing in the resistors should not exceed 5 times the device leakage current to limit resistive loss. Considering the fact that most active control techniques still requires a resistor in parallel with the power device for static voltage sharing, resistive loss associated with the QAGC circuit is just comparable to the other methods.

The capacitor values can be calculated based on the turn-on gate charge criteria. The following equation shows the required gate charge during the active region ($Q_{g,active}$) of the upper device.

$$Q_{g,active} = C_{s1}\Delta V_{Cs1} - C_{s2}\Delta V_{Cs2} \tag{9}$$

If we assume that at the end of the active region V_{Cs1} and V_{Cs2} are equal to $V_{ce,sat}$ of the power devices, then it is reasonable to approximate ΔV_{Cs1} and ΔV_{Cs2} from the static voltages as shown in Fig. 6(a). Given that C_{s1} and C_{s2} are equal, then the minimum value for C_s1 and C_{s2} for a successful turn-on operation can be calculated from the following.

$$C_{s,min} = \frac{Q_{g,active}}{\Delta V_{Cs}} \tag{10}$$

where ΔV_{Cs} equals to $V_{Cs1} - V_{Cs2}$. It is important to allow enough ΔV_{Cs} at the beginning otherwise V_{Cs2} will end up at high voltage level which is much higher than the device saturation voltage (see Fig. 6(b)).

If the value obtained from (10) is too high, the overall energy consumed from the gate driver will be inefficiently utilised as most of the energy is used for charging the balancing capacitors while only a fraction is used for charging the gate capacitance. For example, if ΔV_{Cs} is fixed to $0.1V_{Cs1}$, total charge requirement from the main gate driver ($Q_{GDU,total}$) is:

$$\begin{aligned} Q_{GDU,total} &= Q_g + C_{s1}V_{Cs1}. \\ &= 11Q_g. \end{aligned} \tag{11}$$

When compare with the total gate charge required for 2 power devices $2Q_g$, the QAGC gate driver has to supply 5.5 times more charge than the standard circuit. Therefore, we come up with another possible scheme to allow a smaller value of C_s to be used; hence, more efficient charge utilization. From (9), if we match dV_{Cs1}/dt and dV_{Cs2}/dt, the relationship becomes the following:

$$C_{s1} - C_{s2} = \frac{Q_{g,active}}{V_{Cs2}}. \tag{12}$$

Then, we can choose any values of C_{s1} as long as we keep the difference as in (12). The consequent advantage of this scheme is that extra gate charge is gained from ΔV_{Cs} at the end of dV/dt. This scheme is suitable for a high-power semiconductor device that requires large amount of gate charge.

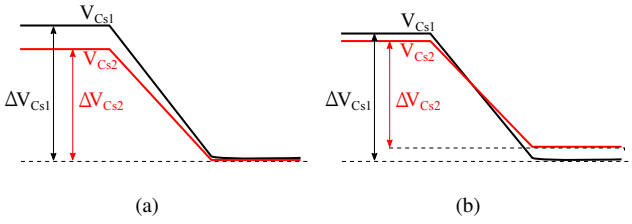


Fig. 6. Capacitors voltages during turn on (a) enough voltage difference (b) not enough voltage difference

Once C_{s1} is established, the values of R_{gate} and R_g can be selected according to the switching speed requirement in (3) and (4). The resistors R_{gate} and R_g should be small for a fast switching but R_g should be big enough for damping local loop oscillations as will be discussed in section III-B.

The other design consideration is a standard gate driver current rating. It should be sufficient to supply the peak current requirement which has to take into account the capacitor charging and discharging current $C_{s1}\frac{dV_{Cs1}}{dt}$.

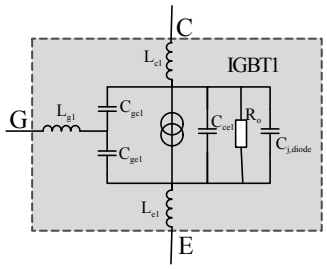


Fig. 7. Small signal model of the IGBT showing the parasitic elements

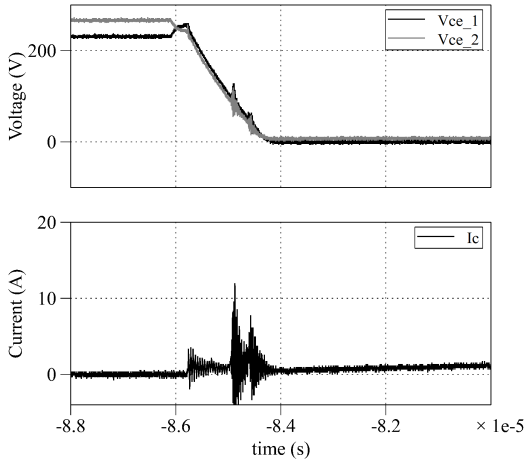


Fig. 8. Switching-on waveforms of the QAGC circuit at zero current load and Vdc of 500 V [17]

B. Influence of Circuit Parameters on Stability

The capacitances and parasitic inductances present in the circuit, both inside the power devices (Fig. 7) and in the main circuit path, may resonate and cause oscillation during switching transients. The switching waveforms of the QAGC circuit in Fig. 8 show some oscillations in voltage and current waveforms. Current and voltage oscillations are undesirable as they may cause several issues such as overvoltage transient on the gate, radio frequency noise emission, high switching losses, and could even lead to uncontrolled oscillation and destruction of one or more power devices [16].

From the analysis presented in [17], there are three groups of resonant frequencies which can be identified as the followings.

- For the low frequency mode, the balancing capacitors resonate with the busbar parasitics in the current return path. The oscillation cannot be damped effectively because of a low resistance path.
- For the medium frequency modes, the oscillation seems to be within the local loop between the power devices and the balancing circuit. The device internal capacitances (C_{ge}, C_{gc}, and C_{ce}) resonate mainly with the device parasitic and PCB track inductances connecting the devices. The gate resistors in the loop should be able to

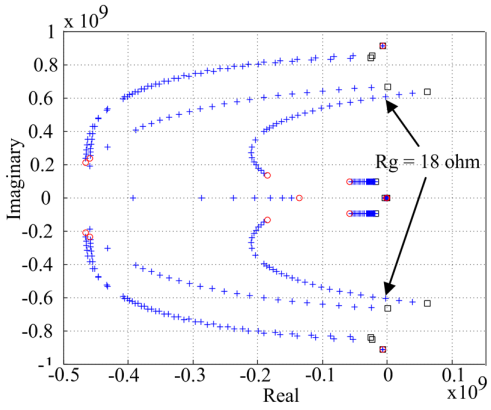


Fig. 9. Root loci when R_g varies from 10 ohms to 50 ohms showing the minimum value of R_g required to keep the complex eigenvalues in the LHS of the s-plane [17]

suppress the oscillations providing their values are big enough. Fig. 9 shows that the unstable eigenvalues of the system occur if R_g is smaller than 18 Ω.

- For the high frequency mode, the oscillation involves the parasitic elements on the load side (bus bar inductances and load parasitic capacitance). Increasing R_{gm} and R_g only gives a slight damping improvement for this mode.

The QAGC circuit parameters must be designed to satisfy not only the switching operation but also stability criteria. Commutation loop inductances should be minimised in order to reduce the oscillation modes that cannot be damped effectively by the gate resistors of the QAGC circuit.

IV. Scalability Issues

This section discusses scalability issues of the QAGC circuit. There are two main concerns about the performance of the circuit when apply to an extension number of the power devices in the series string: how to raise and sustain an appropriate level of the upper gate turn-on voltage and how to minimise an unbalanced dynamic sharing voltage. A modification has to be made to the circuit in order to facilitate these concerns. A discussion is given shortly in this section.

A. Gate Voltage Sustainability

One of the main concerns in driving a stack of power devices is how to raise and sustain an appropriate level of the upper gate turn-on voltage. This is essential to achieve a low on-state voltage of the device to reduce power losses especially for a high-power switch. It has been shown in the previous section that the circuit can provide enough turn-on gate charge up until the end of the active region but after that an extra means to supply the charge to the upper device is required to raise and hold the gate voltage in the saturation region. In [13], they use a diode to supply gate charge to the upper device in the same manner as a bootstrap diode. This method seems efficient enough in case of a two-device series connection. However, an achievable gate voltage is limited due to voltage

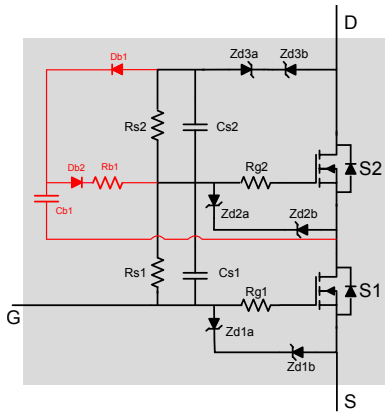


Fig. 10. Modified QAGC circuit

drop in the lower device and in a bootstrap diode; therefore, it may not be suitable for a series stack with a higher number of power devices or a high-power device with a high on-state voltage.

An alternative solution is presented in Fig. 10. The modified QAGC circuit operates in the same manner as the original QAGC except that the boost capacitor C_{b1} is included to store excessive charge during turn-off transients and return back to the gate terminal after turn-on transients. The capacitor C_{b1} is charged to V_{Cs2} during turn off period. It has to store enough charge to supply to the gate capacitance throughout the turn-on period. Its value is much smaller than C_s as its voltage is very high; therefore, this additional capacitor hardly affects the switching speed. The value of C_{b1} can be calculated from the following:

$$C_{b,min} \geqslant \frac{Q_{g,final}}{V_{Cs2}} \tag{13}$$

where $Q_{g,final}$ is the amount of gate charge required to bring the gate voltage to its final value. The resistor R_{b1} serves two functions in this circuit; it limits the speed of discharging C_{b1} (or the speed of charging the gate capacitance) and it is in parallel with R_{s2} to set the effective resistance value for a voltage divider. It should be selected such that the discharging time constant is greater than the longest turn-on period of PWM signals by using the following relationship:

$$R_{b1} \geqslant \frac{\Delta t_{on}}{C_{b1}} \tag{14}$$

where Δt_{on} is the longest pulse width of the PWM signal.

Fig. 11 compares the simulated gate turn-on voltages of the upper device driven by the original and the modified QAGC circuit. The gate voltage with the assistance from the modified circuit rises to 15 V and holds its voltage there even for a long period (1 ms) while the gate voltage from the original circuit increases by 0.5 V only. We can see that a higher gate voltage is achieved with the modified circuit.

The overall gate energy consumed from the main gate driver of the modified circuit is equivalent to the original one as it uses energy from the load current to charge C_{b1}.

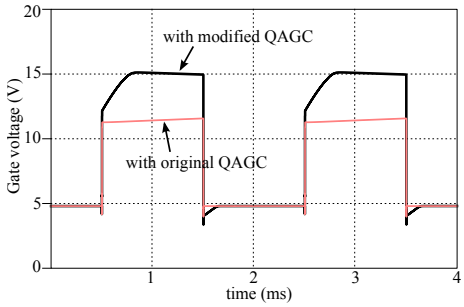


Fig. 11. Simulated gate voltages of the upper device with and without the modified circuit

B. Extension of a Series String

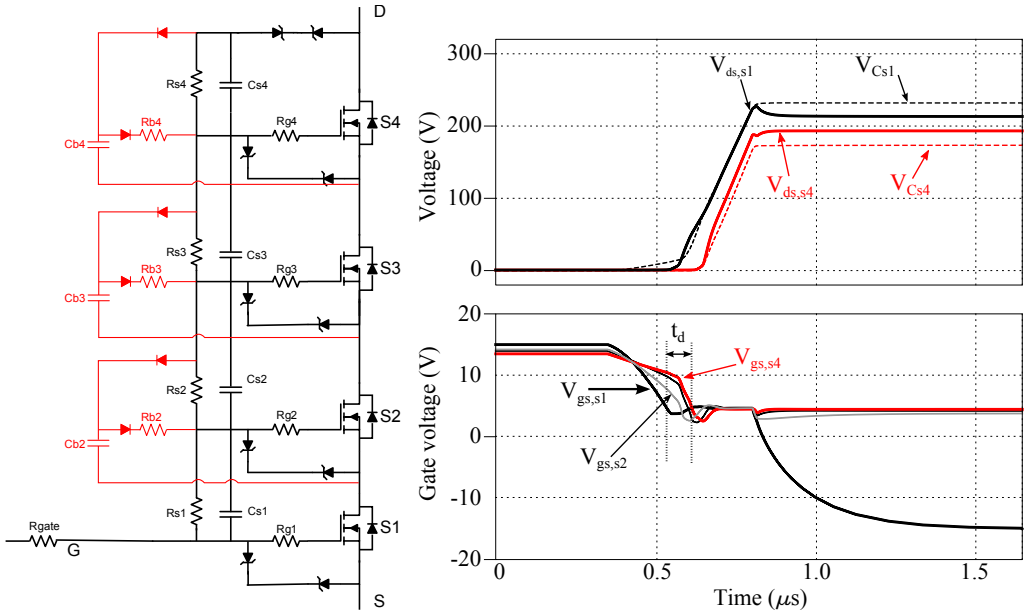
The modified QAGC circuit can be extended for driving an N series-connected power devices as shown in Fig. 12(a) which demonstrates a switch composed of 4 devices in series connection. The circuit arrangement was simulated using SPICE software to validate its operation. MOSFET was chosen over IGBT in this simulation because a MOSFET SPICE model yields a faster, more robust and accurate switching results than the available IGBT model and it has been shown in [13] that MOSFET and IGBT under the QAGC control exhibited the similar switching behaviour. The MOSFET model used in the simulation is IRFP90N20D which requires about 200 nC of gate charge during turn on. The waveforms in Fig. 12(b) show a successful switching operation of the switch. The gate voltages of all devices during turn on are comparable. The additional circuits are able to increase the upper gate voltages close to 15 V. Dynamic voltage sharing between the bottom and the top MOSFETs is well controlled as the maximum mismatched voltage is less than 50 V. We can also notice that the device voltage transients are well contained within the envelopes of the capacitor voltages indicating a controllable voltage sharing performance.

Nonetheless, these waveforms bring out an important aspect when using the QAGC circuit for an extension series string: consecutive turn-off transients from small delay between the two adjacent devices. This delay time is a result of different discharging time constant between the upper and lower gate capacitances. As the number of devices is increased, the overall delay time between the first and the last switching transients is clearly longer resulting in more unbalanced dynamic voltage distribution among the series stack as indicated by a relationship

$$\Delta V_{Ce,max} \cong \sum_{i=1}^{N} t_{di+1,i} . \frac{dV_{ce,off}}{dt} \tag{15}$$

where $t_{di+1,i}$ is a delay between the two adjacent devices and N is the number of power devices in the series string.

Clearly, the delay should be minimum in order to limit the mismatched voltage between the bottom and the top devices. The contours in Fig. 13 shows a calculated delay time as a function of R_g and C_s in the case of a 2-series connected devices. A smaller value of R_{gate} and R_g and a bigger value of C_{s1} can be used to speed up the discharging rate of V_{ge2} to achieve a shorter delay time (within a range of a hundred nanosecond). Comparing to the standard series connection circuit where separate gate drivers are deployed, the delay could be as high as



(a) (b)

Fig. 12. A modified QAGC switch with 4 MOSFETs in series stack (a) schematic (b) turn-off transients from SPICE simulation

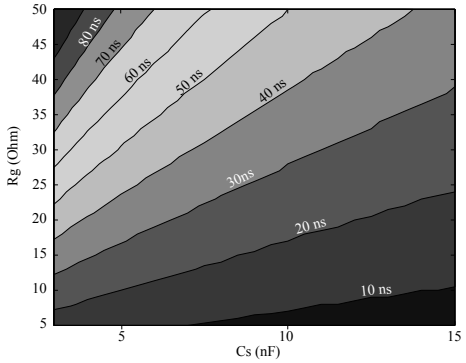


Fig. 13. Contour of delay time as a function of C_s and R_g in case of 2-MOSFET switch ($R_{gate} = 1\Omega$)

480 ns which would cause voltage unbalance of 80% of nominal voltage without any gate delay adjustment [18].

V. Experimental Results

An inductively loaded half bridge circuit as shown in Fig. 14 was constructed and tested using the double-pulse approach. The experiment was carried on to validate the switching operation of the IGBTs under the control of the QAGC circuit. The following section explains the test setup procedure and the experimental results obtained.

A. Test Setup Description

Fig. 14 shows a schematic of the circuit built for the experiment. Two IGBTs are connected in series to form a single switch in both the low side and high side of the half bridge. The choice of the component values used is listed

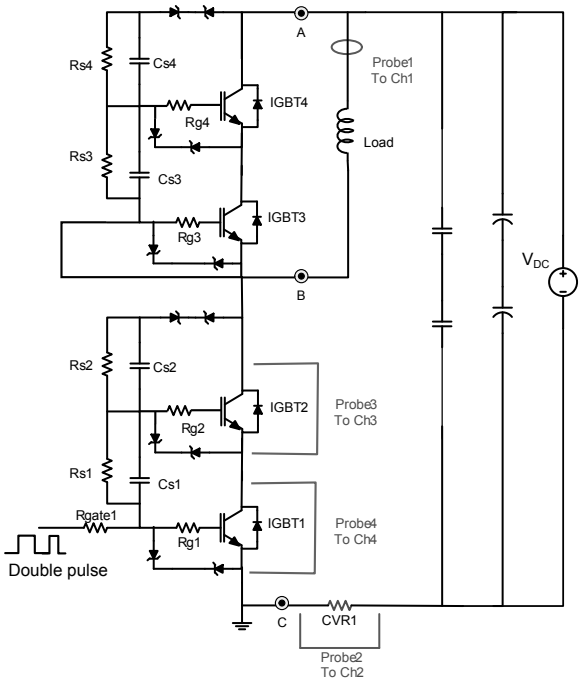


Fig. 14. Experiment setup for a double-pulse switching test

in Table I. The resistors $R_{g1} - R_{g4}$ are high enough to suppress the oscillation in the gate driver loops. The voltage divider network (R_{s1}, R_{s3}) and R_{s2}, R_{s4}) was selected to create ΔV_{Cs} of 30 V. As the test was conducted at low voltage and the device leakage current is very small (several ten μA), effect of leakage current on ΔV_{Cs} would be rather insignificant. Therefore, we could use high values of balancing resistors in order to limit the dissipated losses and a recommended shunt resistor to the bottom IGBT could also be omitted. Then $C_{s1} - C_{s4}$ were calculated from (10) to satisfy the maximum gate charge requirement of the devices (150 nC).

The low side switch was switched twice using a double pulse test method. The first pulse was applied to increase the load current to the desired value. After some delay, the second pulse was applied to capture the current and voltage transient waveforms at turn-on and turn-off. The gate terminal of the high-side switch was connected to the emitter of IGBT3 to turn off the switch during test. The DC link capacitors were charged up to 600 V. The switching characteristics of the switches were measured and recorded using a Tektronix DPO7104 oscilloscope.

B. Measured Results

The operation of the QAGC circuit was validated from the results of the double-pulse switching test at 600 V as shown in Fig. 15. It can be seen that the proposed gate driver is able to turn on and turn off the series string of IGBTs successfully. Voltages across the two IGBTs in the lower switch (V_{ce1} and V_{ce2}) are well balanced during both static and dynamic period such that only a slight voltage difference is presented. This difference at steady state is less than 15 V. It is a result of the difference in steady-state gate voltages between IGBT1 and IGBT2 as stated in (6).

TABLE I

INITIAL VALUES FOR CIRCUIT PARAMETERS

Component	Value	Description
IGBT1,2,3,4	IRG4PC40FD	IGBT with anti parallel diode 600V 27A (TO-247AC)
Rgate1	5 Ω	Main gate resistor
Rg1,2,3,4	100 Ω	Device gate resistor
Rs1,3	660 $k\Omega$	Static voltage divider resistor
Rs2,4	600 $k\Omega$	Static voltage divider resistor
Cs1,2,3,4	5.2 nF	Dynamic voltage divider capacitor
CVR1	0.005018 Ω	Current viewing resistor
Load	3.5 mH	Inductive load
Zener diodes	1N4744	15V zener diode

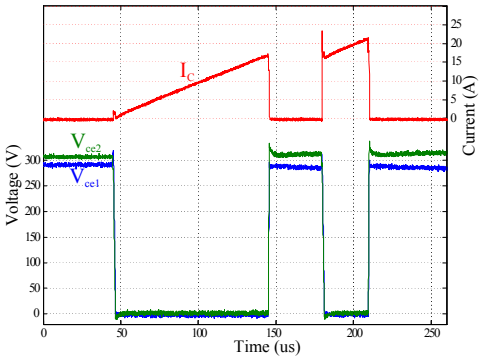


Fig. 15. Measured waveforms of a double-pulse test at V_{dc} = 600 V

The close-up views of the waveforms in Fig. 16 show the transient behaviour of the switch during turn off and turn on. The waveforms agree well with the theoretical operation in section II. Although a delay of 150 ns is present at the beginning of the voltage transient, an interdependent turn off mechanism of the QAGC circuit is able to trim the delay down to less than 80 ns. The voltage rising and falling rate is controlled by the capacitors C_{s1} and C_{s2} effectively so that a very good dynamic voltage sharing for both turn-on and turn-off operations can be obtained and no device suffers from a voltage overshoot.

The effect of tail current to the voltage unbalance that demonstrated in [3], [12], [18] is not present in this experiment even though slight tail current in the switching is also observed. This is because the IGBTs under test are of a low power range. Their tail current variation is quite small such that the trapped charge from mismatch

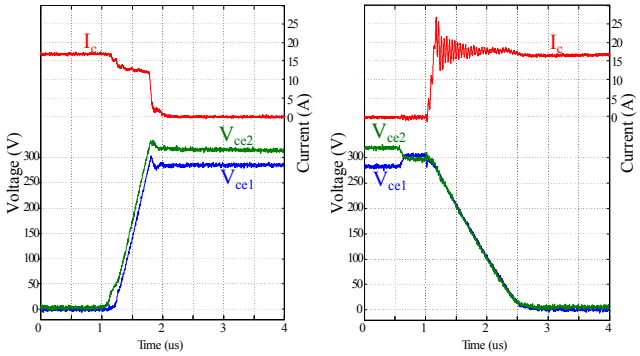


Fig. 16. close-up view of switching waveforms at V_{dc}= 600 V and I_{load}= 17 A (a) during turn off (b) during turn on

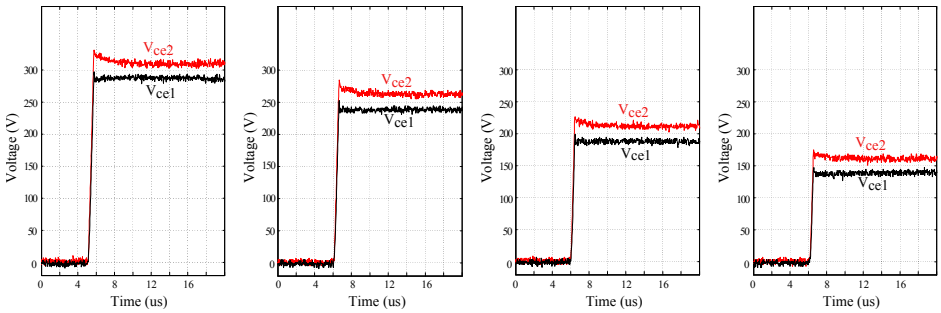


Fig. 17. Measured device voltages when switching off at (a) V_{dc} = 600 V (b) V_{dc} = 500 V (c) V_{dc} = 400 V (d) V_{dc} = 300 V

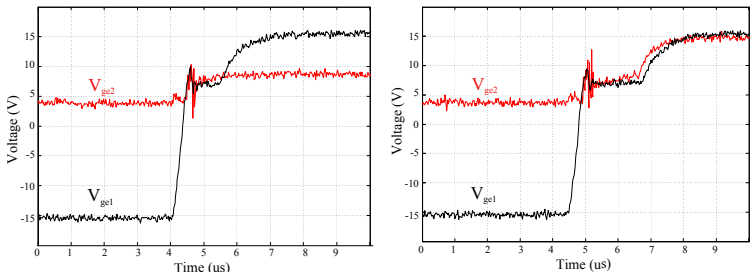
tail current can be distributed through a balancing network in a similar manner to the leakage current.

Fig. 17 compares the voltages across IGBT1 and IGBT2 during turn-off operation at several DC link voltages. It shows that the maximum voltage difference is less than 40 V regardless of what the operating voltage is. This verifies that the circuit is able to provide a balance voltage sharing to the series string.

This suggests that enough gate charge have been transferred to the upper IGBT and confirms that a proper choice of components has been selected. Fig. 18 compares the performance for a range of values of C_s. It shows that the gate voltage will stay at just above the gate plateau voltage if C_s is made too small as in the case of Fig. 18(a) where 2.2 nF capacitors were used. The gate voltage V_{ge2} can rise to nearly 15 V with C_s of 5.2 nF.

VI. Conclusion

This paper has presented a new active gate drive method for driving a series string of IGBTs. It is classified as a gate-side control. The proposed QAGC circuit provides an effective way to drive the power devices and control static and dynamic voltage sharing to the devices at the same time. The experimental results have validated the operation of the circuit. It has been shown that the circuit is able to turn on and off the switch successfully. The driven gate voltage of the upper device during turn on process is comparable to the gate voltage of the lower one.



(a) (b)

Fig. 18. Measured device gate voltages when switching on at I_{load} = 21 A and V_{dc} = 600 V (a) Cs = 2.2nF (b) Cs = 5.2nF

A matched dynamic voltage behaviour is achieved resulting in a well balanced voltage between the devices. Further improvements have been suggested to allow the circuit to be used with an extended number of power devices in the series string. The modified circuit make it possible to implement in high-power semiconductor modules.

The QAGC circuit is attractive in term of simplicity and a small number of component count. Therefore, it is easy to integrate the circuit and the standard gate driver together.

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