Integrated Half-Bridge Switch Using 70-μm-Thin Devices and Hollow Interconnects

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***Abstract*—An application-oriented integration concept for a half-bridge switch assembly has been developed based on the latest generation 70-μm-thin insulated gate bipolar transistorsand diodes, which are rated at 600 V/200 A. This paper addresses the design and reliability of the assembly, with a fully bondwireless approach using cylindrical copper bumps. Advanced numerical structural simulation techniques are also applied to assess the influence of interconnect characteristics (material, size, and shape) and try to determine an optimum solution for reducing the stress and creep strain development in the solder joint. Preliminary experimental tests of the power module are also carried out at different switching frequency and loads to prove the validity of the proposed solution in terms of electromagnetic performance.**

***Index Terms*—Copper bump, flip-chip, power electronics packaging, solder joint, thermomechanical stress.**

I. Introduction

THIS paper addresses the reliable integration of a half-bridge switch (HBS) based on last generation 70-μm-thin 600-V/200-A insulated-gate bipolar transistors (IGBTs) and diodes; in particular, it advances the state of the art as regards a recently presented packaging concept, which targets the optimization from an application point of view [1]. In the application, two transistors with antiparallel diodes need to be connected in series (high-side and low-side switch) to build a half-bridge power switch (HBS) configuration, as extensively required, for instance, by synchronous rectified dc–dc converters and by dc–ac converters (i.e., inverters). During operation within such power converter topologies, load current commutations always take place between high-side transistor and low-side diode (Cell-P) and, vice versa, between low-side transistor and high-side diode (Cell-N). Current commutation between antiparallel transistor–diode pairs only takes place at zero voltage in the case of synchronous rectified dc–dc converters, and at zero current in the case of inverters, and is thus, by definition, noncritical in both cases (i.e., it does not imply power dissipation or potentially destructive voltage overshoots). Therefore, as pointed out in [2] and illustrated in Fig. 1, for improved switching performance, packaging design should aim at integrating and minimizing not the high-side or low-side basic switches, but rather the *positive* and *negative* switching cells, i.e., the high-side transistor/low-side diode and the low-side transistor/high-side diode pairs, respectively (the terminology positive and negative cell is derived from the sign of the load current during inverter operation). Based on these considerations, this paper presents an advanced and application-driven integration approach of a half-bridge power switch. In particular, in trying to optimize the switching and thermal performance of the HBS, the assembly is designed to construct with post (*power bump*) bondwireless sandwich packaging technology, which enables high power density levels, with double-sided cooling and reduced stray inductance. In the preliminary test, bondwires are still used here only for the transistor drive interconnection (i.e., gate and emitter) to use the existing substrate at this stage. However, the power and drive loops are clearly separated, and the driving loops are kept very small.

The use of thin devices in the switch implementation offers not only superior electrical but also thermal performance, as compared with thicker ones, and brings along increased power density figures [3]. Consequently, here, the main focus is on developing interconnect solutions, which can improve the thermomechanical performance of the assembled switch during fabrication and operation, preventing the benefits of thin device technology from being penalized at the packaging level.

II. Switch Assembly

The devices used for the switch assemblies are shown in Fig. 1: $10 \times 9.5 \times 0.07\ \text{mm}^3$ IGBTs and $9.5 \times 5.5 \times 0.07\ \text{mm}^3$ diodes, where the top metallization is treated with NiP/Ag finish being solderable. To achieve optimum performance in the application, packaging needs to target the integration of the positive and negative cells in the HBS (see Fig. 1); this can be achieved by having the devices in the same cell soldered on separate substrates, which are then mounted, one on top of the other, by means of interconnect posts (bumps), as shown in Fig. 2. This results in a low stray inductance and double-sided cooled power switch, where all devices have their backside in direct contact with a cooling surface [1]. Here, both the top and bottom substrates are direct bonded copper (DBC) consisting of a 1-mm-thick aluminum nitride tile sandwiched by 0.3-mm-thick copper on both sides.

The chips are soldered to the DBC substrates with 0.1-mm-thick Sn–3.5Ag solder alloy. The bumps are Cu with an outside

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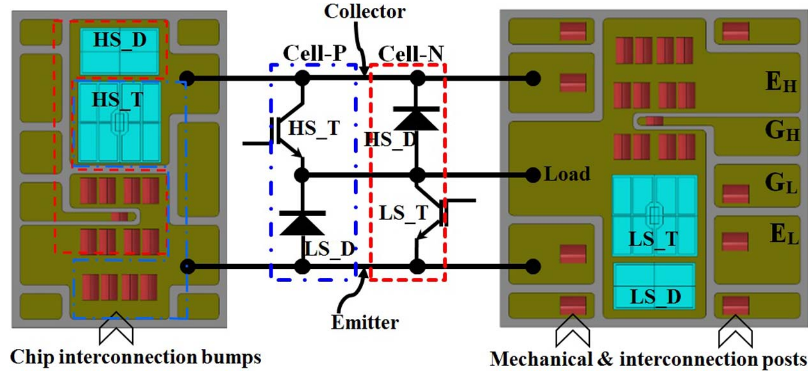

Fig. 1. Schematic of half-bridge power switch and the corresponding structural view.

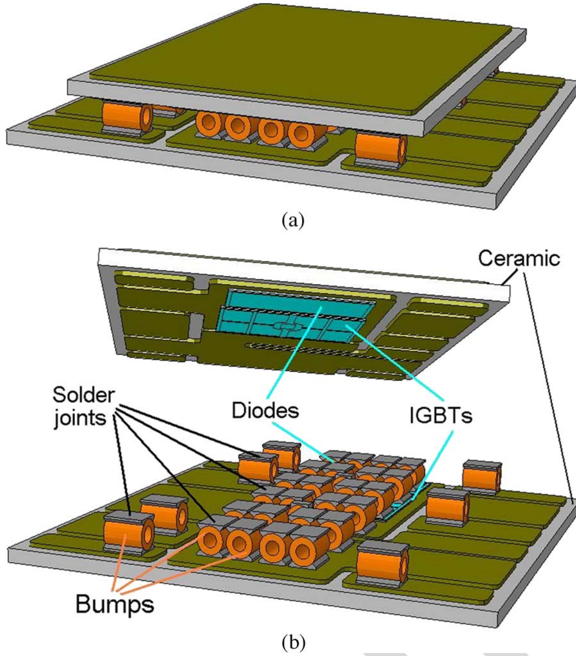

Fig. 2. Stacked assembly of substrate–chip–bump–substrate for the HBS. (a) Overall view. (b) Open view.

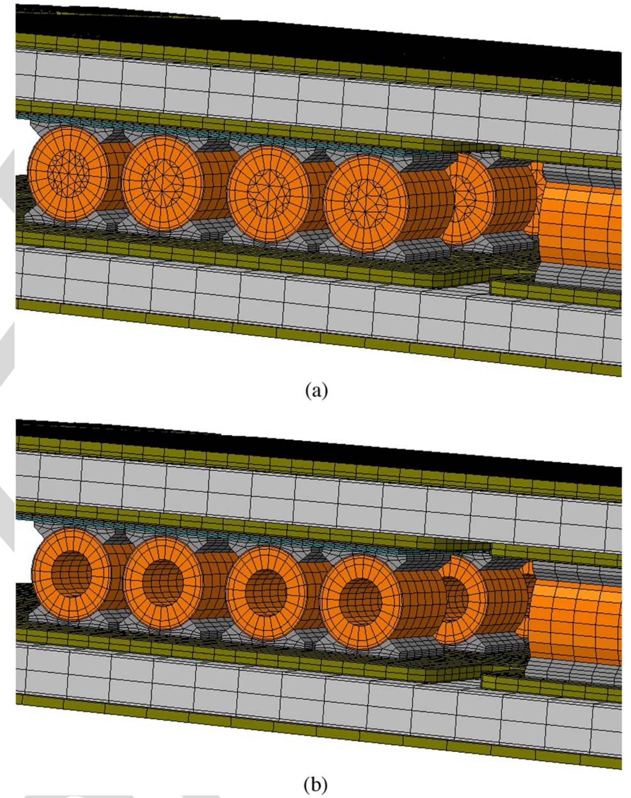

Fig. 3. Meshing systems used to discretize the assemblies with (a) solid bumps and (b) 0.5-mm-thick hollow bumps.

diameter of 2 mm and length of 3 mm. They are soldered to the front sides of the chips with Sn–3.5Ag solder of 0.1–0.4 mm in thickness, following the shape of the bumps. Due to the reduced thickness of the devices in this case, it is important to understand the effects of different interconnection geometries, sizes, materials, and shapes to yield optimum reliability. In particular, we report on a comparison of five hollow cylinder (0.5, 0.375, 0.25, 0.125, and 0.0625 mm in wall thickness) copper bumps with solid ones as the interconnect solution (see Fig. 3).

III. FE Modeling and Simulation

The developed switch model was characterized electromagnetically and electrothermally, employing structural numerical analysis tools [13], and tested for functional performance. Fig. 4(a) shows the 3-D model mesh for the electromagnetic characterization of the assembly, which was performed with FastHenry [14]. As for the model in Fig. 4, it has been assumed that the paths through the chips, solders, and bumps were considered as $5 \times 5 \times 2$ mm^3 copper filament cubes, which carry uniform current and are connected together as a block (i.e., two for diode and four for IGBT). The model also uses a copper conducting material with an electrical conductivity of 59–600–000 S/m. The extraction was taken on a single path, while the unnecessary paths were being excluded, so that they do not contribute to the measuring path. The values of parasitic inductance between all terminal pairs [collector (C), emitter (E), and load (L)] were extracted and provided very encouraging indications. For instance, the estimated parasitic inductance between collector and emitter was less than 7 nH above 10 kHz (see Fig. 4).

The adhesions between the interfaces of the die and solder, and between copper bump and solder, are the most critical surfaces in the whole module because they are prone to failure

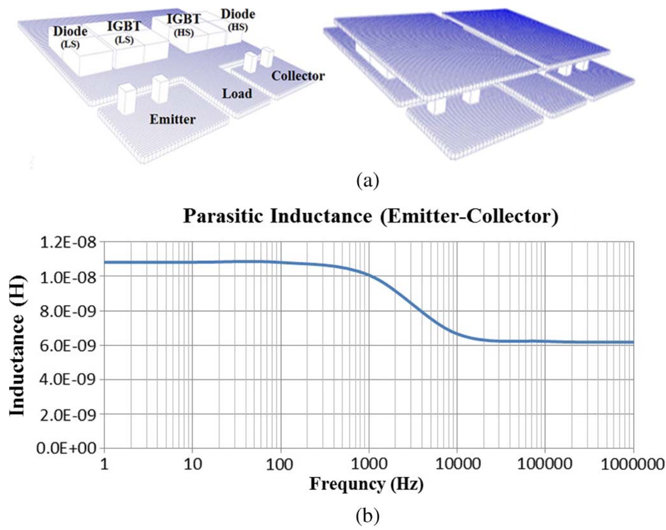

Fig. 4. (a) Three-dimensional model for electromagnetic characterization of the module; (b) extracted parasitic inductance.

119 with thermal cycling [4]. Finite element (FE) thermal and
120 thermomechanical modeling and simulations have been carried
121 out to compare the maximum junction temperature of the
122 chips and the maximum residual stress/creep stain develop-
123 ments in the solder joints in the three assembles constructed
124 using the three different bumps. The modeling and simulation
125 were done using commercial FE analysis software ABAQUS
126 6.10-2 and its graphic user interface Complete Abacus
AQ2 127 Environment. Fig. 3 presents an overview of the meshing
128 systems consisting of 153–134 and 143–690 C3D8 and C3D6
129 linear brick elements and triangular prism elements to discretize
130 the assembly with solid and 0.5-mm-thick hollow cylinder
131 bumps. Here, the largest element is $1 \times 1 \times 0.45$ mm^3, and
132 the smallest element is $0.5 \times 0.25 \times 0.025$ mm^3. In addi-
133 tion, S4 shell elements of 0.5 mm $\times$ 0.5 mm or 0.5 mm
134 $\times$ 0.25 mm, in size, were also used to discretize the NiP
135 (nickel–phosphorus) finish on the surfaces of the substrates
136 and the Al metallization on two sides of the chips and in-
137 cluded in the thermomechanical modeling and simulation. For
138 both diodes and IGBTs, the top side was treated with a gal-
139 vanic process consisting of a 3.2 μm/500 nm/300 nm-thick
140 AlSiCu/NiP/Pd solderable metallization, and the back side
141 consists of a 1 μm/300 nm/300 nm-thick AlTi/Ni/Ag metal-
142 lization. However, in the present model, they were assumed
143 as a layer of 3.2-μm-thick Al on the top side and a layer of
144 1-μm-thick Al on the back side of the chips. This is based on the
145 fact that most of the NiP/Pd and Ni/Ag layers would react with
146 the liquid Sn–3.5Ag solder to form intermetallic compounds
147 (IMCs) embedded within the matrix of the solder during the
148 reflow process, and such IMCs were neglected.

149 As shown in Fig. 5, the assembly was first subjected to
150 a predefined temperature profile to simulate the stress and
151 strain development during the reflow process. In this stage, all
152 the solder joints were deactivated, and thus, strain/stress did
153 not develop in them until solidification of the molten solder
154 occurred. Then, power losses of the IGBTs and diodes (see
155 Fig. 6) were taken as heating sources to simulate the thermal
156 performance of the assembly during a realistic mission pro-

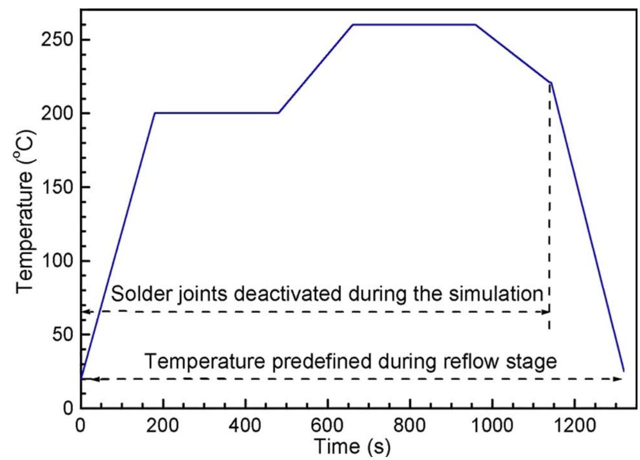

Fig. 5. Temperature profile representative of the reflow process.

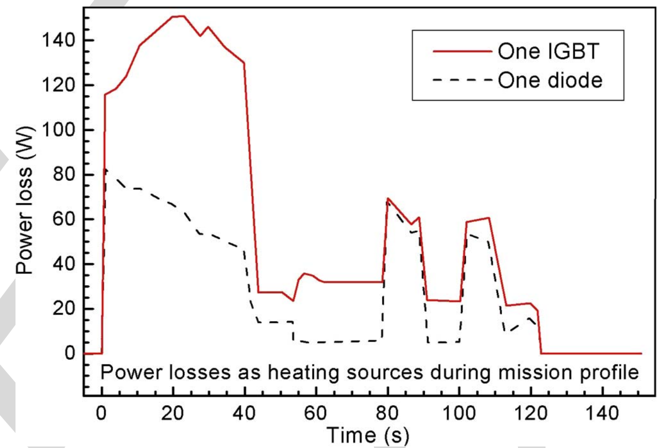

Fig. 6. Power losses of one IGBT and one diode during a mission profile derived from a real system operation.

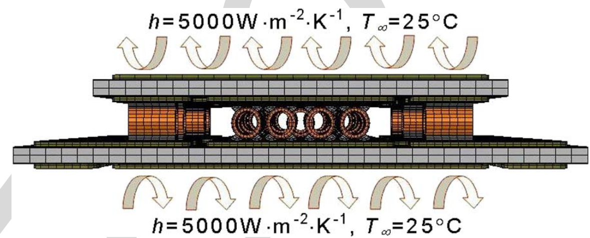

Fig. 7. Boundary condition of heat exchange applied in the thermal simulation during the mission profile.

file, and the heat exchange boundary condition, as described 157
in Fig. 7, was applied to both the top and bottom cooling 158
surfaces of the assembly. The heat exchange coefficient of 159
$5000\ \mathrm{W} \cdot \mathrm{m}^{-2} \cdot \mathrm{K}^{-1}$ is a typical value for using a forced- 160
convection cooling in power electronics. The temperature field 161
obtained from the thermal simulation was used as inputs to sim- 162
ulate the further development of stress/strain in the assembly 163
during the mission profile. 164

The thermal and mechanical properties of the Si, AlN ce- 165
ramic tile, and NiP finish on the substrates for the thermal and 166
thermomechanical simulations are listed in Table I [4]–[6]. For 167
the rest of the materials in the assembly, Chaboche's plastic 168
model was used to describe the mechanical properties of the 169

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TABLE I
THERMAL AND MECHANICAL PROPERTIES OF Si, AlN CERAMIC LE, AND NiP FINISH

	Si	AlN	NiP
λ (W/(K·m))	146	175	…
C (J/(kg·°C)	750	740	…
ρ (kg/cm^3)	2.33	3.30	…
CTE (10^{-6}/K)	2.5	4.6	16.4
E (GPa)	130	331	60
ν	0.22	0.22	0.3

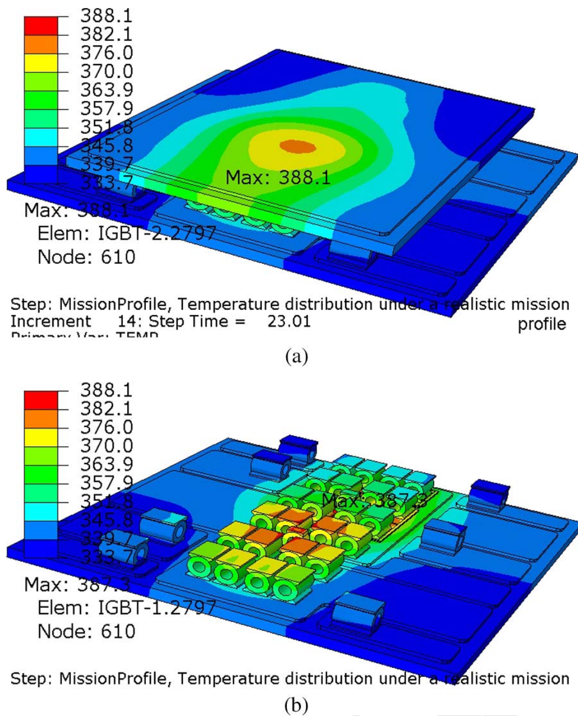

Fig. 8. Simulated results of temperature distribution in the assembly for 0.5-mm-thick hollow bumps: (a) whole assembly and (b) assembly with the top substrate removed.

Cu and Al, and Anand's creep model was used to describe the mechanical properties of the Sn–3.5Ag solder alloy. All the mechanical and thermal properties for the Cu, Al, and Sn–3.5Ag were taken from [5] and [6] and are not repeated here.

The simulation cases of the three assemblies with the three different bumps were executed on a PC computer with an Intel Pentium Core i7 CPU 976 at 3.20-GHz processor and 8-GB RAM. The running times were about 50 h, for all the cases, to simulate the thermomechanical residual stress/strain developments in the assemblies after the reflow process followed by six cycles of the mission profile.

From the simulation results, the highest junction temperature was observed on the IGBT attached on the top substrate and at 23.01 s during the mission profile. Figs. 8 and 9 present the simulated results of temperature distribution in the assembly constructed with the 0.5-mm-thick hollow bumps at 23.01 s during a realistic mission profile, where the bottom chips and substrate of the assembly are separated for observing the hottest IGBT in Fig. 8. Such a result is readily understood because the power loss by an IGBT was higher than a diode, and

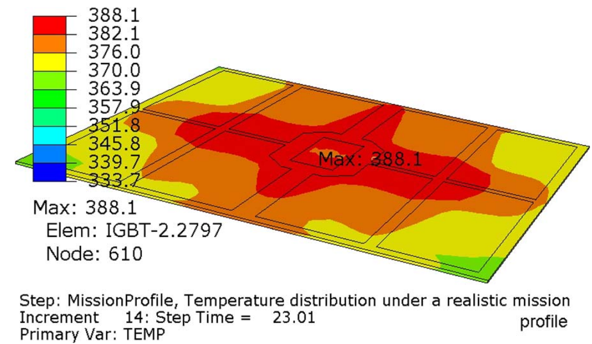

Fig. 9. Simulated temperature distributions in the hottest IGBT of the assembly during the mission profile for 0.5-mm-thick hollow bumps.

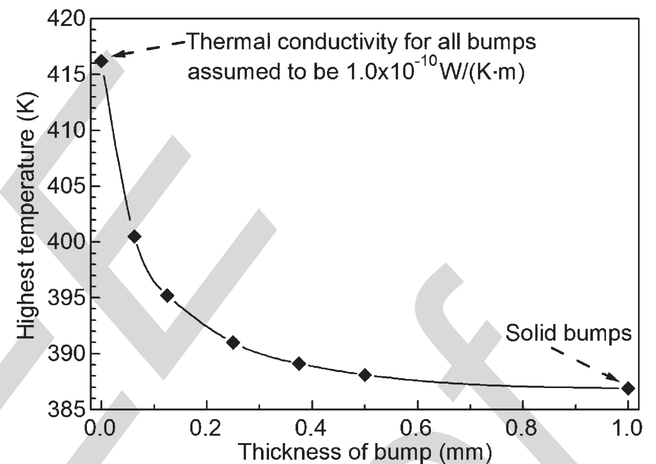

Fig. 10. Dependence of the simulated highest temperature in the assembly on the wall thickness of the bumps.

the cooling surface of the top substrate was slightly smaller than the bottom substrate. The simulated results of temperature distribution in the assembly constructed with the other five types of bumps were similar, but the highest temperature in the hottest IGBT depended on the wall thickness of the bumps (see Fig. 10). The highest temperatures in the assembly constructed with the six types of bumps increased with decreasing the wall thickness of the bumps, and were 16.2 °C–29.3 °C lower than the highest temperature in the assembly where the bumps were assumed to have an extremely low thermal conductivity of 1.0×10^{-10} W/(K · m). In all the six cases with real bumps, the highest temperature location is at the center of the IGBT. In the case where the bumps were assumed to have extremely low thermal conductivity, the highest temperature location is still at the same IGBT, but has been moved to one side (see Fig. 11).

During both reflow process and switch performance over six cycles of the realistic mission profile, the FE thermomechanical simulation results indicate that one of the solder joints between the bumps and the chips has the highest thermomechanical stress and creep strain accumulation among all the solder joints. The maximum von Mises stress and creep strain accumulations are at the corners of the solder layer in contact with the emitter metallization of the IGBT, which are the most critical areas of failure. Such a result can be attributed to the mismatch of thermal expansion between the Sn–3.5Ag solder and the

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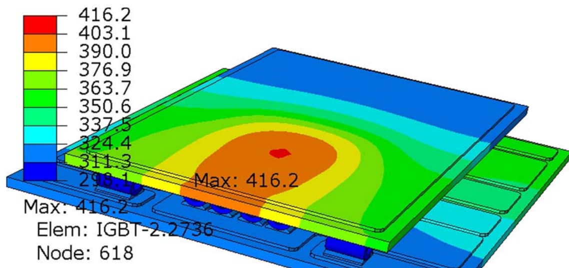
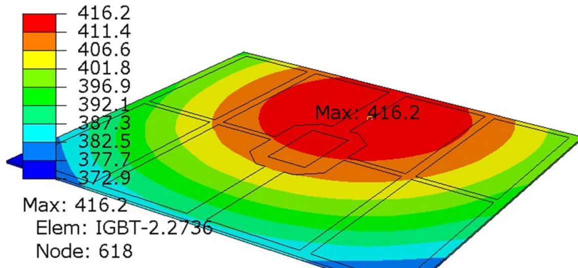


(a)



(b)

Fig. 11. Simulated results of temperature distribution in the assembly for the bumps assumed to have an extremely low thermal conductivity of 1.0×10^{-10} W/(K · m): (a) whole assembly and (b) the hottest IGBT.

Fig. 12. Simulated result of distribution of von Mises stress in the solder joints for the die attachment after a reflow process.

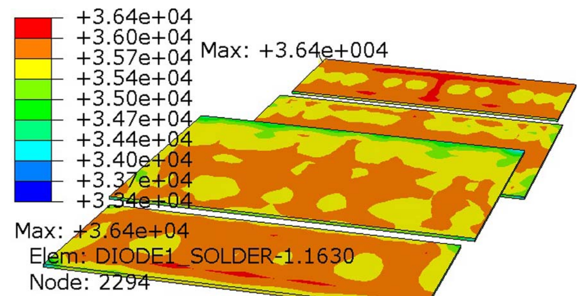


Fig. 13. Simulated distribution of von Mises stress in the solder joints for the die attachment after six cycles of the mission profile.

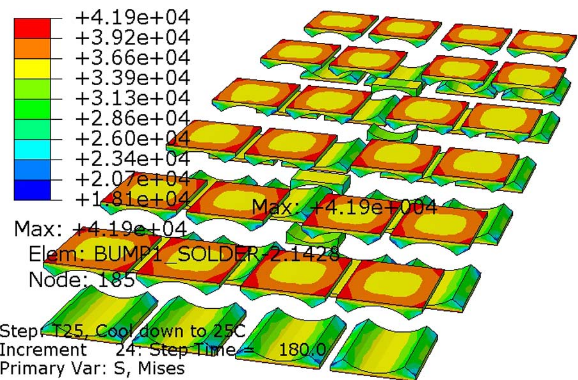


Fig. 14. Simulated distribution of von Mises stress in the solder joints for bump interconnects after the reflow process.

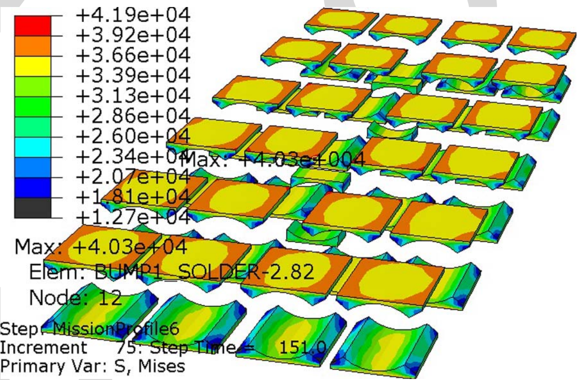


Fig. 15. Simulated distribution of von Mises stress in the solder joints for bump interconnects after six cycles of the mission profile.

217 Si chips. Furthermore, it is also related to the joining area 218 or the shapes and size of the bumps. This can be seen from 219 the representative simulated results of the assembly with the 220 0.5-mm-thick bumps, as shown in Figs. 12–19. In Figs. 14, 15, 221 18, and 19, the first and last rows of four bump solders are for 222 the two diodes, and the center four rows of bump solders are for 223 the two IGBTs.

224 Figs. 20–23 compare the simulated maximum residual von 225 Mises stress and creep strain accumulation in the solder joints 226 for the die attachment and bump interconnects between the 227 assemblies with the six different bumps. In comparison with the 228 solid bumps, the hollow bumps can reduce the residual stress 229 in the as-reflowed solder joint both for the die attachment and 230 for the bump interconnects (see Figs. 20 and 21). It is noted 231 that the maximum residual stresses in the solder joints for the bump interconnects decrease with decreasing the wall thickness 232 of the bumps. This is readily understood because bumps with 233 thinner walls can be the bumps to be more compliant. As a 234 result, the more compliant bumps can withstand more elastic 235 deformation, and the solder joints and Si dice need relatively 236 low stress development against the mismatch coefficients of 237 thermal expansion and the different deformations. However, the 238 maximum residual von Mises stress in the solder joints for the 239 die attachment in the assembly with the 0.5-mm-thick bumps is 240 slightly lower than those in the assemblies with the other hollow 241 bumps. This may be attributed to the nonlinear stress–strain 242 relationship for the creep of the solder alloy. This is because 243

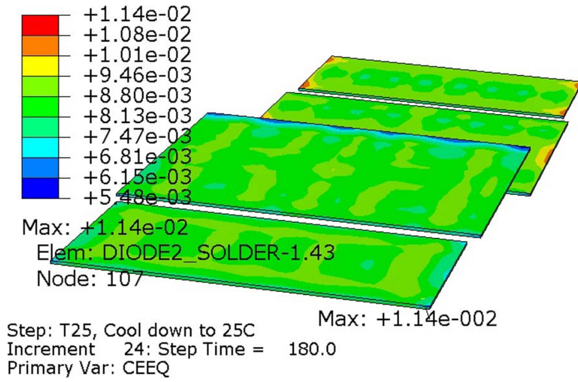


Fig. 16. Simulated distribution of creep strain accumulation in the solder joints for the die attachment after the reflow process.

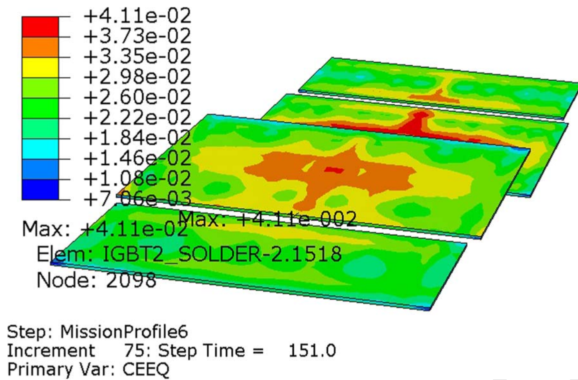


Fig. 17. Simulated distribution of creep strain accumulation in the solder joints for the die attachment after six cycles of the mission profile.

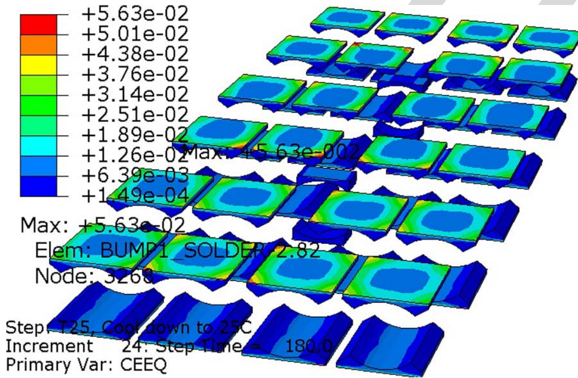


Fig. 18. Simulated distribution of creep strain accumulation in the solder joints for bump interconnects after the reflow process.

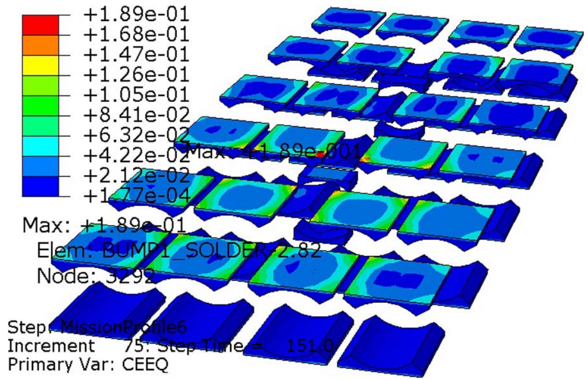


Fig. 19. Simulated distribution of creep strain accumulation in the solder joints for bump interconnects after six cycles of the mission profile.

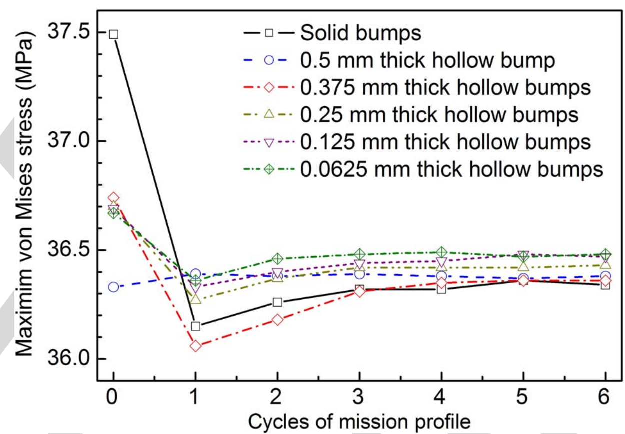


Fig. 20. Evolution of the simulated maximum residual von Mises stress in the solder joints for the die attachment, with respect to cycles of the mission profile.

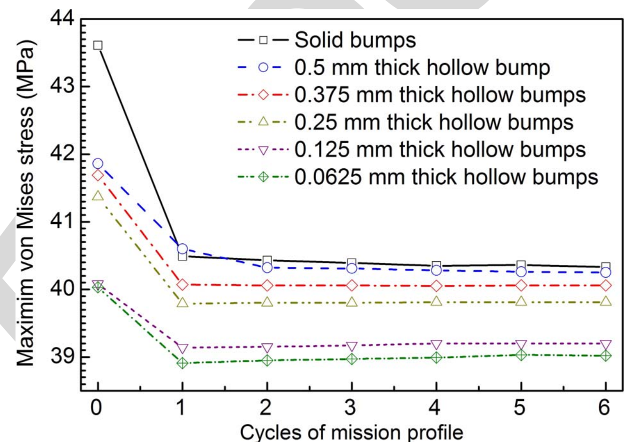


Fig. 21. Evolution of the simulated maximum residual von Mises stress in the solder joints for bump interconnects, with respect to cycles of the mission profile.

a higher stress may lead to a higher creep deformation, while a higher creep deformation may result in a larger stress release. During the cooling stage of the reflow, the solder joints for the die attachment in the assembly with the 0.5-mm-thick bumps were probably experienced with relatively large stress release. Therefore, the maximum residual von Mises stress in the solder joints for the bump interconnects still decrease.

After some stress release during the first cycle of the mission profile, the maximum residual von Mises stress in the solder joints for the die attachment is almost the same for the six different bumps. The stress release in the assembly with the 0.5-mm-thick bumps is negligible, and the stress release in the assembly with the solid bumps is the largest. After the stress release during the first cycle of the mission profile, the maximum residual von Mises stress in the solder joints for the bump interconnects still decrease with decreasing the wall thickness of the bumps. Again, this can be explained with the increased compliance with decreasing the wall thickness of the bumps. Indeed, the difference of the maximum residual von

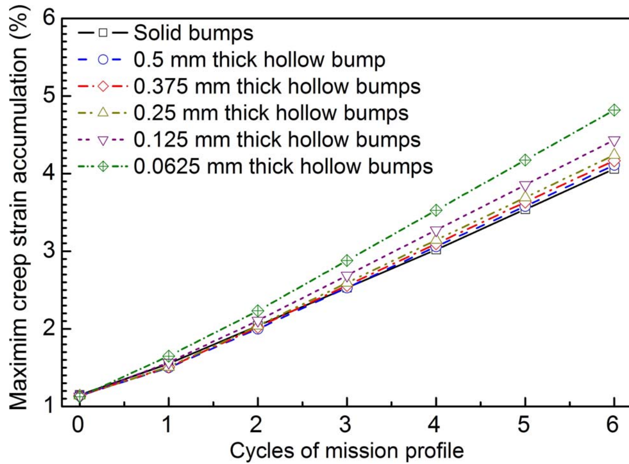


Fig. 22. Evolution of the simulated maximum creep strain accumulation in the solder joints for the die attachment, with respect to cycles of the mission profile.

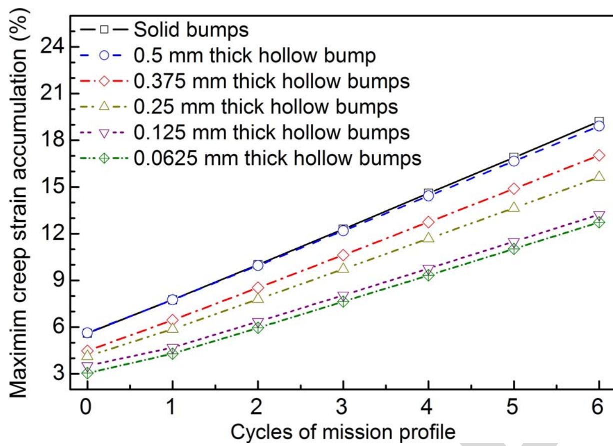


Fig. 23. Evolution of the simulated maximum creep strain accumulation in the solder joins for bump interconnects, with respect to cycles of the mission profile.

263 Mises stress in the solder joints in the assemblies with the 264 different bumps is quite low. This is due to the fact that there 265 was stress saturation during the creep deformation.

266 In response to the stress release during the first cycle of the 267 mission profile (see Figs. 20 and 21), the maximum creep strain 268 accumulations in the solder joints for both the die attachment 269 and the bump interconnects over this cycle are somewhat lower 270 than those over the other five cycles of the mission profile, 271 which are almost constants (see Figs. 22 and 23). Among 272 the six assemblies with the six different bumps, the overall 273 maximum creep strain accumulations in the solder joints for 274 the die attachment, with respect to cycles of the mission profile, 275 slightly increase with a decrease in the wall thickness of the 276 bumps. This can be attributed to the fact that the solder joints 277 in the assembly with thinner hollow bumps were subjected to 278 higher temperatures (see Figs. 8 and 10), and the solder alloy 279 has lower creep resistance at higher temperatures. However, 280 the maximum creep strain accumulation in the solder joints 281 for the bump interconnects clearly decrease with a decrease 282 in the wall thickness of the bumps. The 0.5-mm-thick bumps 283 can slightly reduce, and the 0.0625-mm-thick bumps can sig-

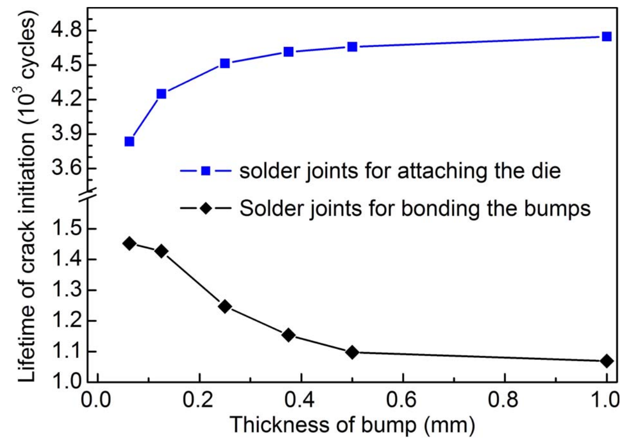


Fig. 24. Lifetimes predicted from the simulated maximum creep strain accumulation per cycle for the initiation of fatigue cracks in the solder joints.

nificantly reduce the maximum creep strain accumulation in 284 the solder joints for the bump interconnects when compared to 285 that for the solid bumps. Such a result reveals that the increase 286 in the compliance of the bumps through reduction in the wall 287 thickness is more effective than reducing the temperatures 288 through an increase in the wall thickness to reduce the creep 289 strain accumulation in the solder joints. 290

From the point of view of structural reliability, the reliability 291 of the solder joints can be assessed with the creep strain range, 292 accumulation, and energy density [5], [8], [9]. In the present 293 work, we employ the lifetime model of the SnAgCu solder 294 joints based on the creep strain accumulation [9], as follows: 295

$$N_f = \frac{1}{0.0405\Delta\varepsilon_{\mathrm{cr}}} \quad (1)$$

where N_f is the lifetime in number of cycles, and $\Delta\varepsilon_{\mathrm{cr}}$ is 296 the creep strain accumulation per cycle. This is because the 297 eutectic Sn–3.5Ag solder alloy used to join the present Cu 298 bumps should be saturated with Cu during the reflow process. 299 Applying (1) to the maximum creep strain accumulations per 300 cycle, which were calculated in Figs. 22 and 23, the predicted 301 lifetimes are presented in Fig. 24. It can be seen that thinner 302 bumps can effectively improve the reliability of the assembly. 303 The maximum creep strain accumulations per cycle in all the 304 solder joints have been used, and thus, the predicted lifetimes 305 are better considered as the cycles of the mission profile, at 306 which fatigue cracks are initiated in the solder joints. They 307 can be used to compare the different bumps and optimize the 308 design. The lifetimes corresponding to the complete failure of 309 the solder joints should be longer than these predictions. 310

It is difficult to manufacture the hollow bumps with a wall 311 thickness thinner than 0.0625 mm. Based on the aforemen- 312 tioned simulation results, the 0.0625- and 0.125-mm-thick hol- 313 low bumps lead to an increase of 8.3 °C and 13.6 °C for the 314 highest temperature in the hottest IGBT, but ∼35% longer for 315 the lifetime of the solder joints for the bump interconnects than 316 the solid bumps. Therefore, it is reasonable to select a wall 317 thickness of the bumps between 0.0625 and 0.125 mm. 318

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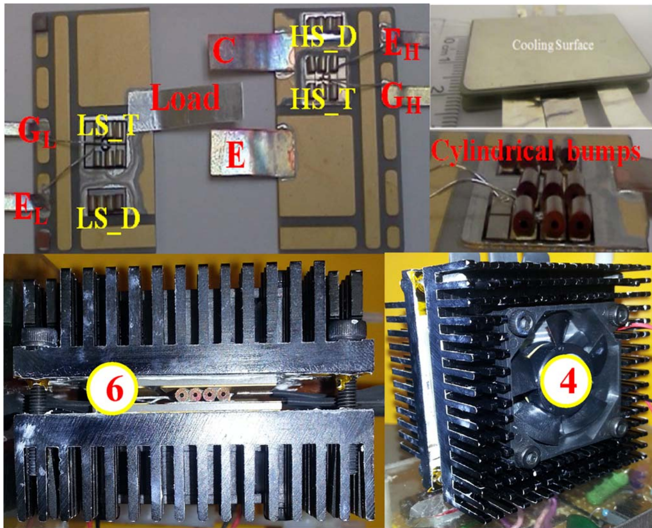

Fig. 25. Structure of half-bridge prototype (HBS).

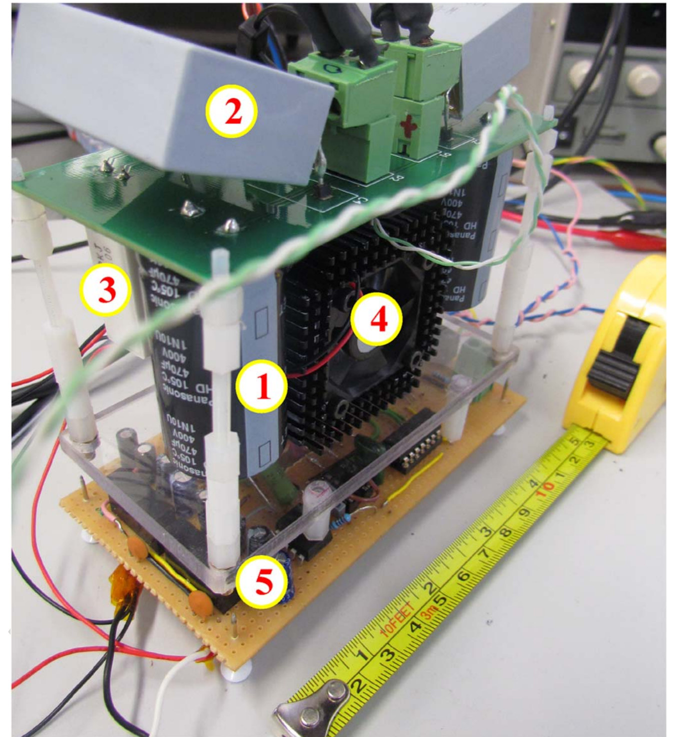

Fig. 26. Half-bridge power module.

IV. Switch Prototype and Preliminary Functional Testing

An initial prototype was constructed with the AlN-based substrate available in our laboratory. First the transistor and diode chips are soldered underside (collector and cathode) onto a DBC substrate with a 100-μm-thick Sn–3.5Ag preform that is employed in a fluxless reflow soldering process at a peak temperature of 260 °C for 5 min. Ultrasonically bonded 375-μm-thick aluminum wires are used to create the gate and emitter interconnections needed to drive the IGBT. These wires are not power connections but only driving signals. Then, the cylindrical copper bumps are soldered onto the chips using the 62Sn36Pb2Ag solder paste reflowed at a peak temperature of 240 °C for 5 min. Finally, the two substrates shown in Fig. 25 are positioned, one on top of the other, and soldered using the 62Sn36Pd2Ag solder paste at a temperature of 260 °C for 5 min.

The functionality of the prototype was tested in a basic half-bridge dc–ac converter, which can be implemented on typical working conditions of multilevel converters. Fig. 25 shows the structure of the HBS topology, where the top view of the HBS structural halves with the indication of the electrical terminals of HS_D and HS_T, corresponding to the high-side diode and transistor, respectively; LS_D and LS_T relate to the low-side diode and transistor, respectively. E_H, G_H, and E_L, G_L are the high- and low-side emitter and gate terminals, respectively.

Fig. 26 illustrates the fully integrated prototype assembly, containing two heatsinks, fans, dc-link capacitors, and resistors mounted all together, such that the gate drive is connected at the bottom and the dc-link capacitors and resistors to the top part of the power module. This configuration will not only isolate the gate signals to/from the power circuit but also reduce the external loop inductance of the wires connected to the module where the dc-link capacitors and the gate signals are very close to the devices. The test conditions were set, as depicted in Table II. A fixed dead time of 0.9 μs was chosen, and the inverter is tested in an open-loop system. Two identical heatsinks, each embedded with a 12-V fan, were attached to both cooling surfaces of the switch, in order to cool down the module at high power rating while providing space exploitation to the overall size of the power cell.

TABLE II
Design Parameters of the Power Module

Input voltage		400V
Switching frequsncies		10KHz, 15KHz & 20KHz
Dead-Time		900ns
Load resistors		19.2Ω, 28.8Ω & 38.4Ω
Load inductor		5mH
1	C3 and C4	470μF (electrolytic)
2	C1 and C2	4.7μF (Film)
3	R1 and R2	22KΩ
4	Heatsink embeded with 12V fan	
5	Gate drive circuit	
6	Device under test (HBS)	

The gate drive circuit and the power side interconnections are kept very close to the power converter, in order to reduce the noise pickup at the gate signals and parasitic inductances. As for the schematic diagram (see Fig. 27), the input is center tapped with dc-link capacitors. This kind of configuration requires a very large capacitor value to decrease the low-frequency voltage oscillation at the capacitor midpoint. Here, both electrolytic and high-frequency capacitors are used to suppress the voltage oscillation at the dc bus. For the gate signal, a basic pulsewidth modulation strategy is used, where the carrier and modulating signals are taken from external signal generators and are properly processed inside the gate drive to provide the required sequence. Both Gate_H and Gate_L drive signals are passed through isolation, deadtime, and current boosting circuitry to prevent shoot through and enable high-frequency operation of the power transistors. The heatsink was equipped

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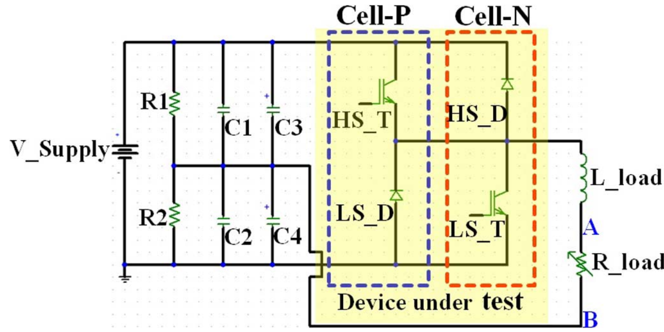


Fig. 27. Schematic of HBS test-circuit.

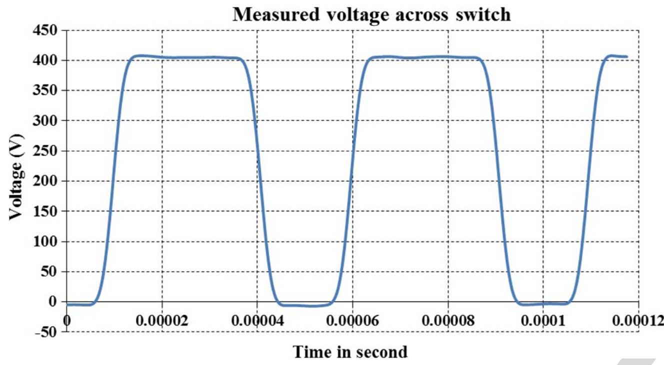


Fig. 28. Experimental result: collector–emitter voltage.

with a thermocouple on the device side closer to the IGBT, so that the average heatsink and device temperature can be estimated.

Two LeCroy differential probes were placed across the high-side transistor and the load resistor of 19.2 Ω, and the corresponding results were then observed using a LeCroy oscilloscope. The representative experimental result shown in Fig. 28 is the voltage across the switch (Vce), and the experimental result in Fig. 29 is the voltage across the load resistor (V_AB) and output current.

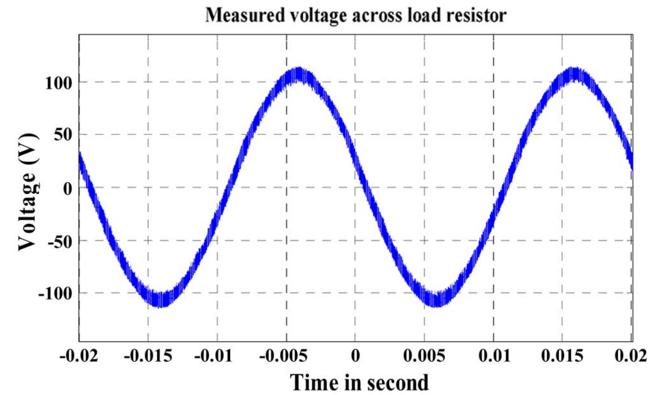
The test results shown in Figs. 28 and 29 were taken, and an average steady-state temperature of 70 °C was recorded, while the switch was operating at 400-V input voltage, 12-V fan voltage, and 20-kHz switching frequency. These results confirm the perfect functionality of the switch and, more importantly, reveal a very contained value of parasitic inductance, as shown in the graph depicted in Fig. 28. As for the result, it is clear that there is an absence of voltage overshoot across the switch during current commutation. In addition, the result also agrees with the reduced stray inductance extracted by the electromagnetic simulation.

The graph shown in Fig. 30 is the calculated efficiency of the converter, using the supply input and experimental results at three different frequencies, as follows:

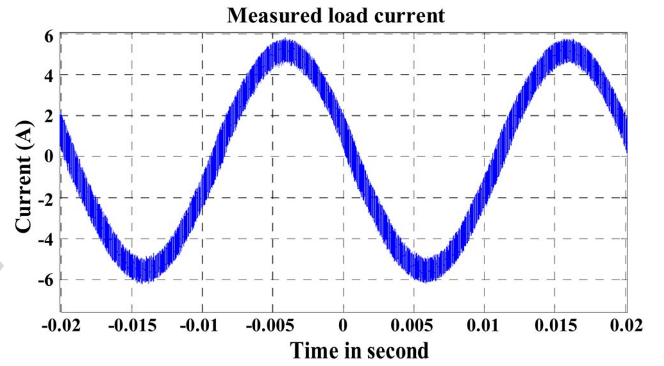
$$\eta = \frac{P_{\text{out}}}{P'_{\text{in}}} \times 100\% \tag{2}$$

$$P'_{\text{in}} = P_{\text{in}} - P_R \tag{3}$$

$$P_R = \frac{2\left(\frac{V_{\text{in}}}{2}\right)^2}{R} \tag{4}$$



(a)



(b)

Fig. 29. Experimental result: output voltage (V_AB) across the (a) load resistor and (b) output current.

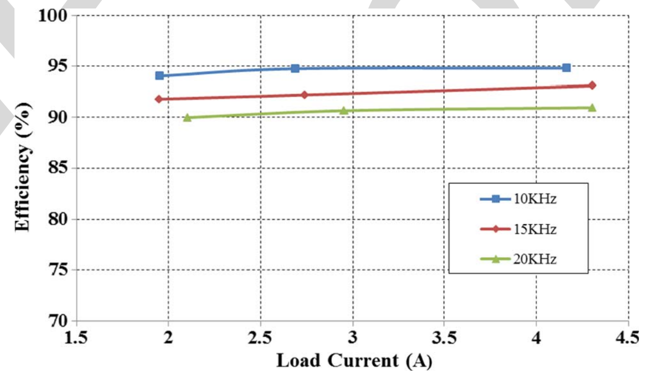


Fig. 30. Efficiency as a function of output current at different switching frequencies.

where

P_{in} input power of the overall circuit;

P_{out} output power;

P'_{in} converter input power.

The total power consumed by the two resistors (R1 and R2 in Fig. 27) was evaluated using (4) and deducted from the measured input power (P_{in}), which is the power that entered into the converter. Then, the efficiency of the converter is calculated.

Looking from the efficiency graph, at the higher switching frequency of 20 kHz, it can be seen that the efficiencies are still above 90% at light and full loads. The efficiency at 20 kHz is 4% lower than that of the 10-kHz switching frequency operation. However, a 20-kHz frequency operation can save

TABLE III
LOAD INDUCTOR COMPARISON

	10KHz	20KHz
	5mH	2.5mH
Output current ripple	0.531A	0.508A
Commercial device	£67.22 – for 2.5mH, £182.08 – for 5mH,	

significant costs on the external passive components and make for a smaller package, while reducing the output ripple current. The price list shown in Table III indicates that using almost the same output ripple current of 0.5 A, a 20-kHz switching frequency operation can reduce the cost of the inductor by almost three times, using 10-kHz frequency operation. In addition, it is worth mentioning that the presented efficiency graph does not include the power consumed by the driver circuit, and it only includes the power semiconductor device losses, input resistance losses, and output inductance losses.

V. CONCLUSION AND OUTLOOK

This paper has presented an advanced integration approach for power device packaging, demonstrating the correct electrical functionality of the half-bridge power switch and its thermal performance. Solid bumps and thicker hollow bumps have better thermal performance than thinner hollow bumps, in terms of reducing the temperatures at the hottest IGBT. However, thinner hollow bumps can reduce the creep strain accumulation in the critical solder joints, as compared to the solid bumps and thicker hollow bumps. As for the thermomechanical simulation results, the 0.0625-mm-thick bumps can significantly reduce the maximum creep strain accumulation in the solder joints for the bump interconnects. For this reason, such results can effectively improve the reliability of the assembly, and the approach can greatly enhance power density and reduce stray inductance, while enabling double-sided cooling capability. Preliminary experimental results show an interesting advancement of the state of the art, which is represented by the recently proposed sandwich package concepts based on solid bump interconnections and double-sided cooling [10]–[12], in particular by ensuring a more even temperature distribution within the power module and by further reducing parasitic inductance. For future work, it is anticipated to extend this approach to a more advanced scheme while further reducing the stray inductance, improving the reliability of such assemblies and the ability to test with a direct substrate liquid cooling system.

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