Dynamic Phasor Analysis and Design of Phase-Locked Loops for Single Phase Grid Connected Converters

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Abstract

Purpose – The purpose of the paper is to introduce the Dynamic Phasor Modelling (DPM) approach for stability investigation and control design of single-phase Phase Locked Loops PLLs. The aim is to identify the system instabilities not predicted using the existent analysis and design methods based on the simplified average model approach.

Design/methodology/approach – This paper starts by investigating the performance of three commonly used PLL schemes: the Inverse Park-PLL, the SOGI-Frequency-Locked-Loop and the Enhanced-PLL, designed using the simplified average model and will show that following this approach, there is a mismatch between their actual and desired transient performance. A new PLL design method is then proposed based on the DPM approach that allows the development of fourth-order DPM models. The small-signal eigenvalues analysis of the 4^{th} order DPM models is used to determine the control gains and the stability limits.

Findings – The DPM approach is proven to be useful for single-phase PLLs stability analysis and control parameters design. It has been successfully used to design the control parameters and to predict the PLL stability limits, which have been validated via simulation and experimental tests consisting of grid voltage sag, phase jump and frequency step change.

Originality/value – this paper has introduced the use of DPM approach for the purpose of single-phase PLL stability analysis and control design. The approach has enabled accurate control gains design and stability limits identification of single-phase PLLs.

Keywords Single phase converters, Phase locked Loop, PLL, Dynamic phasor analysis.

Paper type Research paper.

1- Introduction

Phase-locked loops (PLLs) are widely used for interfacing power electronic converters to single and three-phase grids, (Chung, 2000; Golestan *et al.*, 2013; Silva *et al.*, 2004; Velasco *et al.*, 2011). They are used to extract the information about the fundamental voltage component (phase angle, frequency and voltage magnitude) under various grid disturbances such as the steady state presence of unbalance and harmonics or transients: voltage sag, phase-jump and frequency change. The operation of converters in single phase systems is more challenging because of reduced level of information available in a single phase voltage compared to multiphase.

There are a few single-phase PLL schemes widely discussed in the literature that differ in their structure and estimation laws: the Inverse Park-PLL (IP-PLL) (Filho *et al.*, 2008; Rashed *et al.*, 2013), the Synchronous Reference Frame PLL (SRF-PLL) (Nicastri *et al.*, 2010), the Second-Order Generalized Integrators (SOGI)-based Frequency-Locked Loop (FLL) (SOGI-FLL) (Rodr'iguez *et al.*, 2011), the D-filter-based estimation PLL (Shinnaka, 2011), the Enhanced PLL (EPLL) (Karimi-Ghartemani, 2013; Karimi-Ghartemani *et al.*, 2012) and the Modified Mixer Phase-Detector based PLL (MMPD-PLL), (Thacker *et al.*, 2011). Some of this research work has been aimed at studying the design and performance analysis of single-phase PLLs. The design is typically performed using the simplified average model of the PLL (Karimi-Ghartemani, 2013; Karimi-Ghartemani *et al.*, 2012; Thacker *et al.*, 201; Freijedo *et al.*, 2009) , which ignores the effect of inherently generated double-frequency component during transient on PLL stability. In (Karimi-Ghartemani, 2013), a comprehensive analysis and comparison of many single-phase PLL schemes is carried out using the simplified average model. The study concluded that the small signal mathematical model and the performance of the different PLL schemes were fairly similar, a conclusion which this paper will challenge.

This paper proposes a modelling technique not previously used in PLL stability analysis and design. The technique is known by Dynamic Phasor Modelling DPM and is suitable to represent and to predict the single-phase-PLL dynamic and instability modes not seen by the conventional average modelling technique used in the literature. In the DPM approach, the time-response of the system state variables is represented by a selective number of relevant frequency components of a Fourier series with slowly

time-varying coefficients, (Stankovic *et al.*, 1999; Sanders *et al.*, 1991; Emadi, 2004; Caliskan *et al.*, 1999; Mattavelli *et al.*, 1999). The DPM approach has been successfully applied for modelling and analysis of single phase induction motors (Stankovic *et al.*, 1999), PWM converters, (Sanders *et al.*, 1991), diode bridge rectifiers (Emadi, 2004), DC/DC converters, (Caliskan et al., 1999) and thyristor controlled series capacitor compensators in power systems (Mattavelli et al., 1999).

The DPM approach is also used for the design and stability study of frequency and voltage droop control of microgrids, (Mariani *et al.*, 2014; Xianwei *et al.*, 2011; De Brabandere *et al.*, 2005; Wang *et al.*, 2012). The DPM is found effective in predicting system instabilities not seen by the conventional quasi-steady-state small signal model, (De Brabandere *et al.*, 2005; Wang *et al.*, 2012).

- In this paper, a 4th order DPM is proposed and used for stability analysis, control design and performance comparison of the three representative single phase PLL schemes: the IP-PLL, SOGI-FLL and EPLL. The analysis will demonstrate the shortcomings of the conventional simplified average modelling for determining the stability limits and control gain design of the single-phase PLLs. The contribution of this paper lies in the following: Introducing the DPM approach for the purpose of single-phase PLLs stability analysis and control design.
- Accurate stability limits identification and control gains design of single-phase PLLs using DPM approach.

The paper is organised in five sections. Section 2 gives the basics of the DPM and PLLs. The design of the three PLL schemes using the simplified average model is presented in section 3. In section 4, the simulation results of the PLL schemes under investigation are used to show the discrepancy between their actual dynamic characteristics and the desired performance, and hence the inadequacy of the simplified average model based design. Section 5 details the proposed 4th-order DPM small-signal stability analysis, design and comparison of the three PLLs. Large signal disturbance investigation and performance comparison of the three PLL schemes are presented in section 6 using simulation and experimental validation. Conclusions are given in section 7.

2. Fundamental Principles of DPM and PLL

In this section, the fundamentals of the dynamic phasor modelling and the single-phase PLL concepts will be presented.

2.1 Fundamentals of DPM

In dynamic phasor modelling approach, the Fourier series coefficients of system state-variables are considered the DPM system-state-variables and the state equations are derived for these Fourier coefficients. Therefore, a system state variable $x(\tau)$ can be represented on the interval $\tau \in ((t-T), t]$ using a Fourier series of the form, (Stankovic *et al.*, 1999):

$$x(\tau) = \sum_{k=-\infty}^{\infty} [\langle x \rangle_k(t)] e^{jk\omega_b \tau} \tag{1}$$

Where, T is the time period for the base frequency, $\omega_b = 2\pi/T$, $\langle x \rangle_k(t)$ is the kth complex Fourier coefficient that is varying with time since the interval under consideration slides with time t. The notation < > denotes the averaging operation that is applied to determine the kth complex Fourier coefficient at time t. The averaging operation is

$$\langle x \rangle_k(t) = \frac{1}{T} \int_{t-T}^{t} x(\tau) e^{jk\omega_b \tau} d\tau \tag{2}$$

The kth-order DPM state-space differential equation is a state-space equation formed for the kth frequency-order Fourier series coefficient of the system state variables. The Zero-Order (ZO) DPM equation is the system state-space equation for the dc coefficients of the Fourier series for the system state variables. In practice, the ZO-DPM is the simplified average model usually used in the literature for conventional PLL design.

The derivative of the kth complex Fourier coefficient (2) is given by:

$$\frac{d}{dt}(\langle x \rangle_k) = \langle \frac{d}{dt} x \rangle_k - jk\omega_b \langle x \rangle_k \tag{3}$$

Also, the kth Fourier coefficient for a nonlinear term (e.g. a product of two state variables *x* and *y*) can be obtained using the convolution property (Sanders *et al.*, 1991) as follows:

$$\langle xy \rangle_k = \sum_{l=-\infty}^{\infty} \langle x \rangle_{(k-l)} \langle y \rangle_l \tag{4}$$

Noting that the phasor $\langle x \rangle_{-k}$ is the complex conjugate of $\langle x \rangle_k$. The properties in (3) and (4) are essential for deriving the PLL DPM from the time-domain state space model.

This mathematical approach will be used later to derive the DPM for the PLL schemes under study.

2.2 Fundamentals of PLLs

The structure of a typical PLL scheme that includes also the single-phase PLLs is originated from the well-established three-phase SRF-PLL (Chung, 2000). The 3-phase SRF-PLL contains three main components: the Phase Detector (PD), the filter (which is usually a PI controller), and the Voltage Controlled Oscillator (VCO). These components aim at synchronising the PLL estimated output voltage vector with the input voltage vector as represented by the two orthogonal $\alpha\beta$ voltage components as illustrated in the phasor diagram shown in Fig. 1. The PD generates an error signal (referred as "adaptive law") that is proportional to the phase difference between the input and the estimated output voltage vectors. The error signal is utilised to modify the frequency of the VCO until the average frequency and the phase angle of the input and the estimated (output) voltage vectors are equal (Golestan *et al.*, 2013).

In single phase PLLs (e.g. Fig.2), the measured grid voltage is fed as the α-axis component of the input voltage vector while the β-axis is substituted by a virtual voltage component. The virtual β-axis voltage component can be constructed by applying a 90^o phase shift to the measured α-axis voltage component (Silva *et al.*, 2004; Velasco *et al.*, 2011) or substituted by the estimated β-axis component, (Filho *et al.*, 2008; Rodr'iguez *et al.*, 2011; Karimi-Ghartemani, 2013). The main problem affecting the performance of a single phase PLL is that any mismatch/error in the virtual β-axis component (during transient or steady state) will produce double-frequency ripple component that adversely affects the dynamic performance and the stability of the PLL.

The relationships between the input and the estimated output voltage vectors and their phase angles and rotational speeds are represented and defined by the phasor diagram shown in Fig. 1.

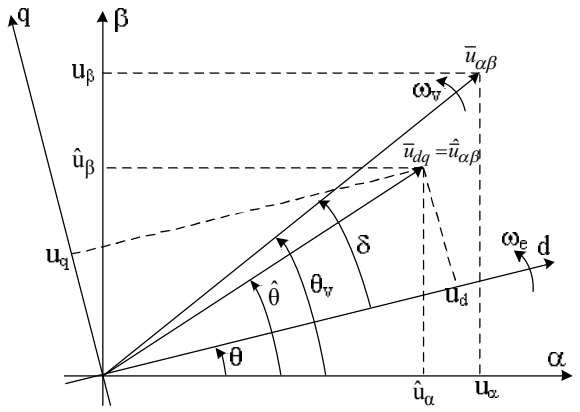

Fig. 1 Single-phase PLL phasor diagram.

Where u_α is the measured grid voltage whilst $\bar{u}_{\alpha\beta} = u_\alpha + ju_\beta$ is the fictious αβ grid voltage vector. If U_v is the grid voltage magnitude, then $u_\alpha = U_v \cos(\theta_v)$. The estimated (output) voltage vector $\hat{\bar{u}}_{\alpha\beta} = \hat{u}_\alpha + j\hat{u}_\beta = \bar{u}_{dq}$ has the corresponding u_d, u_q components in the dq rotating reference frame. The corresponding angles and the rotational speeds that will be used in the development of the DPM of the PLL are also shown in Fig. 1. The phase angle δ is the phase angle difference between the phase angle of the input voltage vector, θ_v and the phase angle $\hat{\theta}$.

3. Modelling and Control Design of Single-Phase PLLs

In this section, the IP-PLL, (Filho *et al.*, 2008), SOGI-FLL, (Rodr'iguez *et al.*, 2011) and the EPLL (Karimi-Ghartemani, 2013; Karimi-Ghartemani et al., 2012) single-phase PLL schemes will be modelled and the phase angle, voltage magnitude and frequency estimation algorithms for the three PLLs will be established utilising the simplified average model. This will be used in the next sections to prove that the dynamic performance of the designed PLLs will not match with the design specification.

The convention used in this paper is that the input of the PLL seen as a control system is the grid voltage, while the outputs are the estimated grid voltage magnitude, frequency and phase angle, which are defined as u_{out}, ω_{out} and θ_{out}, independent on the estimation method used in each PLL.

3.1 The Modelling and Control Design of the Inverse Park PLL

The typical model of the Inverse Park PLL (IP-PLL) expressed in rotating reference frame (Filho *et al.*, 2008; Karimi-Ghartemani, 2013) is shown in Fig. 2.

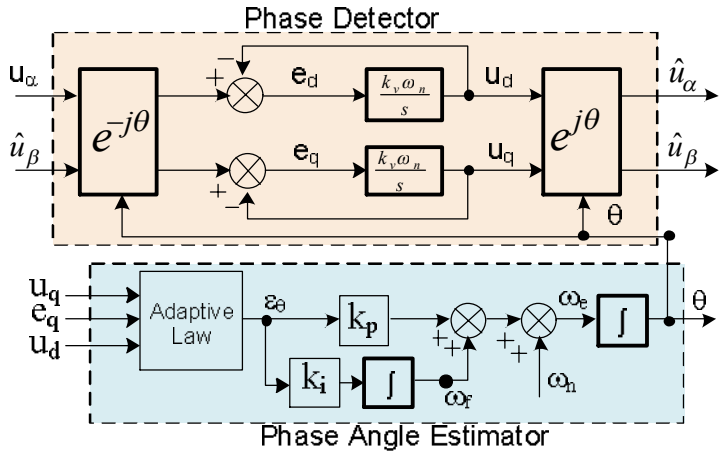

Fig. 2 The model of the Inverse Park Phase Locked Loop (IP-PLL)

The state space variable model for the IP-PLL (Fig. 2) in the rotating reference frame dq is given by:

$$\dot{u}_d = k_v\omega_n\left[0.5U_v cos(\delta) - 0.5u_d + 0.5U_v cos(\delta + 2\theta) - 0.5u_d cos(2\theta) + 0.5u_q sin(2\theta)\right] \quad (5a)$$

$$\dot{u}_q = k_v\omega_n\left[0.5U_v sin(\delta) - 0.5u_q - 0.5U_v sin(\delta + 2\theta) + 0.5u_d sin(2\theta) + 0.5u_q cos(2\theta)\right] \quad (5b)$$

$$\dot{\omega}_f = k_i\,(\varepsilon_\theta) \quad (5c)$$

$$\dot{\delta} = \omega_v - k_p\varepsilon_\theta - \omega_f - \omega_n \quad (5d)$$

Where: ε_θ is the adaptive law (error signal) given by (6), and $\omega_e = (k_p\varepsilon_\theta + \omega_f + \omega_n)$, $\delta = \theta_v - \theta$, $\frac{d}{dt}\theta = \omega_e$, $\frac{d}{dt}\theta_v = \omega_v$ and ω_n is angular speed (rad/s) corresponding to the nominal grid frequency (50Hz).

The adaptive law ε_θ for IP-PLL phase angle estimation was obtained as in (Filho *et al.*, 2008; Rashed *et al.*, 2013):

$$\varepsilon_\theta = \frac{u_q}{u_d} \quad (6)$$

It should be noted that in the literature, the simplified average model typically used in PLL design (Filho *et al.*, 2008; Karimi-Ghartemani, 2013; Thacker *et al.*, 2011; Freijedo *et al.*, 2009) is obtained by ignoring the double-frequency sine and cosine terms in (5a-b).

For the development of the dynamic-phasor differential equations used in the modelling of the PLL schemes under study in this paper for the purpose of stability analysis and control design, the time

period T in (1),(2) is set equal to $2\pi/\langle\omega_e\rangle_0$ and hence ω_b in (3) is substituted by $\langle\omega_e\rangle_0$. Then, the generalised k[th]-order dynamic-phasor state-space differential equations for (5) are given by:

$$\frac{d}{dt}\langle u_d\rangle_k = -jk\langle\omega_e\rangle_0\langle u_d\rangle_k + k_v\omega_n\langle e_d\rangle_k \quad (7a)$$

$$\frac{d}{dt}\langle u_q\rangle_k = -jk\langle\omega_e\rangle_0\langle u_q\rangle_k + k_v\omega_n\langle e_q\rangle_k \quad (7b)$$

$$\frac{d}{dt}\langle\omega_f\rangle_k = -jk\langle\omega_e\rangle_0\langle\omega_f\rangle_k + k_i\langle\varepsilon_\theta\rangle_k \quad (7c)$$

$$\frac{d}{dt}\langle\delta\rangle_k = -jk\langle\omega_e\rangle_0\langle\delta\rangle_k - \langle k_p\varepsilon_\theta + \omega_f + \omega_n\rangle_k + \langle\omega_v\rangle_k \quad (7d)$$

where, e_d, e_q are

$$e_d = 0.5U_v cos(\delta) - 0.5u_d + 0.5U_v cos(\delta + 2\theta) - 0.5u_d cos(2\theta) + 0.5u_q sin(2\theta) \quad (7e)$$

$$e_q = 0.5U_v sin(\delta) - 0.5u_q - 0.5U_v sin(\delta + 2\theta) + 0.5u_d sin(2\theta) + 0.5u_q cos(2\theta) \quad (7f)$$

The DPM of the nonlinear terms such as $cos(2\theta)$, $sin(2\theta)$ and (u_q/u_d) in (7e,f), (6) are obtained as in Appendix 1. The ZO-DPM that corresponds to k = 0 in (7) is then given by:

$$\langle\dot{u}_d\rangle_0 = k_v\omega_n(0.5\langle U_v\rangle_0 - 0.5\langle u_d\rangle_0) \quad (8a)$$

$$\langle\dot{u}_q\rangle_0 = k_v\omega_n\langle 0.5U_v\delta - 0.5u_q\rangle_0 \quad (8b)$$

$$\langle\dot{\omega}_f\rangle_0 = k_i\langle\varepsilon_\theta\rangle_0 \quad (8c)$$

$$\langle\dot{\delta}\rangle_0 = \langle\omega_v\rangle_0 - \langle k_p\varepsilon_\theta + \omega_f + \omega_n\rangle_0 \quad (8d)$$

and

$$\langle e_d\rangle_0 = 0.5\langle U_v\rangle_0 - 0.5\langle u_d\rangle_0 \quad (8e)$$

$$\langle e_q\rangle_0 = 0.5\langle U_v\rangle_0\langle\delta\rangle_0 - 0.5\langle u_q\rangle_0 \quad (8f)$$

From now on, unless otherwise mentioned, the averaging operation symbol $< >_0$ will be ignored for simplicity.

In the following sections, the ZO-DPM such as in (8), which is the simplified average model typically used in the literature in the PLL design, will be used for the design of the phase angle, voltage magnitude and frequency estimator to achieve the design specifications set for the small signal closed loop transfer function (CLTF) of (θ_{out}/θ_v), (u_{out}/U_v) and (ω_{out}/ω_v) for all PLL schemes under study. Afterwards, the actual dynamic performance of the designed PLLs will be proven not to match the design specifications and hence proving the shortcoming of using the ZO-DPM for single-phase PLL design.

First, the small signal ZO-DPM for the adaptive law (6) is derived in Laplace form using (8) for the PLL equilibrium point where $[u_d\ u_q] = [U_v\ 0]$:

$$\Delta\varepsilon_\theta = \frac{0.5k_v\omega_n}{s+0.5k_v\omega_n}\Delta\delta \tag{9}$$

(9) shows that $\Delta\varepsilon_\theta$ is linearly dependent on Δδ via the transfer function of a LPF. To eliminate the LPF influence in (9), a new phase angle adaptive law to replace (6) is introduced in this paper:

$$\varepsilon_\theta = \frac{u_q}{u_d} + 2\left(\frac{e_q}{u_d}\right) \tag{10}$$

which results in a small signal ZO-DPM of

$$\Delta\varepsilon_\theta = \Delta\delta \tag{11}$$

identical (for comparison purpose) to the small signal adaptive law model of the other PLL scheme (EPLL) as it will be shown later. Fig. 3 depicts the resulting small signal ZO-DPM for the IP-PLL phase angle estimator using the proposed adaptive law in (10),(11).

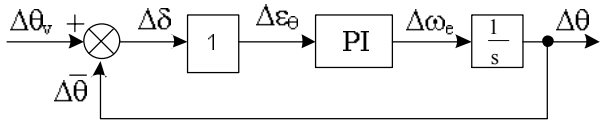

Fig. 3 Small signal ZO-DPM for the IP-PLL phase angle estimator

In the IP-PLL, the outputs θ_{out} and u_{out} are set equal to θ and u_d. Hence, the small signal ZO-DPM CLTF for the IP-PLL phase angle estimator (from Fig. 3) is given by:

$$\frac{\Delta\theta_{out}}{\Delta\theta_v} = \frac{\Delta\theta}{\Delta\theta_v} = \frac{k_p s+k_i}{s^2+k_p s+k_i} \tag{12}$$

Where k_p and k_i are the gains of the PI controller.

The small signal CLTF for the output (estimated) voltage magnitude is also derived from (8) and is equivalent to a first order LPF (13) with a time constant of $2/k_v\omega_n$:

$$\frac{\Delta u_{out}}{\Delta U_v} = \frac{\Delta u_d}{\Delta U_v} = \frac{0.5k_v\omega_n}{s+0.5k_v\omega_n} \tag{13}$$

The gain k_v (13) determines the dynamic response of the voltage magnitude estimation. On the other hand, the k_p and k_i gains of the PI controller (12) determine the dynamic characteristics for the phase-angle estimation. The values of k_p and k_i are chosen to achieve a damping coefficient $\xi = 1$ for (12) as recommended in (Karimi-Ghartemani *et al.*, 2012; Freijedo *et al.*, 2009). In this paper, k_p is selected to be equal to $k_v\omega_n$ so that the CLTF poles of (12) coincide with the CLTF pole of the voltage magnitude estimator in (13). And hence, $k_i = (k_v\omega_n/2)^2$. Therefore, the small signal ZO-DPM CLTF poles of

the PLL voltage and phase-angle estimators are located on the real axis at $(-k_v\omega_n/2)$. Then, the phase-angle estimator small signal CLTF (13) can be expressed as:

$$\frac{\Delta\theta_{out}}{\Delta\theta_v} = \frac{\Delta\theta}{\Delta\theta_v} = \frac{k_v\omega_n s+(0.5k_v\omega_n)^2}{s^2+k_v\omega_n s+(0.5k_v\omega_n)^2} \tag{14}$$

In (Rodr'iguez *et al.*, 2011), the small signal CLTF for the frequency estimator ω_{out}/ω_v was equivalent to a first order LPF. In this paper (for comparison purpose) we will also carry out the design to achieve a LPF behaviour for the CLTF of the frequency estimator. Therefore, ω_{out} for IP-PLL is proposed here to be:

$$\omega_{out} = \omega_e - 0.5k_p\varepsilon_\theta \tag{15}$$

which yields a LPF small signal ZO-DPM CLTF of;

$$\frac{\Delta\omega_{0ut}}{\Delta\omega_v} = \frac{0.5k_v\omega_n}{s+0.5k_v\omega_n} \tag{16}$$

It should be noted from (13), (14) and (16) that the CLTF poles for the PLL estimators (θ_{out}, u_{out} and ω_{out}) are located at $-0.5k_v\omega_n$ and k_v becomes the only gain that determines the small signal dynamic response of the PLL estimators. Having only one control gain is deliberate to simplify the comparison of the PLLs in this paper.

In the next sections, small signal ZO-DPM CLTFs will be derived for the SOGI-FLL and EPLL estimators to be identical to (13), (14) and (16), which if the ZO-DPM design approach is adequate, it will result in identical performance matching the design specification.

3.2 The Modelling and Control Design of the SOGI-FLL

The typical implementation of the SOGI-FLL (Rodr'iguez *et al.*, 2011) is shown in Fig. 4. Compared to the IP-PLL, SOGI-FLL model is implemented in the stationary reference frame. For comparison purpose, the stationary frame SOGI-FLL model needs to be transformed to the rotating reference frame.

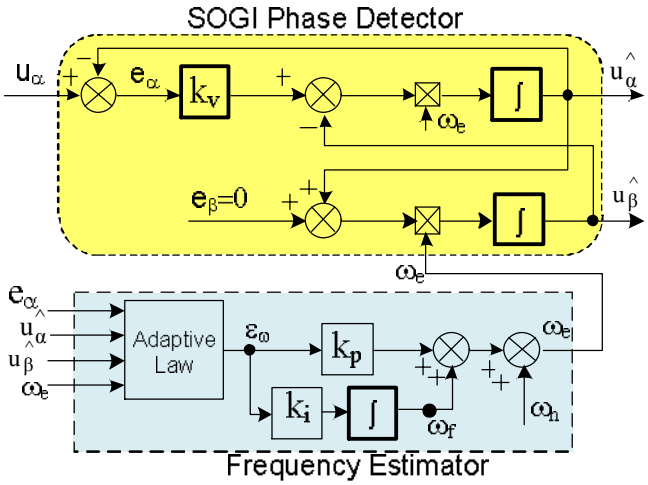

Fig. 4 Typical model of the SOGI-FLL

The model for the SOGI-FLL phase detector (Fig.4) as presented in (Rodr'iguez *et al.*, 2011) is

$$\dot{\hat{u}}_\alpha = [(u_\propto - \hat{u}_\propto)k_v - \hat{u}_\beta]\omega_e \quad \& \quad \dot{\hat{u}}_\beta = \omega_e \hat{u}_\propto \tag{17}$$

The transformed SOGI-FLL (Fig. 4) model expressed in the rotating reference frame (assuming slow varying ω_e) is:

$$\dot{u}_d = k_v\omega_e\left[0.5U_v\cos(\delta) - 0.5u_d + 0.5U_v\cos(\delta + 2\theta) - 0.5u_d\cos(2\theta) + 0.5u_q\sin(2\theta)\right] \tag{18a}$$

$$\dot{u}_q = k_v\omega_e\left[0.5U_v\sin(\delta) - 0.5u_q - 0.5U_v\sin(\delta + 2\theta) + 0.5u_d\sin(2\theta) + 0.5u_q\sin(2\theta)\right] \tag{18b}$$

$$\dot{\omega}_f = k_i\,(\varepsilon_\omega) \tag{18c}$$

$$\dot{\delta} = \omega_v - k_p\varepsilon_\omega - \omega_f - \omega_n \tag{18d}$$

where: ε_ω is the adaptive law and is given by (19), $\omega_e = (k_p\varepsilon_\omega + \omega_f + \omega_n)$ and $d\theta/dt = \omega_e$.

The model in (18) is quite similar to that of IP-PLL (5). However, the SOGI-FLL is robust to grid frequency variation since ω_n in (5) is replaced by the estimated value ω_e in (18).

The frequency adaptive law as given in (Rodr'iguez *et al.*, 2011) is:

$$\varepsilon_\omega = \frac{-k_v\omega_e e_\alpha \hat{u}_\beta}{\hat{u}_\alpha^2 + \hat{u}_\beta^2} \tag{19}$$

The small-signal ZO-DPM based transfer function of the adaptive law in (19) around the equilibrium point *($\omega_e = \omega_n$, $u_q = 0$)* is:

$$\Delta\varepsilon_\omega = \frac{0.5k_v\omega_n}{s + 0.5k_v\omega_n}(\Delta\dot{\delta}) \tag{20}$$

Equation (20) shows that contrary to the small signal model given in (Rodr'iguez *et al.*, 2011), the adaptive law small signal transfer function is equivalent to the transfer function of a first order LPF and for this reason, a full PI controller is used (see Fig. 4) for frequency estimation rather than an

Integral controller as in (Rodr'iguez *et al.*, 2011). The PI controller gains are set $k_p = 1$ and $k_i = 0.5k_v\omega_e$ in order to obtain a small-signal CLTF equivalent to that of the IP-PLL (16). Hence, the small signal ZO-DPM for the frequency estimator (19)-(20) is represented by the block diagram in Fig. 5.

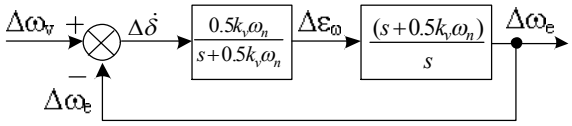

Fig. 5 Small signal ZO-DPM for the SOGI-FLL frequency estimator

with the small-signal ZO-DPM based CLTF:

$$\frac{\Delta\omega_{out}}{\Delta\omega_v} = \frac{\Delta\omega_e}{\Delta\omega_v} = \frac{0.5k_v\omega_n}{s+0.5k_v\omega_n} \tag{21}$$

The SOGI-FLL output phase angle θ_{out} is given by, (Rodr'iguez *et al.*, 2011):

$$\theta_{out} = \hat{\theta} = atan\left(\frac{\hat{u}_\propto}{\hat{u}_\beta}\right) = \theta + atan\left(\frac{u_q}{u_d}\right) \tag{22}$$

Then, the small signal ZO-DPM based CLTF for the phase angle estimator is derived using (21), (22) and (18) at the equilibrium point ($\omega_e = \omega_n$, $u_q = 0$) and given by:

$$\frac{\Delta\theta_{out}}{\Delta\theta_v} = \frac{\Delta\theta}{\Delta\theta_v} = \frac{k_v\omega_n s+(0.5k_v\omega_n)^2}{s^2+k_v\omega_n s+(0.5k_v\omega_n)^2} \tag{23}$$

which is equivalent to (14) for the IP-PLL. Furthermore, the estimated voltage magnitude in SOGI-FLL is calculated as

$$u_{out} = \hat{u} = \sqrt{u_d^2 + u_q^2} \tag{24}$$

and the small signal ZO-DPM based CLTF for (24) at the equilibrium point ($\omega_e = \omega_n$; $u_q = 0$) is derived and given by:

$$\frac{\Delta u_{out}}{\Delta U_v} = \frac{\Delta\hat{u}}{\Delta U_v} = \frac{0.5k_v\omega_n}{s+0.5k_v\omega_n} \tag{25}$$

From (21),(23),(25), the SOGI-FLL is designed to provide identical small signal ZO-DPM CLTF to that for IP-PLL frequency (16), phase angle (14) and voltage magnitude (13) estimators. This procedure will be repeated for the EPLL in the next section.

3.3 The Modelling and Control Design of the EPLL

The typical EPLL model (Karimi-Ghartemani, 2013; Karimi-Ghartemani *et al.*, 2012) is represented by the block diagram given in Fig. 6.

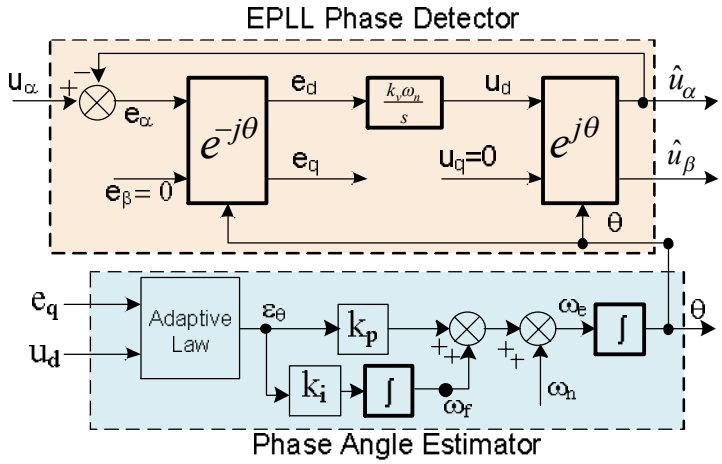

Fig. 6 Typical model of the EPLL

The EPLL model in the rotating reference frame is:

$$\dot{u}_d = k_v\omega_n[0.5U_v\cos(\delta) - 0.5u_d + 0.5U_v\cos(\delta + 2\theta) - 0.5u_d\cos(2\theta)] \quad (26a)$$

$$\dot{\omega}_f = k_i\,(\varepsilon_\theta) \quad (26b)$$

$$\dot{\delta} = \omega_v - k_p\varepsilon_\theta - \omega_f - \omega_n \quad (26c)$$

$$e_q = [0.5U_v\sin(\delta) - 0.5U_v\sin(\delta + 2\theta) + 0.5u_d\sin(2\theta)] \quad (26d)$$

Where, the adaptive law ε_θ for phase angle estimation as used in (Karimi-Ghartemani, 2013; Karimi-Ghartemani *et al.*, 2012) is:

$$\varepsilon_\theta = \frac{2e_q}{u_d} \quad (27)$$

The small signal ZO-DPM transfer function for the adaptive law (27) at the equilibrium point ($e_q = 0$) is:

$$\Delta\varepsilon_\theta = \Delta\delta \quad (28)$$

which is identical to (11) for IP-PLL and hence k_p, k_i and the ZO-DPM CLTF of the phase angle estimator for the EPLL are equal to that given in (12) and (14).

In the EPLL, $u_{out} = u_d$ and hence the small-signal ZO-DPM CLTF of the voltage magnitude estimator is derived from (26) and given by:

$$\frac{\Delta u_{out}}{\Delta U_v} = \frac{\Delta u_d}{\Delta U_v} = \frac{0.5k_v\omega_n}{s+0.5k_v\omega_n} \quad (29)$$

Similar to the IP-PLL, the output frequency ω_{out} for the EPLL is calculated as.

$$\omega_{out} = \omega_e - 0.5k_v\omega_n\varepsilon_\theta \quad (30)$$

with the small-signal ZO-DPM CLTF of:

$$\frac{\Delta\omega_{out}}{\Delta\omega_v} = \frac{0.5k_v\omega_n}{s+0.5k_v\omega_n} \quad (31)$$

with this, the small signal ZO-DPM CLTFs for phase angle, frequency and voltage magnitude estimators for all three PLL schemes under study have been designed to be identical and this should lead to identical dynamic performance. Also, the transfer functions show that the PLLs should remain stable in a very wide range of k_v. In the next section, the performance of the designed PLLs (using the ZO-DPM) will be investigated using simulations with different values of k_v which should help in validating the ZO-DPM based design approach and identifying the potential differences in actual dynamic performance.

4. Performance Comparison of PLL Schemes Designed Using the ZO-DPM

The PLL schemes presented in Figs 2, 4 and 6 and using the adaptive laws in (10), (19) and (27) and having the control gains k_p and k_i designed to provide identical ZO-DPM based small signal CLTFs are implemented using Simulink/Matlab. The simulation models are tested for three small step changes in phase-angle, frequency and voltage magnitude for different values of gain k_v. The higher the value of k_v, the faster the expected PLL dynamic response.

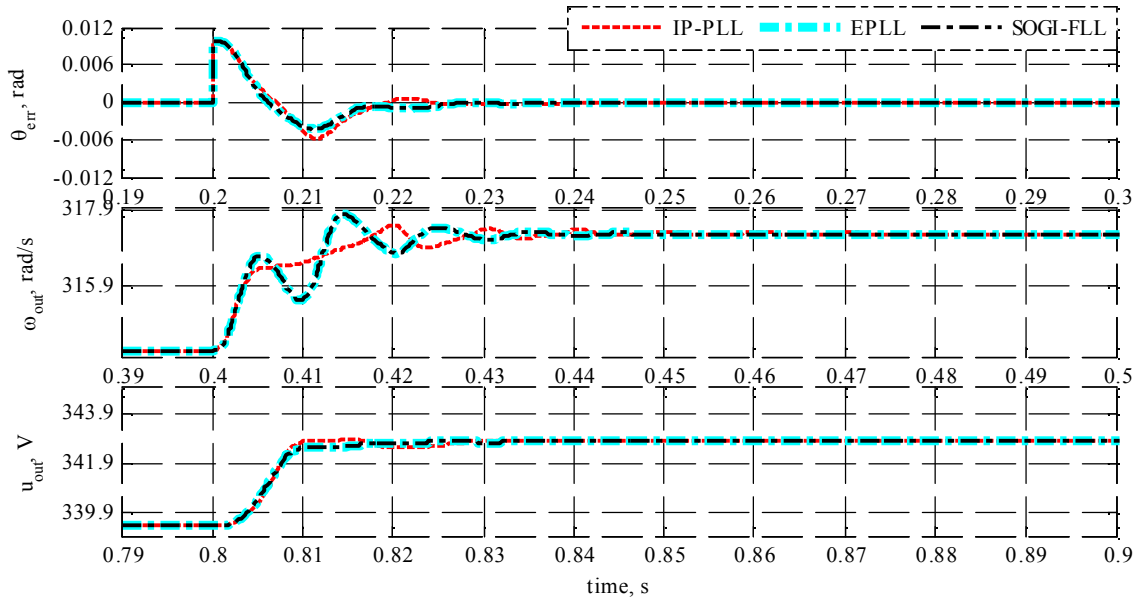

Fig. 7 Simulation results: PLLs testing under three small signal step changes for $k_v = 1$. Top subplot: shows phase angle response to a phase-angle step of 0.01 rad (at t=0.2s), middle subplot: shows frequency response to a frequency step of 1% (at t=0.4s), bottom subplot: shows voltage magnitude response to a voltage step of 1% (at t=0.8s). "red" IP-PLL, "cyan" EPLL, "black" SOGI-FLL.

The simulation results from the three tests with $k_v = 1$ is shown in Fig. 7. It is noted that the dynamic response for all PLLs has a superimposed transient oscillation that decays quickly. The SOGI-FLL and the EPLL response are visibly identical for all three tests, while the IP-PLL response differs slightly,

with the largest mismatch noticed in the frequency step change test. The three tests are repeated for kv = 2 (faster PLL dynamic performance is expected). The simulation results are shown in Fig. 8. It is clear that the IP-PLL becomes unstable in all three tests but the SOGI-FLL and the EPLL remain stable but having slow decaying oscillations, although a higher k_v should have resulted in shorter time response, which contradicts the desired dynamic performance set for the ZO-DPM based design.

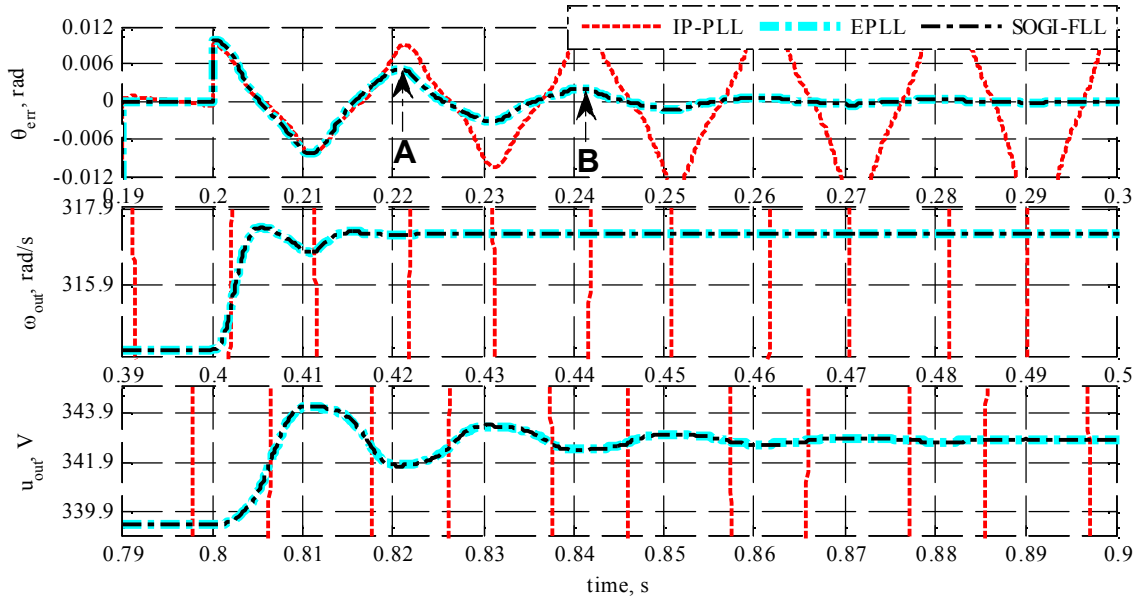

Fig. 8 Simulation results: PLLs testing under small signal step changes for $k_v = 2$. Top subplot: shows phase angle response to a phase-angle step of 0.01 rad (at t=0.2s), middle subplot: shows frequency response to a frequency step of 1% (at t=0.4s), bottom subplot: shows voltage magnitude response to a voltage step of 1% (at t=0.8s). "red" IP-PLL, "cyan" EPLL, "black" SOGI-FLL.

From the simulation results for θ_{err} (δ) in (Fig. 8), the slow dynamic PLL eigenvalue that is responsible of the slow decaying oscillation can be approximately determined by measuring the ratio magnitude between two consecutive oscillation peaks A ($\Delta\theta_A$=0.005rad, t_A=0.221s) and B ($\Delta\theta_B$=0.002rad, t_B=0.241s) which results in the position of the eigenvalue on the real axis of $-\ln(\Delta\theta_A/\Delta\theta_B)/(t_A-t_B) \sim -45.8s^{-1}$. This results in much slower response in comparison to $-314.1\ s^{-1}$, the desired PLL eigenvalue as emerged from the ZO-DPM based design (14), for k_v=2 (see text above (14)). The problem is that this slow dynamic eigenvalue which is noted by the simulation results of the actual PLL was not possible to be predicted by the ZO-DPM and this is why a higher order DPM is proposed to account for the effect of selected frequency components that might have resulted in such slow dynamic eigenvalue. The DPM developed in general form in §3 (e.g. for IP-PLL (7)) is customised to 4^{th}-order DPM and will be used in the design of the three PLL schemes in the next section.

5. Fourth-order Dynamical Phasor Model based Stability Analysis of the PLL Schemes Under Investigation

5.1 Analysis of the 4th-order DPM for IP-PLL

The 4th-order DPM for the IP-PLL is established using (7), (10). The model is linearized and the small signal eigenvalues are obtained for the equilibrium point $u_q = 0$, $u_d = U_v$. The linearized state space model is of 36th order (4 states for the zero-order and 8 states for each "complex" order from 1 to 4), which for the sake of maintaining a reasonable paper length, are not detailed. Only four trajectories (TA, TB, TC and TD) for the most dominant complex eigenvalues are plotted in Fig. 9 for $0.52 < k_v < 2.1$. Four sets of the eigenvalues are highlighted for $k_v = 0.52$ (blue square), 0.92 (cyan star), 1 (red diamond) and 1.12 (green circle) as shown in Fig. 9.

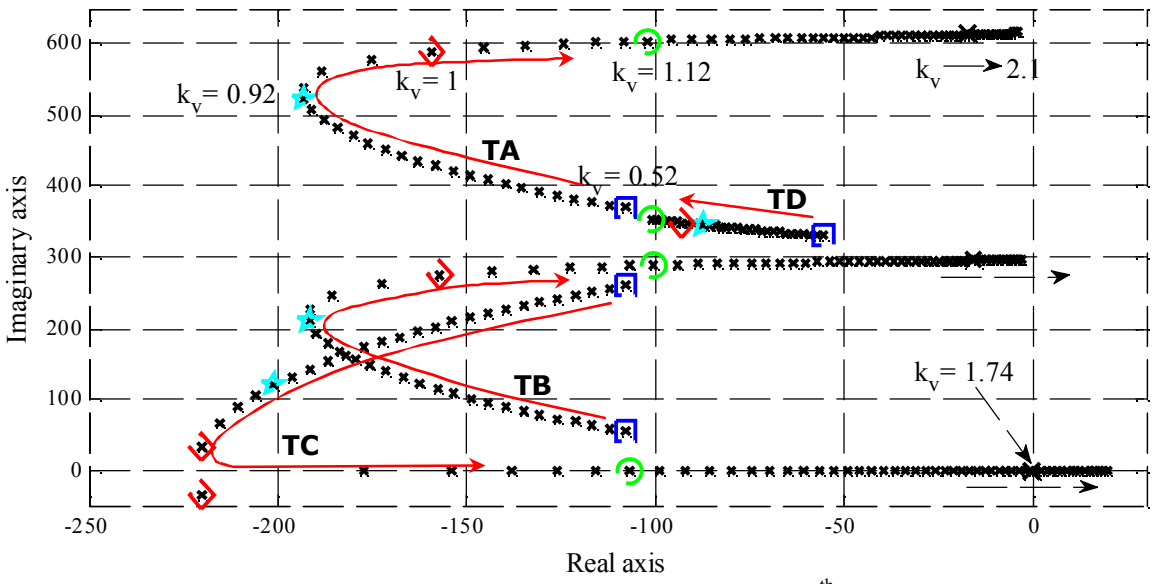

Fig. 9 The four most significant eigenvalue trajectories for the IP-PLL 4th order DPM, ($0.52 < k_v < 2.1$).

The results show that for $k_v > 1.74$, the eigenvalue TC moves to the right hand plane (instability region), which is consistent with the simulation results presented in Fig. 8 for $k_v = 2$ and in contradiction with the ZO-DPM based small-signal analysis that untruly tells that the PLL is stable for any values of k_v. It is also noted that as k_v increases from 0.52 to 0.92, the eigenvalues move further into the left side of the s-plane. The increase of k_v beyond 0.92 makes three eigenvalue trajectories (TA, TB and TC) to reverse direction towards the unstable side of the s-plane one of which (TC) will tend to cross the stability line first at $k_v > 1.74$. Because the position of one eigenvalue (TD) starts (at

k_v=0.52) significantly on the right side compared to the other three and slowly moves left, whilst the other three start moving right for k_v>0.92, the optimum k_v is chosen 1.12 so that the position of all four eigenvalues are pushed as left as possible with respect to the real axis to maximize the dynamic response.

5.2 Analysis of the 4th-order DPM for SOGI-FLL

The 4th-order DPM for the SOGI-FLL is derived from (18),(19). The linearized state-space model is of 36th order (not shown to minimise paper length) and the trajectories (TA, TB, TC and TD) of the four most dominant complex eigenvalues are plotted in Fig. 10 for 0.92< k_v < 3.3. It is found that the eigenvalues for the SOGI-FLL (Fig. 10) are situated more to the left than the eigenvalues for IP-PLL (Fig. 9), which means SOGI-FLL will actually provide better dynamic response than the IP-PLL that contradicts the expected identical dynamic characteristic for all PLLs under study as imposed by the ZO-DPM based design (§3). In Fig. 10, three sets of eigenvalues are highlighted for k_v = 0.92 (blue square), 1.3 (red diamond), 1.44 (green circle). This stability analysis based on eigenvalues confirms that the SOGI-FLL is stable for k_v < 2.82, which is consistent with the simulation results shown in Fig. 8. Based on the results in Fig. 10, it is recommended that k_v < 1.44 to ensure the placement of all the most dominant eigenvalues is situated as far left as possible into the s-plane. The stability limit is found at k_v = 2.82.

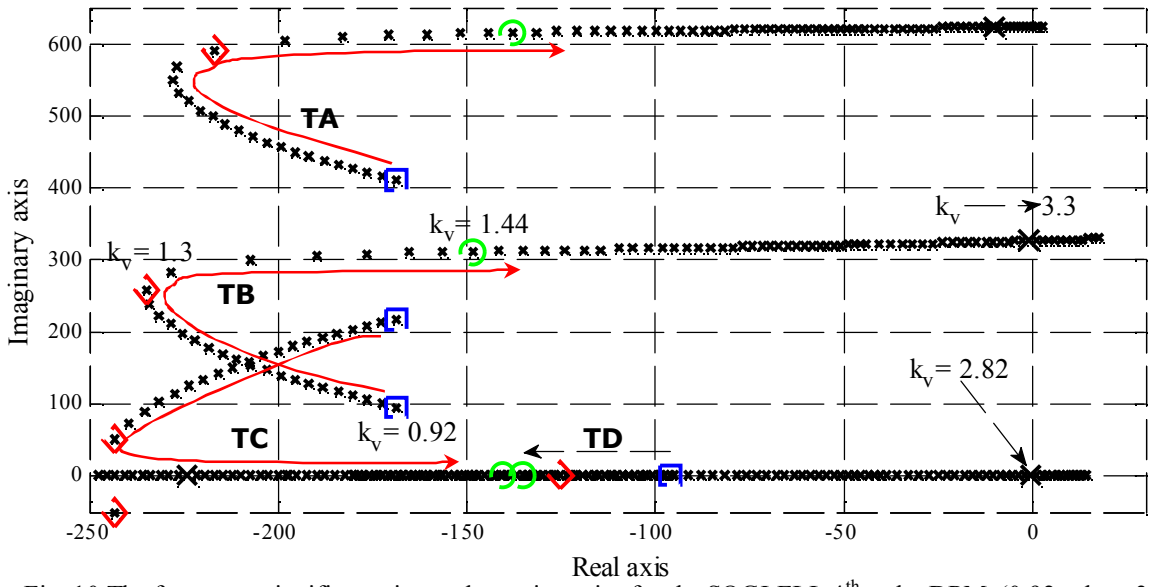

Fig. 10 The four most significant eigenvalue trajectories for the SOGI-FLL 4th order DPM, (0.92 < k_v < 3.3).

5.3 Analysis of the 4th-order DPM for EPLL

The state space model for the EPLL (26), (28) is also used to derive the 4th-order DPM. The linearized state space model is of 27th order and the trajectories of the four most dominant complex eigenvalues are plotted in Fig. 11 for $0.92 < k_v < 3.3$. The EPLL eigenvalue trajectories reveal similar trend to that of the SOGI-FLL. The EPLL is also found unstable for $k_v > 2.82$. Three sets of eigenvalues are highlighted for $k_v = 0.92, 1.3, 1.44$ as shown in Fig. 11. The trajectories of the EPLL and SOGI-FLL eigenvalues are almost the same as revealed by comparing Figs 10 and 11. Therefore, the recommended value for k_v is equal to that for SOGI-FLL, i.e. $k_v < 1.44$.

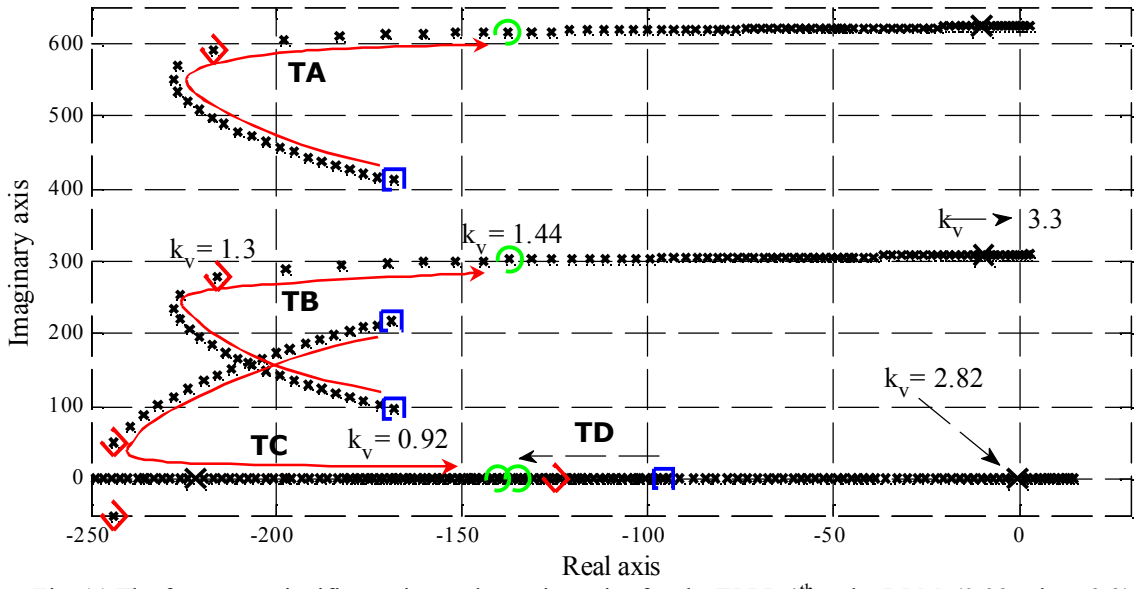

Fig. 11 The four most significant eigenvalue trajectories for the EPLL 4th order DPM, ($0.92 < k_v < 3.3$).

5.4 Validation by Simulation of the 4th-order DPMs

The analysis of the eigenvalues presented in the previous sections can be summarised in Table 1 which contains the values of k_v for operation at stability limit (top), for keeping all of the most dominant eigenvalues as far left on the s-plane as possible as a design limit (middle) and a set of gains selected in the paper (bottom) that agree with both previous limitations and were recommended to be used in the large signal tests.

Table 1: Gain k_v design values for the three PLLs under study.

	IP-PLL	SOGI-FLL	EPLL
Stability limit	$k_v < 1.72$	$k_v < 2.82$	$k_v < 2.82$
Design limit	$k_v < 1.12$	$k_v < 1.44$	$k_v < 1.44$
Recommended in this paper	$k_v = 1$	$k_v = 1.3$	$k_v = 1.3$

The eigenvalues analysis of the 4th-order DPM of the PLL schemes under study is validated by simulation. Fig. 12 illustrates the simulation results of the three PLL schemes for $k_v = 2.82$ subjected to small step changes in phase angle, frequency and voltage magnitude. All three tests show that the IP-PLL is unstable while the SOGI-FLL and the EPLL response were both on the verge of instability. These findings validate the obtained stability limits from the small signal eigenvalues analysis shown in Figs 9-11 and hence prove the suitability of the 4th-order DPM for PLL stability analysis and control design.

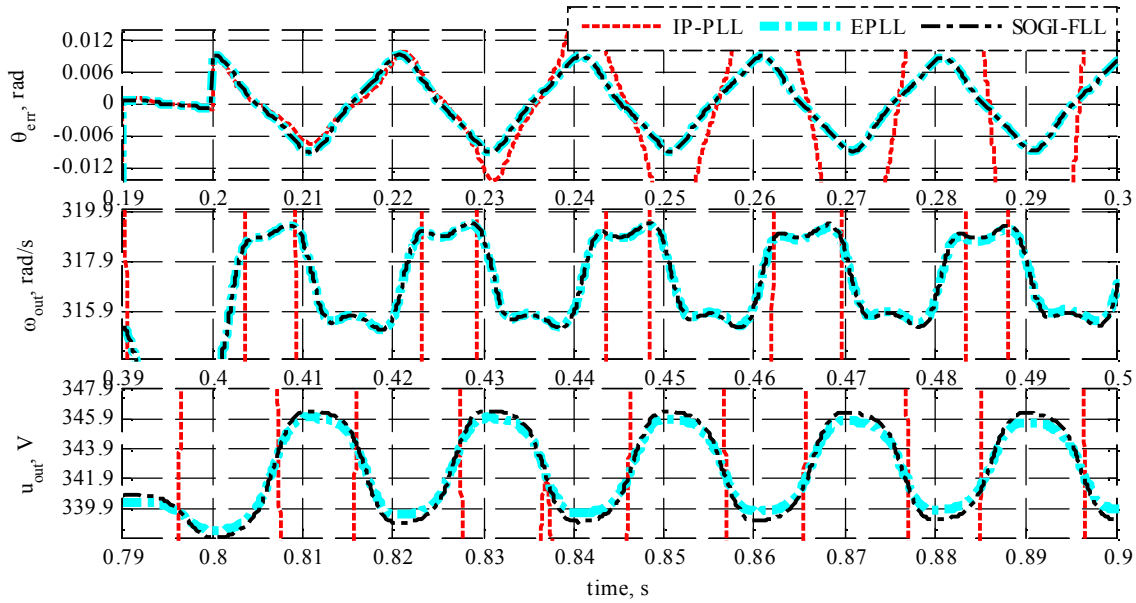

Fig. 12 Simulation results: PLLs testing under small signal step changes for $k_v = 2.82$. Top subplot: shows phase angle response to a phase-angle step of 0.01 rad (at t=0.2s), middle subplot: shows frequency response to a frequency step of 1% (at t=0.4s), Bottom subplot: shows voltage magnitude response to a voltage step of 1% (at t=0.8s). "red" IP-PLL, "cyan" EPLL, "black" SOGI-FLL.

In the next section, the three PLL schemes using the recommended design values for k_v in Table 1 will be tested and compared for large signal disturbances.

6. Large Signal Testing and Performance Comparison of the PLL Schemes

The models for the PLL schemes in Fig. 2, 4, 6 using the design adaptive laws derived in (10), (19) and (27) will be tested by simulation and experimental implementation for large signal disturbances. The recommended values for k_v listed in the last row of Table 1 are used in both simulations and experiments. The disturbances applied are: phase jump ($\Delta\theta_v = 1\,rad$), voltage sag ($\Delta U_v = 80\%$ of the nominal value) and frequency step change ($\Delta\omega_v = 10\%$ of the nominal value). Large disturbance

in grid voltage can cause the PLLs to slip and loose the locking state for one or more cycles. The locking state is maintained attractive under large disturbance by limiting ω_e to be within a band of ±30% from the nominal-value such that $0.7\omega_n < \omega_e < 1.3\omega_n$. Also, the absolute value of u_d is used in the denominator of the adaptive laws (10) and (27). The simulation models are implemented in Matlab/Simulink. The models of the three PLL schemes are also implemented on a 32-bit floating point DSP+FPGA laboratory digital platform equipped with 16 bit A/D converters specially designed for real time control of power electronic systems. All three PLL schemes were running simultaneously and independently in the DSP with a sampling time of 100 μs. A programmable electronic AC power source (Chroma) is used to generate the various types of grid voltage disturbances needed for the experimental validation such as phase jump, voltage sag and frequency step change tests. Because of the existence of an LC filter on the output of the electronic power supply, there is a limitation of how fast/sharp the voltage transients can be replicated and this can explain some of the differences that will be seen in the next subsections between the simulation and the experimental results.

The DSP control algorithm which is executed every sampling time starts by acquiring the supply voltage, then independently calculates the state variables for all three PLL schemes; at the end of every sampling time, all state variables (including the measured supply voltage) are saved into a memory buffer with a sufficient length to store the full response to the disturbance. The content of this memory buffer is later transferred to the PC for visualisation. There is no post processing of data.

The simulation and experimental results of the three PLL schemes under investigation will be compared in the following sections. The simulation results are shown in the left subplots of following figures while the corresponding experimental results are shown in the right subplots.

6.1 Response Following the Phase Jump Test

The PLLs are tested for large and sudden phase jump of 1 rad. The PLLs with the ±30% ω_e limit are tested for phase jump response. The results in Fig. 13 show that all three PLL schemes are stable for a large phase jump disturbance. It is noted that the SOGI-FLL phase tracking is faster simply because the phase angle is estimated using the “arctangent” function of the estimated voltage vector (22) rather

than by direct integration of ω_e which is subject to the ±30% limit. On the other hand, the EPLL and IP-PLL have experienced slow phase-angle tracking responses because of the limits imposed to ω_e that is fed to the integrator. It is also noted that SOGI-FLL has provided smaller disturbance to the estimated voltage magnitude (see bottom subplots of Fig. 13) during the phase jump. The results show that SOGI-FLL could be the most suitable choice for grids that suffer from frequent phase jumps.

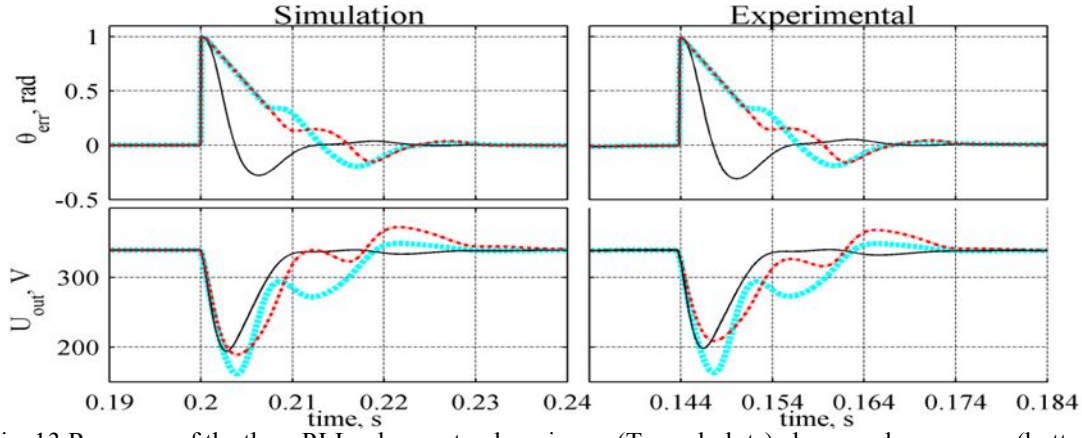

Fig. 13 Response of the three PLL schemes to phase jump: (Top subplots) phase angle response, (bottom subplots) voltage magnitude response. "red" is for IP-PLL, "cyan" is for EPLL and "black" is for SOGI-FLL.

6.2 Response Following the Voltage Sag Test

Modern grid codes require the converters to continue operation even under severe voltage sags to support the grid recovery by injecting reactive current. This will require PLLs to maintain tracking of the grid voltage vector trajectory with minimal error in phase angle estimation. Typically, the voltage sag transient that signals the beginning of a grid fault is the sharpest whilst the grid voltage recovery is a much slower process (slow ramp). The designed PLLs are tested for a large voltage sag of 80% applied at the zero crossing of grid voltage (worst case for voltage estimation) and setting the limit for the estimated angular frequency as $0.7\omega_n < \omega_e < 1.3\omega_n$. The simulation and the experimental results are shown in Fig 14. The voltage tracking of all three PLL schemes is good with no cycle slip. The EPLL have shown the faster voltage magnitude response to the step voltage change. The phase angle error for SOGI-PLL was the largest.

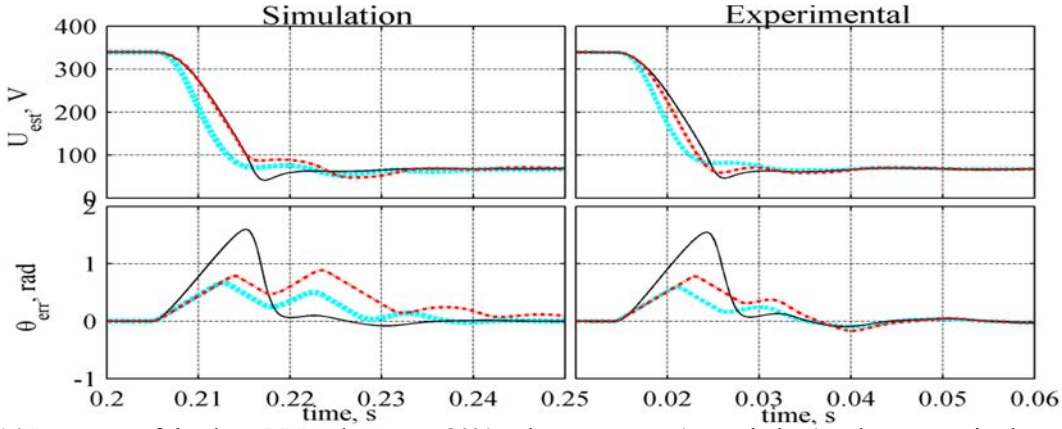

Fig. 14 Response of the three PLL schemes to 80% voltage sag test; (top subplots) voltage magnitude response, (bottom subplots) phase angle response. "red" is for IP-PLL, "cyan" is for EPLL and "black" is for SOGI-FLL.

6.3 Response Following the Frequency Step Change Test

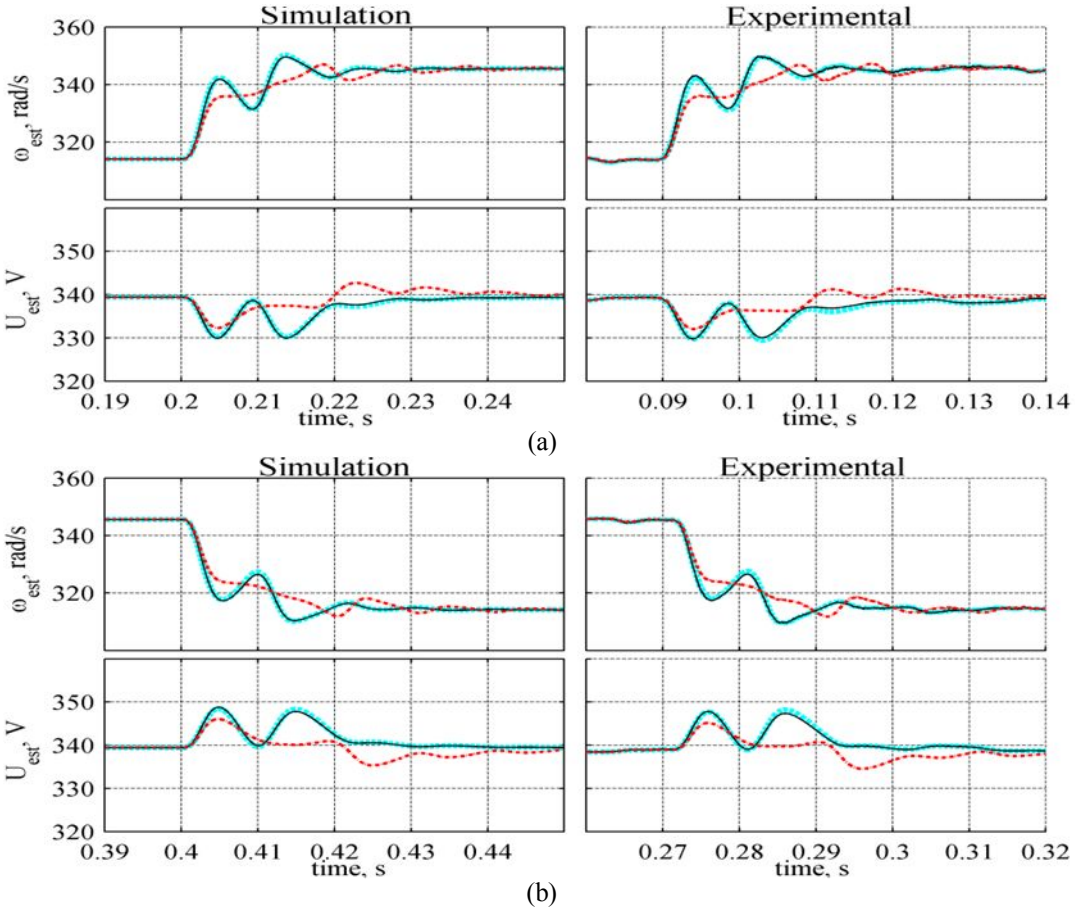

Fig. 15 Response of the three PLL schemes to frequency step change test: a) frequency step increase results, b) frequency step decrease results. (top subplots) frequency response, (bottom subplots) voltage magnitude response. "red" is for IP-PLL, "cyan" is for EPLL and "black" is for SOGI-FLL.

The PLL schemes are tested for a sudden change in grid frequency. The frequency is changed by applying a ±10% step of the nominal value (50Hz). The simulation and the experimental results are shown in Fig. 15a,b. The results show that all PLL schemes are stable but whilst the EPLL and SOGI-

FLL have nearly identical response, the IP-PLL has a slightly slower response. The error in the voltage estimation of the IP-PLL was the smallest.

The conclusion of these tests is that all three PLL schemes perform well under all three large signal disturbances. The SOGI-FLL was able to maintain its good phase angle dynamic response during the phase jump test because the output phase angle is calculated directly from the PLL output voltage vector using arctangent. However, during the voltage sag test which would result in errors in the estimated voltage, it results in the largest phase angle error. The responses of the three PLL schemes to a step change in grid frequency were similar, but with slightly slower dynamics for IP-PLL.

7. Conclusion

The use of Dynamic Phasor Modelling DPM is proposed in this paper to improve the modelling for the purpose of stability analysis and design of three PLL schemes, the single-phase IP-PLL, SOGI-FLL and EPLL PLL. First, the simplified average model usually used in the literature for single phase PLL design and stability analysis has been used to design three PLL schemes to achieve identical dynamic characteristics which when evaluated via simulation, are found to differ significantly.

For this reason, fourth-order DPMs have been developed for the three PLL schemes under study. An analysis of the most predominant eigenvalues is used to determine the stability limits and the recommended design gains which are then validated via simulation for small signal disturbances. The actual small-signal dynamic response of the PLLs was as predicted by the 4^{th}-order DPM eigenvalue analysis.

The final validation of the 4^{th}-order DPM based design of the PLL schemes is achieved by large signal disturbance testing (phase jump, voltage sag and frequency step change) implemented both in simulation and on an experimental digital control platform using (as input) actual voltage disturbances produced by a programmable electronic AC power supply. The SOGI-FLL is found to be more suitable for operation under severe phase jump situations. EPLL on the other hand, had the best response during voltage sag.

Appendix 1

Dynamic Phasor Modelling of Non-linear State Variables

The DPM of the nonlinear terms such as $cos(2\theta)$ and $sin(2\theta)$, e.g. in (5a,b) are given by:

$$\langle sin(m\theta)\rangle_k = \begin{cases} \mp\frac{1}{2}j & \dots\dots for\ k = \pm m \\ 0 \dots\dots\dots\dots otherwise \end{cases} \quad \text{(A1a)}$$

$$\langle cos(m\theta)\rangle_k = \begin{cases} \frac{1}{2} & \dots\dots for\ k = \mp m \\ 0 \dots\dots\dots\dots otherwise \end{cases} \quad \text{(A1b)}$$

For the nonlinear cosine and sine terms function of θ and δ in (5a,b), Taylor expansion method is applied before using the convolution property (4) to determine the DPM. The Taylor expansion for the various nonlinear terms in (5a,b) assuming δ is small are expressed as:

$$\begin{gathered} cos(\delta) \sim 1 \quad ; \quad sin(\delta) \sim \delta \\ cos(\delta + 2\theta) \sim \cos(2\theta) - \delta sin(2\theta) \\ sin(\delta + 2\theta) \sim \sin(2\theta) + \delta cos(2\theta) \end{gathered} \quad \text{(A2)}$$

Then, the Fourier coefficients for the nonlinear terms in (A2) are derived by applying rules (4) and (A1):

$$\begin{gathered} \langle cos(\delta)\rangle_0 = 1 \ ; \ \langle cos(\delta)\rangle_{k\neq 0} = 0 \\ \langle sin(\delta)\rangle_k = \langle \delta \rangle_k \\ \langle cos(\delta + 2\theta)\rangle_2 = 0.5 + 0.5j\langle\delta\rangle_0 - 0.5j\langle\delta\rangle_{-4} \quad \text{and} \quad \langle cos(\delta + 2\theta)\rangle_{k\neq 2} = 0 \\ \langle sin(\delta + 2\theta)\rangle_2 = -0.5j + 0.5j\langle\delta\rangle_0 + 0.5\langle\delta\rangle_{-4} \quad \text{and} \quad \langle sin(\delta + 2\theta)\rangle_{k\neq 2} = 0 \end{gathered} \quad \text{(A3)}$$

The nonlinear term (u_q/u_d) in (e.g. in (10), (27)) is approximated by assuming u_d is mainly a dc quantity with additional small ripple component, (Emadi, 2004) (i.e. $u_d = \langle u_d\rangle_0 + \tilde{u}_d$) and hence (using Taylor expansion method):

$$\frac{u_q}{u_d} \sim u_q\left[\frac{1}{\langle u_d\rangle_0} - \frac{\tilde{u}_d}{(\langle u_d\rangle_0)^2}\right] \sim u_q\left[\frac{2}{\langle u_d\rangle_0} - \frac{u_d}{(\langle u_d\rangle_0)^2}\right] \quad \text{(A4)}$$

where $\tilde{u}_d$ is the sum of the ripple components and $<u_d>_0$ is the DC component of u_d. Then, the convolution property (4) is applied to (A4) to give:

$$\left\langle\frac{u_q}{u_d}\right\rangle_k \sim \left[\frac{2}{\langle u_d\rangle_0}\langle u_q\rangle_k - \frac{1}{(\langle u_d\rangle_0)^2}\langle u_q u_d\rangle_k\right] \quad \text{(A5)}$$

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