Fast Convergence Delayed Signal Cancellation Method for Sequence Component Separation

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***Abstract*— Delayed Signal Cancellation (DSC) is one of the methods used to separate the negative and positive sequence components in unbalanced 3ϕ systems. In this paper a DSC methodology with a fast convergence time is proposed and is shown that an improved separation of the positive and negative sequences is feasible. Experimental results are presented to demonstrate the performance of the proposed methodology.**

***Index Terms*— Delay Signal Cancellation, Symmetrical Components, Control Systems.**

I. Introduction

In several applications it is necessary to obtain the negative and positive sequence components of voltage and current signals. Typical examples are control systems for Low Voltage Ride Through (LVRT) [1], flicker mitigation [2] and phase locked loop implementations [3], [4], etc.

Conventional DSC methods reported in the literature separate the positive and negative sequence components using (1) and (2):

$$\hat{v}_{1\alpha\beta} = \frac{1}{2}\left[\underline{v}_T(t) - j\underline{v}_T(t-\frac{T}{4})\right] \quad (1)$$

$$\hat{v}_{2\alpha\beta} = \frac{1}{2}\left[\underline{v}_T(t) + j\underline{v}_T(t-\frac{T}{4})\right] \quad (2)$$

where $\hat{v}_{1\alpha\beta}$, $\hat{v}_{2\alpha\beta}$ are estimations of the positive and negative sequence signals respectively, $\underline{v}_T$ is the total voltage vector and T is the signal period. The main disadvantage of using (1-2) is that a significant delay (5*ms* for 50Hz) is created in the result. Additionally in digital implementations the ratio $T/(4T_s)$ (where T_s is the sampling period) has to be an integer, which is not always feasible [2]. Moreover, another disadvantage of (1-2) is that a relatively large number of memory positions could be required to store the vector $\underline{v}_T(t-T/4)$. In this work a DSC methodology with a reduced settling time is proposed for separation of the sequence components.

Conventional DSC methods, as well as the fast settling method presented in this paper, are affected by harmonic distortion in the signals [2]. Filtering has to be applied before using (1-2) [3] or a complex generalised DSC (which has a high computational burden) has to be implemented [4]. The filtering or pre-processing stage is considered outside the scope of this paper. Therefore in this work it is assumed that the signals at the DSC input have reduced harmonic distortion. Hence the voltage vector $\underline{v}_T$ is composed of positive and negative sequence components as shown below:

$$\underline{v}_T = v_1 e^{j\omega t+\emptyset_1} + v_2 e^{-j\omega t+\emptyset_2} \quad (3)$$

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Then, using (3) it can be shown that the positive and negative sequence signals can be obtained as:

$$v_{1\alpha\beta} = \frac{1}{2}\left[\underline{v}_T(t) - \frac{j}{\omega}\frac{\partial \underline{v}_T(t)}{\partial t}\right] \quad (4)$$

$$v_{2\alpha\beta} = \frac{1}{2}\left[\underline{v}_T(t) + \frac{j}{\omega}\frac{\partial \underline{v}_T(t)}{\partial t}\right] \quad (5)$$

It is well known that in a digital implementation direct differentiation of the voltage amplifies the noise in $\underline{v}_T$. Therefore an alternative is to use the following expression:

$$\underline{v}_s = \underline{v}_T(\omega t) - e^{-j\theta_d}\underline{v}_T(\omega t - \theta_d) \quad (6)$$

where θ_d is the delay angle. In an experimental implementation this angle is calculated as $\theta_d = 2\pi T/(NT_s)$ where *N* is an integer. Using (3) in (6) (assuming $\emptyset_1 = \emptyset_2 = 0$) the vector $\underline{v}_s$ is obtained as:

$$\underline{v}_s = v_1 e^{j\omega t} + v_2 e^{-j\omega t} - e^{-j\theta_d}\left[v_1 e^{j(\omega t-\theta_d)} + v_2 e^{-j(\omega t-\theta_d)}\right] \quad (7)$$

By simple inspection of (6)-(7) it is concluded that the negative sequence component is cancelled, yielding:

$$\hat{v}_{1\alpha\beta} = \frac{\underline{v}_s}{\left[1-e^{-j2\theta_d}\right]} = \frac{1}{2}\frac{\left[\underline{v}_T(\omega t) - e^{-j\theta_d}\underline{v}_T(\omega t-\theta_d)\right]\left(1-e^{j2\theta_d}\right)}{[1-2\cos(2\theta_d)]} \quad (8)$$

where $\hat{v}_{1\alpha\beta}$ is an estimation of the positive sequence signal. The negative sequence component of the signal is estimated using:

$$\hat{v}_{2\alpha\beta} = \frac{1}{2}\frac{\left[\underline{v}_T(\omega t) - e^{j\theta_d}\underline{v}_T(\omega t-\theta_d)\right]\left(1-e^{-j2\theta_d}\right)}{[1-2\cos(2\theta_d)]} \quad (9)$$

It can be shown that (8)-(9) are equivalent to (4)-(5) when $\theta_d \to 0$. Using (8-9) the implementation of the proposed fast DSC is shown in Fig. 1. The time delay of NT_s seconds corresponds to a delay angle of θ_d rads. Using $\theta_d = \pi/2$ the conventional DSC of (1-2) is obtained. Notice that the use of $\theta_d > \pi/2$ is also possible, which could be an alternative for sequence separation with very noisy signals (i.e. delays >5*ms*).

Using Fig. 1 and (8)-(9), the estimation (in the α-β frame) of the sequence components can be obtained using the equations shown in Table 1. For compactness, $\underline{v}_T^{\theta_d}$ stands for

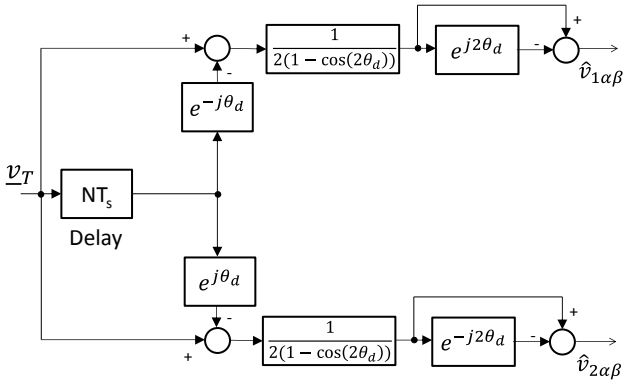

Fig.1. Proposed fast DSC

TABLE I. CALCULATIONS OF THE POSITIVE AND NEGATIVE SEQUENCE VOLTAGES USING (8) AND (9).

$$\hat{v}_{1\alpha}=\frac{(v_{\alpha T}-v_{\alpha T}^{\theta_d}\cos\theta_d-v_{\beta T}^{\theta_d}\sin\theta_d-(v_{\alpha T}-v_{\alpha T}^{\theta_d}\cos\theta_d-v_{\beta T}^{\theta_d}\sin\theta_d)\cos 2\theta_d+(v_{\beta T}-v_{\beta T}^{\theta_d}\cos\theta_d+v_{\alpha T}^{\theta_d}\sin\theta_d)\sin 2\theta_d)}{2(1-\cos 2\theta_d)}$$

$$\hat{v}_{1\beta}=\frac{(v_{\beta T}-v_{\beta T}^{\theta_d}\cos\theta_d+v_{\alpha T}^{\theta_d}\sin\theta_d-(v_{\beta T}-v_{\beta T}^{\theta_d}\cos\theta_d+v_{\alpha T}^{\theta_d}\sin\theta_d)\cos 2\theta_d-(v_{\alpha T}-v_{\alpha T}^{\theta_d}\cos\theta_d-v_{\beta T}^{\theta_d}\sin\theta_d)\sin 2\theta_d)}{2(1-\cos 2\theta_d)}$$

$$\hat{v}_{2\alpha}=\frac{(v_{\alpha T}-v_{\alpha T}^{\theta_d}\cos\theta_d+v_{\beta T}^{\theta_d}\sin\theta_d-(v_{\alpha T}-v_{\alpha T}^{\theta_d}\cos\theta_d+v_{\beta T}^{\theta_d}\sin\theta_d)\cos 2\theta_d+(v_{\beta T}-v_{\beta T}^{\theta_d}\cos\theta_d-v_{\alpha T}^{\theta_d}\sin\theta_d)\sin 2\theta_d)}{2(1-\cos 2\theta_d)}$$

$$\hat{v}_{2\beta}=\frac{(v_{\beta T}-v_{\beta T}^{\theta_d}\cos\theta_d-v_{\alpha T}^{\theta_d}\sin\theta_d-(v_{\beta T}-v_{\beta T}^{\theta_d}\cos\theta_d-v_{\alpha T}^{\theta_d}\sin\theta_d)\cos 2\theta_d-(v_{\alpha T}-v_{\alpha T}^{\theta_d}\cos\theta_d+v_{\beta T}^{\theta_d}\sin\theta_d)\sin 2\theta_d)}{2(1-\cos 2\theta_d)}$$

$\underline{v}_T(\omega t-\theta_d)$ and the subscripts '*1*', '*2*' stand for positive and negative sequence respectively. Notice that *N* samples of the signal $\underline{v}_T(t)$ have to be stored in the digital processor memory for the implementation of this fast convergence DSC algorithm.

II. EXPERIMENTAL IMPLEMENTATION

The fast DSC algorithm proposed in this work has been experimentally tested. A TMS320C6713 DSP augmented with an FPGA board has been used to estimate the sequence components using the equations depicted in Table I. A data acquisition system with a sampling frequency of 10kHz is used in this application. Three Hall-effect voltage transducers are used to measure the grid voltages. A programmable AMETEK power source is used to generate type *D* voltage dips. The output of this power source is regulated to 110-V_{rms} at 50Hz.

In the DSP implementations the proposed fast DSC has been programmed with delays (in parallel) of *T*/4 (conventional DSC [2]), *T*/8, and *T*/40 (*T*=20*ms*). Fig. 2 shows the experimental results for a voltage dip of type *D*. As shown in Fig. 2a, at t≈20*ms* voltages v_{an} and v_{cn} decrease by 50% and v_{bn} decreases by 75% of their previous values. In Fig. 2b the estimated negative sequence voltages are shown. Notice the relatively high peak achieved by the *T*/40 estimation. This is produced by the numerical implementation of $(\partial\underline{v}(t)/\partial t)$ using a 500μs time delay (see (9)). Fig. 2c shows an amplified view of the dip. Notice that the conventional DSC takes 5*ms* to converge to the correct negative sequence voltage. The *T*/40

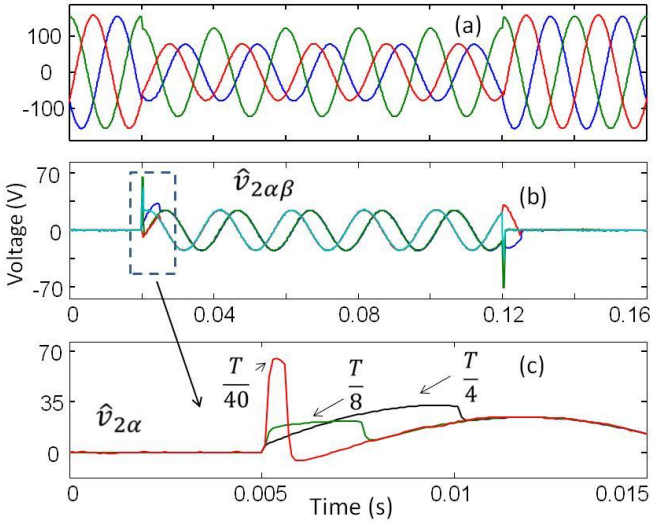

Fig. 2. Experimental results. a) v_{an}, v_{bn} and v_{cn} for a dip D grid-fault. b) α-β negative sequence components. c) Amplified view of 2b) for $\hat{v}_{2\alpha}$.

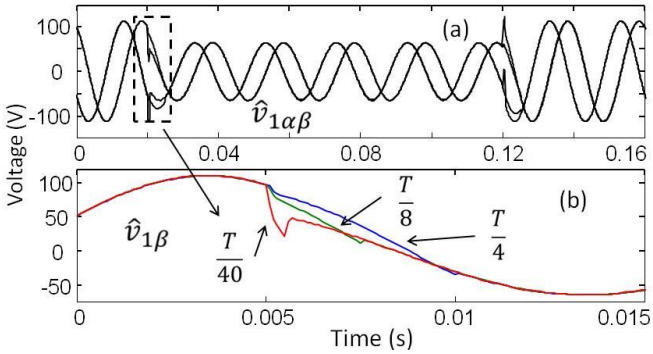

Fig. 3. a) α-β positive sequence components corresponding to the test shown in Fig.2a . b) Amplified view of a) for $\hat{v}_{1\beta}$

DSC converges very fast in almost 500μs (5 samples). Fig. 3a shows the estimation of the positive sequence component for the voltages depicted in Fig. 2a. In Fig. 3b an amplified view (corresponding to the dashed box of Fig. 3a) of $\hat{v}_{1\beta}$ is shown. Again the convergence is very fast for a delay time of *T*/40. The estimator with a delay time of *T*/8 settles down in ≈2.5*ms* with a reduced overshoot. Therefore, for a given application a compromise between the minimum value of θ_d, the noise level and the maximum overshoot allowed can be reached.

III. CONCLUSIONS

An improved DSC method with fast settling time has been proposed in this work. The implementation is based on the equations given in Table I. Unlike the conventional methodology the proposed DSC can estimate the positive/negative sequence signals using a small fraction of a cycle. For instance in this work the method has been tested for θ_d>9° (500μs) with good performance. As anticipated from (4)-(5) for smaller values of θ_d, more noise and overshoot are expected because the numerical implementation of $\partial\underline{v}(t)/\partial t$ is implicit in (8-9). Therefore, for a particular application a compromise between noise, overshoot and minimum θ_d value has to be reached.

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