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Electrical and thermal failure modes of 600 V p-gate GaN HEMTs

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ABSTRACT

A study of electrical and thermal failure modes of 600 V p-doped GaN HEMTs is presented, which focuses on the investigation of short-circuit limitations. The electrical failure mode seems to be an electrical field breakdown in the structure which is caused by excessive carrier concentration, rather than primary thermal generated. Accordingly, a thermal failure mode is observed, which features a distinctive behaviour and seems to be similar to schottky-gate HEMTs. Concerning the electrical failure mode, a specific p-gate HEMT short-circuit safe operating area (SCSOA) is presented as a novelty. However, a short-circuit capability of up to 520 V can be achieved, regarding the design of the gate-drive circuit.

1. Introduction

A significant milestone for power electronic applications is related to the efficiency and robustness of the semiconductor devices. In the recent years the high electron mobility transistor (HEMT) based on an AlGaN/GaN heterojunction, has been proven to be sufficient for this aim. In order to ensure the operation robustness, the device featured safe operating area (SOA) has to be investigated.

A recent study on the short-circuit safe operating area (SCSOA) of a depletion-mode HEMT [1] refers the short-circuit failure to an avalanche generation of accumulated holes under the gate at high electrical fields. Additionally, a reduction of the withstand capability has been observed, according to an increasing drain-source voltage and gate-bias condition. A similar behaviour has been investigated for enhancement-mode HEMTs [2] and is introduced as a p-gate type specific gate-bias dependence (GBD) [3].

In another investigation of SCSOA on enhancement-mode HEMTs [4] an increase of gate-current I_G prior to failure has been indicated, which was proven to be sufficient to cause a thermal runaway [5].

In this paper, a comprehensive study is carried out, to investigate further the origin of the short-circuit (SC) failure as well as its limiting characteristics. In Section 2 the test set-up within the conditions of the study is shown. The investigation of short-circuit robustness and their electrical limiting characteristics are presented in Section 3. Accordingly, the temperature limiting characteristics is investigated in Section 4. Summarizing the observations, a novel proposal of a specific p-gate HEMT short-circuit safe operating area (SCSOA) is presented in Section 5. Finally, with the results of the SCSOA an improved SC capability is achieved and shown in Section 6.

2. Set-up and conditions

The device under test (DUT) is a 600 V p-doped gate (p-gate) AlGaN/GaN HEMT fabricated on a Si substrate. A simplified cross-section of the DUT is depicted in Fig. 1. The aim of the p-doped layer is to ensure an enhancement-mode operation [6] and realised in AlGaN (p-AlGaN) to prevent by hole injection [7] the switching from causing a current collapse.

The test set-up to investigate the SC capability of the DUT is shown in Fig. 2. It consists of a gate-driver in conjunction with a modulation network of the gate signal that eventually is applied on the DUT gate terminal. The voltage V_{DS} for the SC is provided by an external low inductive linked source in the power-path, which can be assumed as constant due to a large stabilisation capacitance. The

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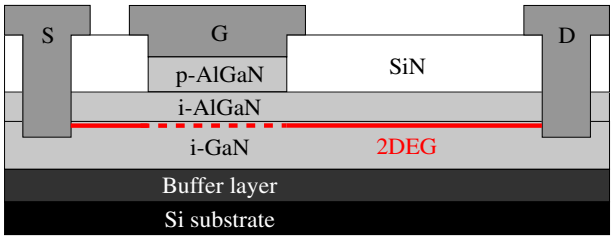

Fig. 1. Simplified cross-section of the investigated transistor. The gate prevents a p-doped AlGaN layer for the enhancement-mode operation.

duration of the SC t_{SC} can be adjusted on the gate-driver by applying a voltage-pulse of variable time, which transmits an equivalent power-pulse on the gate to set the DUT in on-state. Due to feedback related effects during the destructive SC failure, the gate-loop is galvanic (optical) decoupled to prevent the driver from destruction.

For operation in on-state, the HEMT exhibits a forward current I_G due to the p-gate structure. The respective value is set by an appropriate gate-resistance R_G. Furthermore, the driver-voltage V_{DD}, together with the voltage drop over R_G, is used to set the gate-source voltage V_{GS} and the gate-bias condition, respectively. In order to ensure a gate-bias condition a modulation-network is inserted as part of the gate-drive circuit, comparable with the usage in a power electronic application. Optimised transient on- and off-state conditions of the DUT can be achieved, due to the intended use of the branch with R_{RC} and C_{RC} in parallel to R_G.

In order to specify the DUT failure mechanism, a parametric study on the influence of the gate-drive circuit on the SC capability is carried out, which is summarised in Table 1. The influence of a V_{GS} has already been investigated [1], therefore the voltage for all the conditions is defined as nominal $V_{GS} = 3.5$ V. The on-state performance of the DUT predicts an insignificant reduction, regarding the range of nominal bias currents I_G. In order to investigate the transferability on the SC capability, the condition A features a high value within the range, while the condition B features a low. The transient performance is mainly determined by the design of the gate-driver. Therefore, the condition C exhibits a lower drive-voltage V_{DD} and slew-rate (SR), rather than the conditions A and B. In order to prevent comparability, the resistance R_G is adjusted to keep a similar low current I_G. Condition C_{opt} corresponds to an optimisation of the modulation-network branch containing R_{RC} and C_{RC}, which is detailed in Section 6.

3. Electrical limiting characteristics

For the investigation of the electrical short-circuit limiting characteristics the gate-source voltage is fixed in which a distinction occurs, according to the applied drain-source voltage. This behaviour, within its impact, is known as the gate-bias dependence (GBD) [3] and therefore it is not considered in the following observations.

The experimental study is carried out as the investigation of the maximum voltage and time duration withstand capability of the DUT, by applying a SC in the proposed conditions (see Table 1). In a typical power electronic application, the requirement for the DUTs is to withstand a SC within 50% of the nominal breakdown-voltage for a duration of 10 µs.

Table 1
Parametric variation test conditions. If not further indicated, the to R_G paralleled branch is parametrised $R_{RC} = 50\Omega$ and $C_{RC} = 1740$pF. The parametrisation is chosen in accordance to an optimised application design.

Condition		A	B	C	C_{opt}
Drive-voltage	V_{DD}[V]	12	12	5	5
Drive-slew-rate	SR[kV/µs]	50	50	20	20
Gate-resistance	$R_G[\Omega]$	470	4.7k	980	980
RC-resistance	$R_{RC}[\Omega]$	50	50	50	50
RC-capacitance	$C_{RC}[pF]$	1740	1740	1740	330

3.1. Influence of the steady-state gate-current

For the investigation of maximum voltage withstand capability, the SC duration is kept to the required time, whereas the voltage is increased (10 V/step) until a failure occurs. The waveforms of the SC current I_D, comparing the conditions A and B, for the maximum withstand capability are depicted in Fig. 3. In condition A, a failure-voltage of $V_{DS} = 350$ V is observed, whereas B is capable to withstand up to $V_{DS} = 400$ V. As is can be observed, the DUT withstands the required duration until a certain voltage, whereas a slightly increase leads in all conditions to a DUT destruction within a few hundred nanoseconds.

The decrease in the saturation value of the current I_D for an increase of the voltage V_{DS}, is related to the impact of mobility temperature degradation caused by an to excessive power dissipation. However, the impact of a thermal dependent failure can be neglected, due to the dramatical decrease in the withstand time. A lower initial drain-current peak leads the condition C to withstand voltages up to $V_{DS} = 450$ V, whereas a not negligible limitation related to the gate-current I_G can be observed. The impact of I_G is dedicated to the discussion of the SCSOA in Section 5.

The gate-currents, for a similar operation at $V_{DS} = 300$ V and $t_{SC} = 10$ µs, are depicted in Fig. 4. Due to the particular aims of the conditions, the steady-state values of the currents I_G differ one magnitude of order, within a respective difference in the initial peak value.

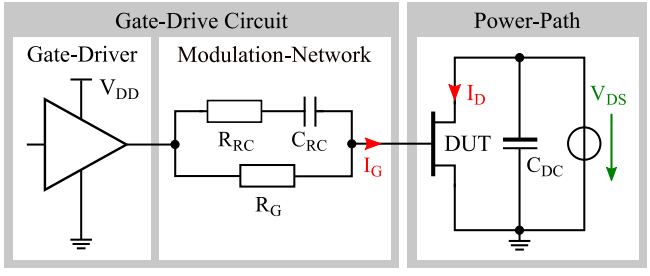

Fig. 2. Test set-up, composed of: a galvanic (optical) decoupled gate-driver, a modulation-network of the gate-signal (typ. GaN app.), and a power-path with the device under test (DUT).

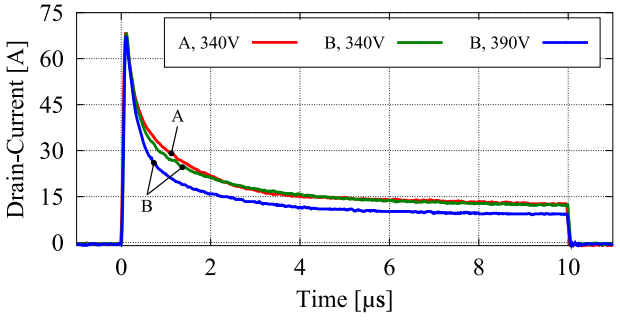

Fig. 3. Experimental results of maximum voltage withstand capability, comparing conditions A and B before failure. The exceeded capability of B refers to the steady-state value of the gate-, rather than the drain-current.

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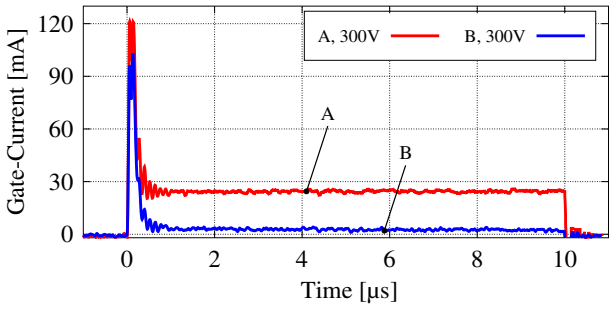

Fig. 4. Experimental waveforms of the bias-conditions for a similar operation point, comparing conditions A and B. The waveforms of the gate-source voltages are approximately identical.

3.2. Influence of the initial current peaks

For the investigation of maximum time withstand capability, the SC voltage is kept to the required value, whereas the duration is increased (5 µs/step) until a failure occurs. The waveforms of the SC current I_D, as a comparison between the conditions B and C for the maximum withstand capability are depicted in Fig. 5 (top). In condition B a failure-time of $t_{SC} = 40$ µs is observed, whereas C is capable to withstand durations more than an order of magnitude higher. Furthermore, no failure-time can be observed in condition C whereat for clarity the presented duration is reduced.

The main distinction between these two conditions is the initial peak of the current I_D. For clarification purposes, Fig. 5 (bottom) depicts the zoom into the initial waveforms. However, if the current peak is kept below a given critical value, the DUT can withstand very long pulse-widths. Additionally, it can be mentioned that the failure of B is not related to a thermal issue, because the withstand capability within the associated energy is much higher in condition C.

The waveforms of the gate-bias conditions, for a similar operation at $V_{DS} = 300$ V and $t_{SC} = 10$ µs, are depicted in Fig. 6. The initial peak of the drain-current is related to the peak value of the voltage V_{GS}, see

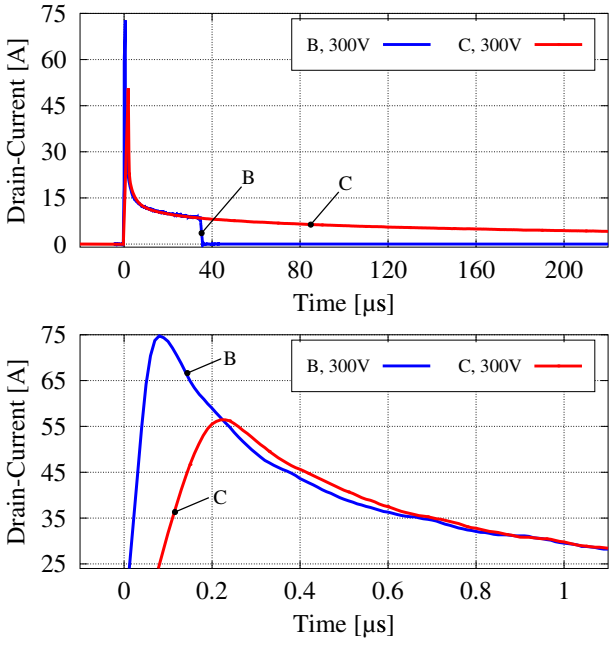

Fig. 5. Experimental results of maximum time withstand capability, comparing the conditions B and C before failure. Although an equivalent peak of condition A, due to the gathered observations in Section 3.1, the capability is less than B.

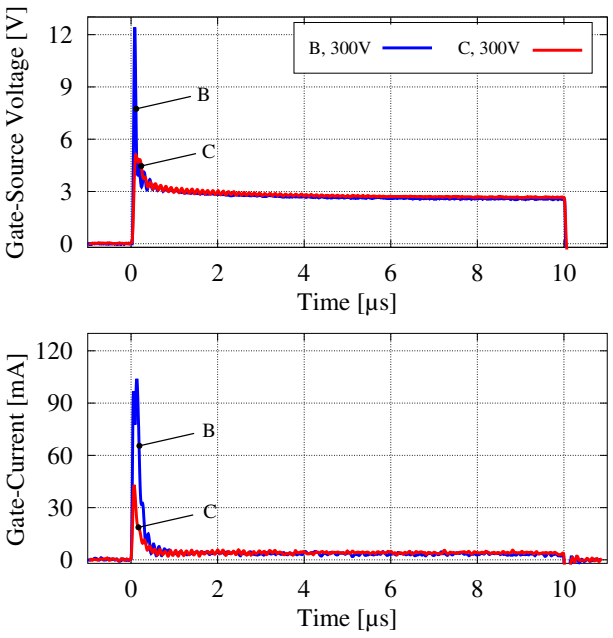

Fig. 6. Experimental waveforms of the bias-conditions for a similar operation-point, comparing condition B and C.

Fig. 6 (top). Furthermore, the amount of the current peak depends strongly on the drive-voltage V_{DD} and the respective slew-rate (SR) of the gate-driver, see Table 1. A further lowering in the initial peak of the current I_G is achieved, due to a reduction in case of condition C, see Fig. 6 (bottom).

4. Thermal limiting characteristics

During the investigation of temperature limiting characteristics, the DUT overcomes the major issue of the drain-current peak limitation, see Section 3.2. For an increase of ambient-temperature T_A the current I_D decreases respective to the mobility temperature degradation, which leads to lower peak values. Consequently, the maximum voltage withstand capability tends to raise, which is increasing in case of condition C, up to $V_{DS} \geq 500$ V. The ambient-temperature is kept below $T_A \leq 500$ K, in order to ensure the thermal stability of the die attached materials.

In the range of the proposed V_{DS} and T_A limitations, the test conditions T_1 to T_3 are used for the determination of temperature limitation. These conditions differ slightly in the power-dissipation as well as the initial temperature of the DUT junction T_J. A temperature limitation can be observed, wherefore Fig. 7 implies the significant waveforms and Fig. 8 the appropriate temperature T_J. The temperature is simulated numerically with a 3D temperature simulator, as detailed in [5].

However, by reaching a critical temperature, which has been proven to be significant in terms of schottky-gate HEMTs [8], the gate-current increases dramatically, see Fig. 7 (bottom). Due to the operating mode of the gate-driver (see Section 2), an appropriate decrease of the current I_D can be observed, see Fig. 7 (top). The temperature related failure exhibits in a permanent short of the gate-source path and features a distinctive behaviour in comparison with the electrical related failure (see Section 3).

5. Short-circuit safe operating area

According to the observations of Section 3.2, the SC capability is mainly limited by the initial peak values of the currents I_D and I_G.

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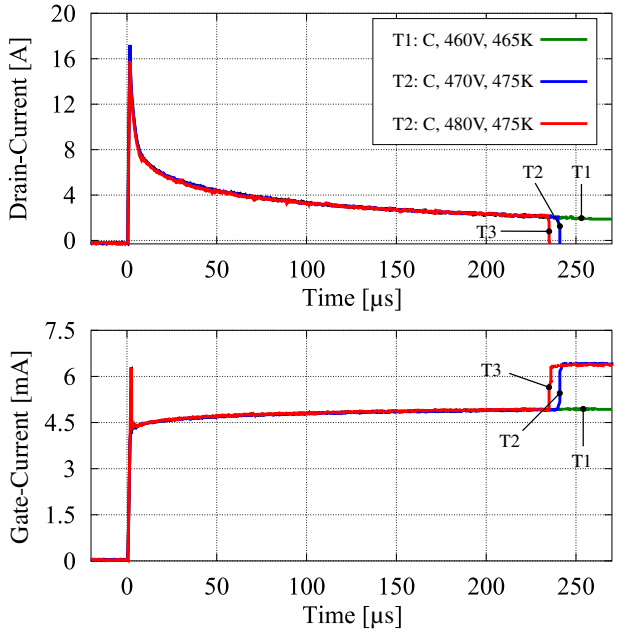

Fig. 7. Experimental results of the thermal failure mode, comparing condition C in a variation of power dissipation and ambient-temperature.

Their charge density's influence the magnitude of the electrical field. Hitting the value of the critical field strength leads to an electrical breakdown within the structure, accompanied by avalanche carrier generation and virtually instantaneous catastrophic device failure. This critical value is estimated by the results of the measurements and in sufficient accordance to the maximum electrical field strength of AlGaN $E_F = 5.5$ MV/cm [9].

The current I_D is provided by a physical-based compact model approach, which considers the surface-potential and therefore the intrinsic charges in the AlGaN/GaN HEMT structure [10]. In the p-gate structured HEMT the effect of hole injection occurs according to [11]. The holes can be injected from the gate electrode into the GaN channel (2DEG), when the voltage V_{GS} exceeds the bandgap energy of GaN [12]. Therefore, the amount and density of the injected holes in the proposed model is defined as the gate-current peak related carrier density:

$$N_h = \frac{1}{W \cdot L \cdot d} \int_{t_0}^{t_1} \frac{i_g(t) - i_{g,dc}}{q} dt \quad (1)$$

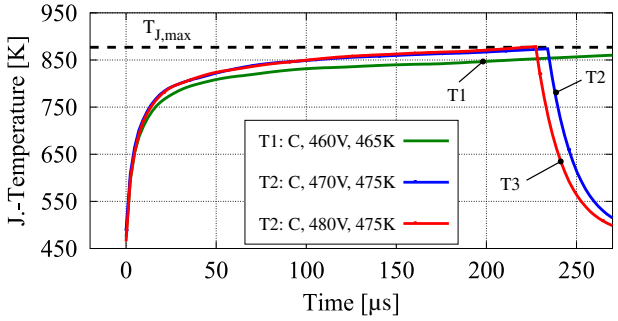

Fig. 8. Simulated results of the respective junction-temperature according to the thermal-failure mode, presented in Fig. 7. The estimate is conducted with usage of a numerical 3D temperature simulator.

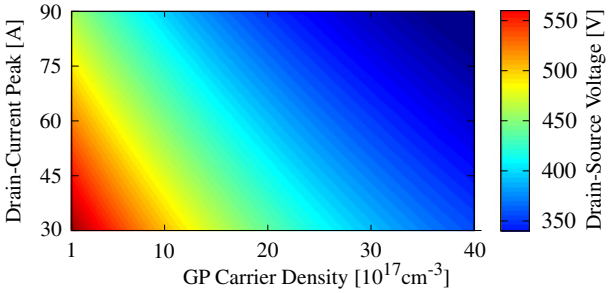

Fig. 9. Short-circuit safe operating area (SCSOA) of p-gate HEMTs. Achievable drain-source voltage in the respective condition of the drain-current peak and the gate-current peak (GP) related carrier density.

The amount can be determined by the integral of the current I_G with the fraction of the elementary charge (q), neglecting the steady-state value $I_{G,DC}$. The time t_0 and t_1 correlates to $V_{GS} \geq E_{G,GaN}$, which is approximately accurate for considering only the current I_G above the steady-state value (e.g. Fig. 6). For the determination of the density, the gate-width W and -length L as well as the i-AlGaN layer-thickness d are defined by the geometric parametrisation of the model. The geometric parametrisation of the model accord to Uemoto et al. [7] and is valid due to the output- and transfer-characteristics of the investigated DUT.

The proposed short-circuit safe operating area (SCSOA), specific for a p-gate HEMT, is illustrated in Fig. 9. Regarding the observations of Section 3.2 and Fig. 6 respectively, the amount of the drain-current peak cannot be set independently to the initial bias-condition. However, the SCSOA illustrates an independent variation of the drain- and gate-current induced equivalent carrier density's (see Eq. (1)), within the respective achievable drain-source voltage. The SCSOA is established in accordance to the used conditions and is validated with the presented failure-points.

Within the observations, the SC withstand capability strongly depend on the design of the gate-driver. The investigated drivers accord to M1: $V_{DD} = 12$ V, SR $= 50$ V/µs and M2: $V_{DD} = 5$ V, SR $= 20$ V/µs.

Apart from the design of the gate-driver, the carrier density N_h can be further adjusted by the parametrisation of the modulation-network branch which consists of R_{RC} and C_{RC}. Therefore, the network is analysed theoretically and depicted in Fig. 10. The analytical model constitutes an inverse laplace-transformation, for the calculation of the gate-current $i_g(t)$ time-domain response, according to the respective gate-driver pulse $V(s)$ and modulation-network impedance $Z(s)$ in frequency-domain.

$$i_g(t) = \mathcal{L}^{-1}\left(V(s) \cdot Z(s)^{-1}\right) \quad (2)$$

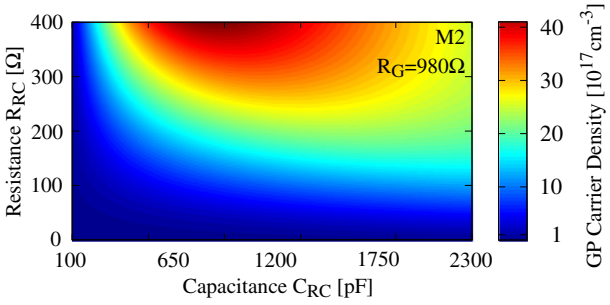

Fig. 10. Simulated result of the originated gate-current peak (GP) related carrier density. The density can be adjusted regarding the parametrisation of the modulation-network branch containing R_{RC} and C_{RC}.

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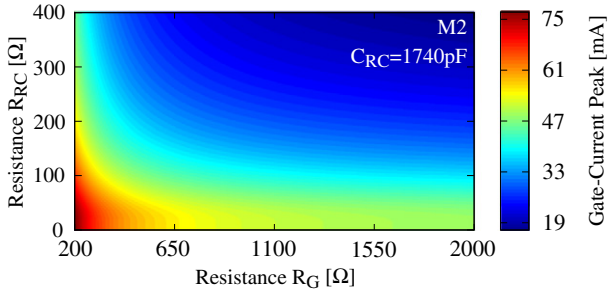

Fig. 11. Simulated result of the originated gate-current peak value. The value can be adjusted regarding the parametrisation of the modulation-network resistance R_G and R_{RC}.

Therefore, $V(s)$ is described as a trapezoidal signal which consists of a superposition of two ramps with a defined slope regarding the gate-driver specific drive-slew-rate SR. The respective drive-voltage V_{DD} is set by a time-shifted compensation. The impedance $Z(s)$ considers the paralleled branches of R_G and R_{RC} with C_{RC}. The determination is conducted by using a fixed value of R_G in accordance with the condition C, see Table 1.

Regarding the functionality of the gate-drive circuit (see Section 2) and the observations of Fig. 6, the amount of current I_D is related to the bias-condition. The initial peak of the current I_G occur in a respective value of the voltage V_{GS}, which leads to an appropriate peak of the current I_D. The amount of the initial peak of the current I_G can be adjusted to the parametrisation of the resistances in the modulation-network, see Fig. 11. Therefore, the values of the resistance R_G accord the nominal range of the current I_G. For the determination, a fixed value of C_{RC} is chosen according to the presented measurement conditions, see Table 1.

However, the initial peak of the current I_D can be adjusted by the parametrisation of the resistances R_G and R_{RC}. The determination of R_{RC} together with C_{RC}, define the RC time constant. The initial peak of the current I_G, together with the RC time constant, define the hole injection. Consequently, the SC capability of the DUT can be adjusted regarding to the parametrisation of the components in the modulation-network and the design of the gate-driver.

6. Design related limitation

According to the prediction of the SCSOA in Section 5, an improvement of the SC capability is achieved. Therefore, the maximum voltage withstand capability of the condition C in two optimised variations are depicted in Fig. 12. The bias-conditions for the optimisations, at a similar operation point, are shown in Fig. 13. In comparison to the origin bias-condition of C (see Fig. 6) a reduction of the initial peak current I_G is achieved, due to a lowering of the RC-capacitance $C_{RC} = 330$ pF. This leads to a reduction of voltage

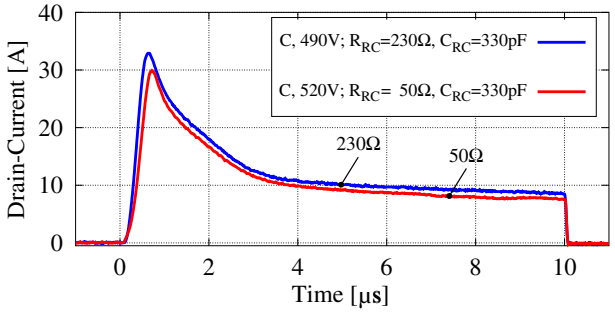

Fig. 12. Experimental results of maximum voltage withstand capability, comparing condition C in two different optimisations before failure.

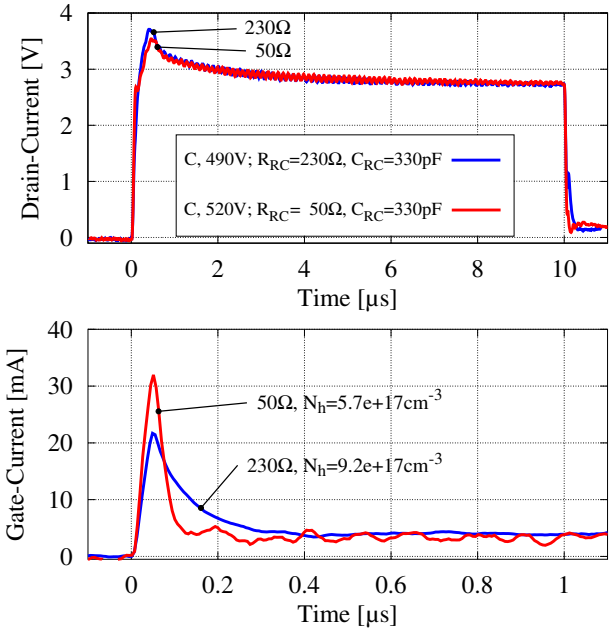

Fig. 13. Experimental waveforms of the bias-conditions for a similar operation-point, comparing condition C in two different optimisations.

V_{GS} and an appropriate decrease of the hole injection, respectively. The initial peak of the current I_D is reduced, due to the peak reduction of the voltage V_{GS}. Conspicuously, for a certain threshold of the I_G peak the respective peak of I_D cannot be reduced. For an approximately identical peak of I_D, a superior improvement of the condition with the lower carrier density N_h can be achieved, which confirms the validity of the SCSOA. However, the SC capability is mainly limited by the carrier density N_h with an underlying limitation of the peak of I_G and its respective peak of I_D.

The investigated conditions regarding Table 1, within their maximum achieved SC capability, are depicted in Table 2. Therefore, the design related bias-conditions and their impact are specified. The presented failures are a subject of a low quantity investigation with a statistical stray of $V_{DS} = \pm 10$ V and $t_{SC} = \pm 5$ µs.

7. Conclusion

Two distinct failure modes have been identified. The first is of a merely electrical nature and strongly depends on the charge accumulation phenomena within the device structure, mainly affected by the bias and operational current values, and to some extent by the voltage bias. If the value of accumulated charge is kept below a minimum threshold (e.g., by optimised design of the driver or operating temperature), then the device features extreme robustness and the thermal failure is only reached for very long pulses and very large values of the drain-source bias voltage.

Table 2
Impact of the design related SC capability with their significant bias-conditions. The failure-time is determined with $V_{DS} = 300$V and the failure-voltage with $t_{SC} = 10$ µs. The (dc) indexed values accord to a nominal dimensioning for the DUT operation.

Condition		A	B	C	C_{opt}
GS voltage (dc)	V_{GS}[V]	3.5	3.5	3.5	3.5
GS voltage (peak)	V_{GS}[V]	12.5	12.5	5.5	3.7
Gate-current (dc)	I_G[mA]	25	2.5	4.2	4.2
Gate-current (peak)	I_G[mA]	125	105	42	32
GP carrier density	$N_h[\frac{10^{17}}{cm^3}]$	25.4	21.8	13.6	5.7
Drain-current (peak)	I_D[mA]	75	75	52	30
Failure-time	t_{SC}[µs]	20	40	None	None
Failure-voltage	V_{DS}[V]	350	400	450	520

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References

[1] X. Huang, D.Y. Lee, V. Bondarenko, A. Baker, D.C. Sheridan, A.Q. Huang, B.J. Baliga, Experimental study of 650 V Algan/Gan HEMT short-circuit safe operating area (SCSOA), In: 2014 IEEE 26th International Symposium on Power Semiconductor Devices IC'S (ISPSD), 2014, pp. 273–276. http://dx.doi.org/10.1109/ISPSD.2014.6856029.

[2] M. Landel, C. Gautier, D. Labrousse, S. Lefebvre, [131] Experimental study of the short-circuit robustness of 600 V E-mode GaN transistors, Microelectron. Reliab. 64 (2016) 560–565. http://dx.doi.org/10.1016/j.microrel.2016.07.042.

[3] T. Oeder, A. Castellazzi, M. Pfost, Experimental study of the short-circuit capability of a 600 V normally-off P-gate Gan HEMT, In: 2017 IEEE 29th International Symposium on Power Semiconductor Devices IC'S (ISPSD), 2017, accepted for publication.

[4] C. Abbate, F. Iannuzzo, G. Busatto, Thermal instability during short circuit of normally-off AlGaN/GaN {HFETs}, Microelectron. Reliab. 53 (9-11) (2013) 1481–1485. European Symposium on Reliability of Electron Devices, Failure Physics and Analysis. http://dx.doi.org/10.1016/j.microrel.2013.07.119.

[5] M. Mocanu, C. Unger, M. Pfost, P. Waltereit, R. Reiner, Thermal stability and failure mechanism of schottky gate algan/gan HEMTs, IEEE Trans. Electron Devices 64 (3) (2017) 848–855. http://dx.doi.org/10.1109/TED.2016.2633725.

[6] E.A. Jones, F. Wang, B. Ozpineci, Application-based review of Gan HFETs, 2014 IEEE Workshop on Wide Bandgap Power Devices and Applications, 2014, pp. 24–29. http://dx.doi.org/10.1109/WiPDA.2014.6964617.

[7] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, D. Ueda, Gate injection transistor (GIT) - a normally-off algan/gan power transistor using conductivity modulation, IEEE Trans. Electron Devices 54 (12) (2014) 3393–3399. http://dx.doi.org/10.1109/TED.2007.908601.

[8] C. Unger, M. Mocanu, M. Pfost, P. Waltereit, R. Reiner, Pulse robustness of Algan/Gan HEMTs with Schottky- and MIS-gates, In: 2017 IEEE 29th International Symposium on Power Semiconductor Devices IC'S (ISPSD), 2017, accepted for publication.

[9] X. Gang, E. Xu, N. Hashemi, Z. Bo, F.Y. Fu, W.T. Ng, An algan/gan HEMT with a reduced surface electric field and an improved breakdown voltage, Chin. Phys. B 21 (8) (2012) 086105. http://stacks.iop.org/1674-1056/21/i=8/a=086105.

[10] S. Khandelwal, Y.S. Chauhan, T.A. Fjeldly, Analytical modeling of surface-potential and intrinsic charges in algan/gan HEMT devices, IEEE Trans. Electron Devices 59 (10) (2012) 2856–2860. http://dx.doi.org/10.1109/TED.2012.2209654.

[11] H. Chonan, T. Ide, X.-Q. Shen, M. Shimizu, Effect of hole injection in algan/gan HEMT with GIT structure by numerical simulation, Phys. Status Solidi C 9 (3-4) (2012) 847–850. http://dx.doi.org/10.1002/pssc.201100330.

[12] L.Y. Su, F. Lee, J.J. Huang, Enhancement-mode gan-based high-electron mobility transistors on the si substrate with a p-type gan cap layer, IEEE Trans. Electron Devices 61 (2) (2014) 460–465. http://dx.doi.org/10.1109/TED.2013.2294337.

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