Improved performance of InSe field-effect transistors by channel encapsulation

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Abstract

Due to the high electron mobility and photo-responsivity, InSe is considered as an excellent candidate for next generation electronics and optoelectronics. In particular, in contrast to many high-mobility two-dimensional (2D) materials, such as phosphorene, InSe is more resilient to oxidation in air. Nevertheless, its implementation in future applications requires encapsulation techniques to prevent the adsorption of gas molecules on its surface. In this work, we use a common lithography resist, poly(methyl methacrylate) (PMMA) to encapsulate InSe-based field-effect transistors (FETs). The encapsulation of InSe by PMMA improves the electrical stability of the FETs under a gate bias stress, and increases both the drain current and electron mobility. These findings indicate the effectiveness of the PMMA encapsulation method, which could be applied to other 2D materials.

1. Introduction

The isolation of graphene and other two-dimensional (2D) materials has raised expectations for a revolution in electronics and optoelectronics [1-3]. However, graphene has a zero band gap, which prevents its use in many applications. Thus, continuous efforts have turned to explore other 2D materials with a band gap, such as transitional metal dichalcogenides (TMDs) [4-6], black phosphorus [7, 8], and III-VI group semiconductors [9, 10]. Among the III-VI semiconductors, InSe has emerged as a promising material due to its direct band gap over a range of layer thicknesses and light in plane electron effective mass (m^*_{InSe}= 0.14m_0) [11]. High performance few-layered InSe photodetectors were reported by Tamalampudi *et al*, demonstrating a responsivity that is four orders of magnitude higher than that of MoS_2 and graphene phototransistors [12]. Also, Feng *et al* have reported multilayer InSe field-effect transistors (FETs) on SiO_2/Si substrate, reaching field-effect mobilities of 162 $cm^2V^{-1}s^{-1}$ at room temperature[13]. These mobilities can be further increased up to 1055 $cm^2V^{-1}s^{-1}$ by using poly(methyl methacrylate) (PMMA)/Al_2O_3 as dielectric layer rather than SiO_2 due to a significant reduction of carrier scattering by surface charged impurities and polar phonon scattering [14].

Although layered InSe exhibits outstanding optical and electrical properties [12, 15, 16], and better resilience to oxidation under ambient conditions than many other 2D materials, the electrical stability and performance of InSe-based devices can be affected by the exposure and interaction of the InSe surface to chemical species in air, such as water or oxygen [17]. For example, Balakrishnan *et al* have shown that the oxidation of InSe surface in air can be induced by both thermal and photo annealing, which converts a few surface layers of InSe into In_2O_3, thus forming an InSe/In_2O_3 heterostructure [18]. On the other hand, Feng *et al* have demonstrated that InSe-based FETs become unstable under a gate bias stress due to the absorption (desorption) of oxygen and water on the InSe surface[19]. Thus, the development of techniques for improving the stability in air of InSe-based devices is critical to future applications.

PMMA is an ideal encapsulation dielectric to isolate the channel of FETs from air. Being readily available as a standard electron-beam lithography resist of high purity, it can be dissolved easily into organics and can be used to form thin films by a simple spin-coating process [4, 20]. Furthermore, PMMA has been used to modify the surface states of semiconductors, resulting in improved performances, as shown by Bao *et al* who have used PMMA to

encapsulate the channel of MoS_2-based FETs, thus increasing the carrier mobility [4]. In this work, we use PMMA as the channel encapsulation to improve the performance of InSe-based FETs. The electrical stability of InSe FETs is investigated in response to a constant gate bias stress (±40 V) for 300 s under ambient conditions. The encapsulation of InSe by PMMA enables the fabricated FETs with higher mobility and significantly improved electrical stability. This work offers a convenient method to improve the mobility and stability of 2D-material-based devices.

2. Methods and results

We use InSe-based FETs with and without encapsulation of the InSe layer by PMMA, as shown in figures 1(a) and 1(b). The InSe layers are prepared from bulk Bridgman-grown rhombohedral γ-InSe by mechanical exfoliation using adhesive tape and deposited on SiO_2/*p*-Si substrates for the fabrication of InSe FETs. The primitive unit cell of γ-InSe contains three layers, each consisting of four closely-packed, covalently bonded, atomic sheets in the sequence Se-In-In-Se; within each layer plane, atoms form hexagons (figure 1(c)) [21]. The source and drain electrodes, Ti/Au (10/40 nm), are defined by shadow masks and deposited by electron-beam evaporation. For the channel encapsulation, 200 nm PMMA (950K, 4.5 wt. %) is spin-coated onto the FETs and baked at 110 °C for 2 hours. A typical optical image of the unencapsulated InSe FET is shown in the right part of figure 1(c). This has a channel length L = 50 μm and width W = 45 μm. The corresponding thickness t of the InSe layer is approximately t = 40 nm, as measured by atomic-force microscopy (AFM) (figure 1(d)).

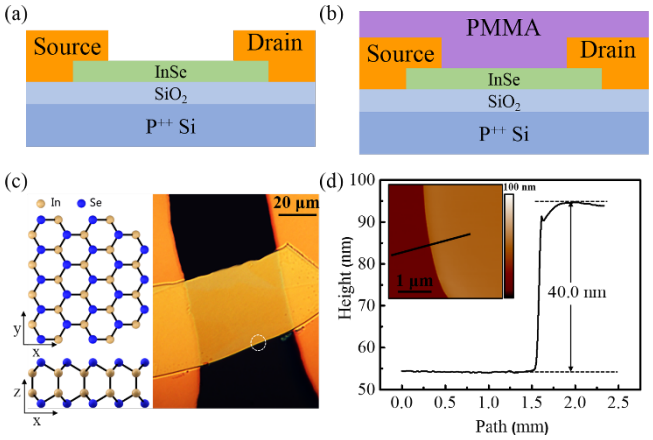

Figure 1. Schematic of back-gate InSe-based FETs (a) without or (b) with PMMA as channel encapsulation,

respectively. (c) Left: crystal structure of InSe; Right: optical image of an InSe FET. (d) The thickness of InSe is about 40 nm, as measured by AFM. The inset is the AFM image.

The electrical performance of the fabricated back-gated FETs is characterized with a standard electrical probe station and an Agilent 2902A semiconductor analyzer. As shown by the transfer and output characteristics in figures 2a and 2b, the InSe FET shows n-type behaviour. For transfer characteristics, as shown in figure 2(a), the V_{GS} sweep takes 16 s (0.75 V/step), from V_{GS} = -30 to +30 V at V_{DS} of 0.1 V, and another 16 s for the sweep back from V_{GS} = +30 to -30 V. Following the encapsulation of InSe by PMMA, the *on* current increases from 2.0 to 3.4 μA at V_{GS} = +30 V, and the width of the hysteresis loop decreases from 8.2 to 4.0 V. For the output characteristics, the current I_{DS} is measured for V_{DS} swept from 0 to +30 V while stepping V_{GS} from -30 to +30 V in increments of 12 V, as shown in figure 2(b). The I_{DS}-V_{DS} curves indicate that fairly good ohmic contacts form between InSe and the Ti source/drain electrodes (Ti has a work function work of 4.3 eV, slightly smaller than that of InSe around 4.6 eV).[9,13] The field-effect mobility of the InSe FETs can be extracted from the transfer curve by the equation [14, 21, 22]:

$$\mu = \frac{L}{W}\frac{1}{C_{\mathrm{i}}V_{\mathrm{DS}}}\frac{\mathrm{d}I_{\mathrm{DS}}}{\mathrm{d}V_{\mathrm{GS}}} \qquad (1)$$

where C_{i} is the capacitance of SiO_2 with a thickness of 300 nm per unit area (1.15×10^{-8} Fcm^{-2}) [23]. We find that with PMMA encapsulation, the electron mobility increases from 186 to 220 $cm^2V^{-1}s^{-1}$. A similar improvement is measured on other FETs in which the InSe layer thickness ranges from 20 to 70 nm. As shown in figure 2(c), with PMMA encapsulation, all the InSe FETs reveal an improved mobility. In particular, the mobility increases as the layer thickness of InSe increases from 20 to 30 nm, and decreases as the InSe thickness increases from 30 to 70 nm, consistent with a previous report [14]. For thinner layered InSe, the interaction distance between charged impurities on the substrate and free carriers in InSe is smaller, which enhances carrier scattering and reduces the mobility. For thicker InSe layers, because the source and drain electrodes are contacted only directly to the top InSe layer, electron transport into the bottom layers involves additional interlayer resistors, resulting in a lower mobility of the FETs [24].

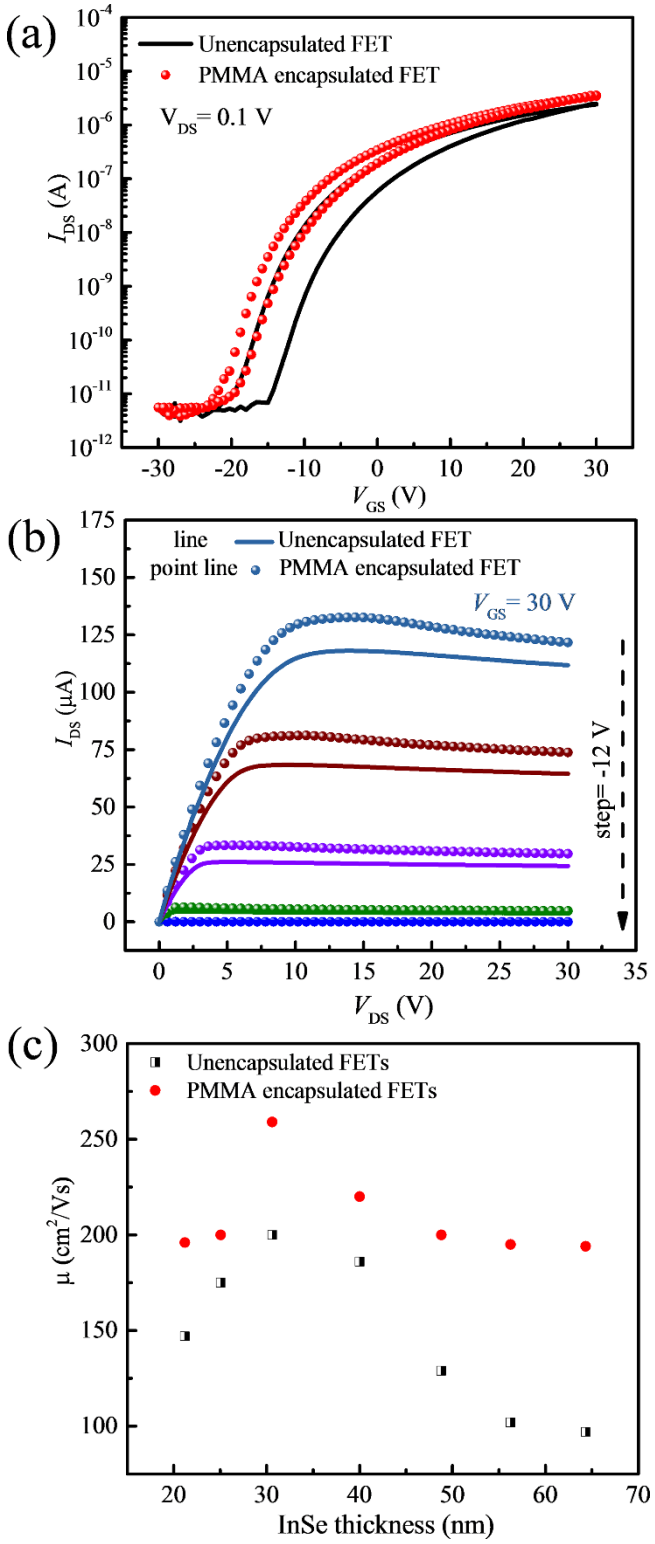

Figure 2. (a) Transfer characteristics and (b) output characteristics of InSe FETs with and without PMMA at a drain

voltage V_{DS}= 0.1 V under ambient conditions, respectively. (c) Dependence of the field-effect electron motility of InSe FETs on the InSe layer thickness.

The electrical stability of the as-fabricated FETs is investigated by applying a constant gate bias stress (±40 V) for 300 s. The transfer characteristic curves are measured immediately after the bias stress at V_{DS} = 1 V and at regular time intervals. For the unencapsulated FET, after applying a gate bias stress of -40 V, the drain current increases from 26 to 30 μA at V_{GS} = +30 V, and the threshold voltage shifts in the negative direction (ΔV_{th} = -7.4 V), as shown in figure 3(a). After applying a gate bias stress of 40 V, the drain current decreases from 25 to 13 μA at V_{GS} = +30 V, and the threshold voltage increases (ΔV_{th} = 4.3 V), as shown in figure 3(b). For the PMMA encapsulated FET, after applying a gate bias stress of -40 V, the drain current increases from 31 to 34 μA at V_{GS} = +30 V, and the threshold voltage reduces (ΔV_{th} = -3.5 V), as shown in figure 3(c). On the other hand, for a gate bias stress of +40 V, the drain current decreases from 30 to 20 μA at V_{GS} = +30 V, and the threshold voltage increases (ΔV_{th} = 2.5 V), as shown in figure 3(d). Figures 3(e) and 3(f) compare the changes of the threshold voltage and mobility for each measurement with the values of the pre-biased devices. The PMMA encapsulated FET shows much smaller shifts of the threshold voltage for both positive and negative gate bias stress than those for the FET without the encapsulation. Also, after PMMA encapsulation, the mobility is less sensitive to the gate bias stress, as shown in figure 3(f). Without PMMA encapsulation, the mobility decreases by 22.3% from 76 to 59 $cm^2V^{-1}s^{-1}$ after a positive gate bias stress, and increases by 14.4% from 76 to 87 $cm^2V^{-1}s^{-1}$ after a negative gate bias stress. With PMMA encapsulation, the mobility decreases by 13.0% from 100 to 87 $cm^2V^{-1}s^{-1}$ after a positive gate bias stress, and increases by 5.0% from 100 to 105 $cm^2V^{-1}s^{-1}$ after a negative gate bias stress. As such, our results demonstrate an improved stability of InSe FETs by using PMMA for the encapsulation.

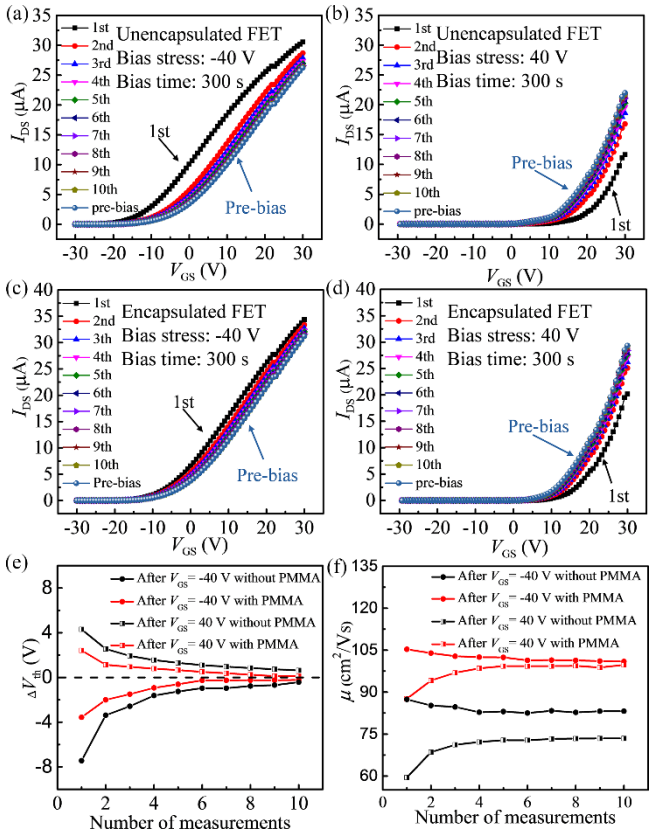

Figure 3. Transfer characteristics of an unencapsulated InSe FET measured before applying the gate bias and 10 transfer curves at V_{DS}=1 V measured after (a) -40 V and (b) +40 V gate bias stress for 300 s under ambient conditions. Transfer characteristic of encapsulated InSe FET measured before applying the gate bias and 10 transfer curves at V_{DS}=1 V measured after (c) -40 V and (d) +40 V gate bias stress for 300 s under ambient conditions. (e) Threshold voltage shifts of unencapsulated and encapsulated InSe FETs for each measurement compared with the value of pre-bias curves. (f) Field-effect mobility of unencapsulated and encapsulated InSe FETs for each measurement in linear regime following the gate bias stress.

3. Discussion

To discuss the results, we consider the energy band diagram in figure 4. Under the ideal condition, without gate bias stress, electron accumulation forms at each Ti/InSe interface because the electron affinity of InSe (~4.5 eV) is higher than the work function of Ti (~4.3 eV) [25], as shown in figure 4(a). However, under ambient condition, the InSe channel surface is subject to the adsorption of water and oxygen molecules in air [26-29]. For example, Bickley *et al.* studied photoadsorption at rutile surface, indicating that the adsorption oxygen could capture electrons from the

rutile surface and form negatively charged species ($O_{2(s)}^{-}$) through the reaction:

$$O_{2(g)} + e^{-} \leftrightarrow O_{2(s)}^{-} \qquad (2)$$

where $O_{2(s)}^{-}$ donates the adsorbed oxygen on the surface and $O_{2(g)}$ donates the neutral oxygen in gas form [26]. Such adsorption of oxygen has also been observed in IGZO [28-30] and MoS2 [31] devices. Lopes *et al.* investigated the performance a-IGZO TFT with water vapor exposure. The drain current exhibited an apparent increasing after water vapor exposure [29]. Fuh *et al.* further studied the effect and summarized the reaction as:

$$H_2O_{(g)} \leftrightarrow H_2O_{(s)}^{+} + e^{-} \qquad (3)$$

where $H_2O_{(s)}^{+}$ donates the adsorbed water molecule and $H_2O_{(g)}$ donates the neutral water molecule [28], meaning that an adsorbed water molecule can be positively charged on the channel surface by releasing an electron.

Here, such adsorption/desorption of oxygen and water is also expected to occur on the InSe channel, while the contact region is not effected by such adsorption/desorption[32]. Under ambient conditions, pristine defects and dangling bonds on the surface of InSe can facilitate absorption of oxygen or water from air, thus forming charged species that affect the band bending and the electrical transport [29, 33]. With a positive gate bias stress, the increase of electron concentration facilitates the adsorption of oxygen and desorption of water, resulting in a more negative surface and hence an increase of electrons depletion in the InSe channel. In this case, the electrons have to traverse a higher channel-depletion-induced barrier during the transport process, as shown in figure 4(b), causing a decline of drain current and a positive shift of threshold voltage. On the other hand, with a negative gate bias stress, the decrease of electron concentration in the FET facilitates desorption of oxygen and adsorption of water, resulting in a release of electrons from oxygen and water. As a result, the channel depletion-induced barrier decreases, making the transport of electrons easier, as shown in figure 4(c). This causes the increase of drain current and the negative shift of threshold voltage. By using PMMA to isolated InSe from air, the surface states of InSe channel is reduced, resulting in reduced scattering and increased mobility. Furthermore, owing to the isolation from water or oxygen in ambient air, InSe FETs become more stable under both positive and negative bias stresses as observed in figures 3(e) and 3(f).

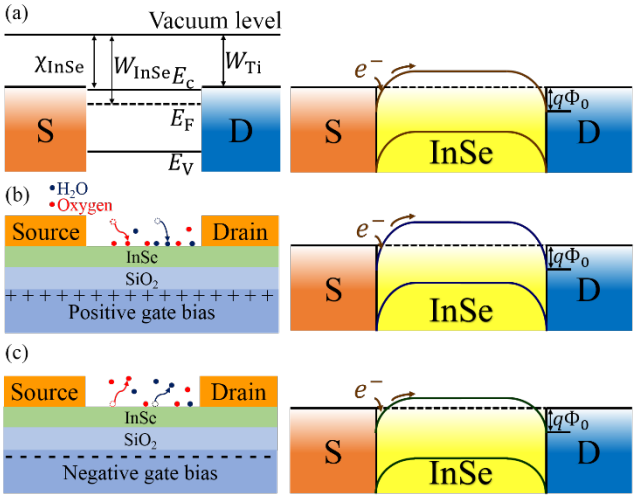

Figure 4. Schematic energy band diagrams of InSe FETs at V_{GS} = 0 V under (a) ideal condition, (b) positive gate bias stress, and (c) negative gate bias stress conditions.

4. Conclusion

In conclusion, PMMA has been used for the channel encapsulation to improve the performance of back-gated InSe FETs in air. A number of devices with InSe channel of different thicknesses have been fabricated. All devices showed increased mobility as well as bias-stress stability after the encapsulation. The effect can be explained by the isolation of InSe channel surface from adsorption of oxygen and water in air. Our study may have implications for a better design of functional nanodevices based on two-dimensional layered materials for a wide range of device structures.

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SYG201616), Special Foundation for Postdoctoral Innovation Projects of Shandong Province (NO. 201602017), the EU Graphene Flagship Project 604391, and the National Academy of Sciences of Ukraine.

6. REFERENCES

[1] Novoselov K S, Jiang D, Schedin F, Booth T J, Khotkevich V V, Morozov S V and Geim A K 2005 Two-dimensional atomic crystals *Proceedings Of the National Academy Of Sciences Of the United States Of America* **102** 10451-3

[2] Rogers J A, Lagally M G and Nuzzo R G 2011 Synthesis, assembly and applications of semiconductor nanomembranes *Nature* **477** 45-53

[3] Geim A K and Grigorieva I V 2013 Van der Waals heterostructures *Nature* **499** 419-25

[4] Bao W, Cai X, Kim D, Sridhara K and Fuhrer M S 2013 High mobility ambipolar MoS2 field-effect transistors: Substrate and dielectric effects *Applied Physics Letters* **102** 042104

[5] Chuang H J, Tan X, Ghimire N J, Perera M M, Chamlagain B, Cheng M M, Yan J, Mandrus D, Tomanek D and Zhou Z 2014 High mobility WSe2 p- and n-type field-effect transistors contacted by highly doped graphene for low-resistance contacts *Nano Lett* **14** 3594-601

[6] Fang H, Tosun M, Seol G, Chang T C, Takei K, Guo J and Javey A 2013 Degenerate n-doping of few-layer transition metal dichalcogenides by potassium *Nano Lett* **13** 1991-5

[7] Pan Y, Dan Y, Wang Y, Ye M, Zhang H, Quhe R, Zhang X, Li J, Guo W, Yang L and Lu J 2017 Schottky Barriers in Bilayer Phosphorene Transistors *ACS Appl Mater Interfaces* **9** 12694-705

[8] Buckley J, De Salvo B, Deleruyelle D, Gely M, Nicotra G, Lombardo S, Damlencourt J F, Hollinger P, Martin F and Deleonibus S 2005 Reduction of fixed charges in atomic layer deposited Al2O3 dielectrics *Microelectronic Engineering* **80** 210-3

[9] Mudd G W, Svatek S A, Ren T, Patane A, Makarovsky O, Eaves L, Beton P H, Kovalyuk Z D, Lashkarev G V, Kudrynskyi Z R and Dmitriev A I 2013 Tuning the bandgap of exfoliated InSe nanosheets by quantum confinement *Advanced materials* **25** 5714-8

[10] Tu H and Kelley D F 2006 Photoinduced direct electron transfer from InSe to GaSe semiconductor nanoparticles *Nano Lett* **6** 116-22

[11] Bandurin D A, Tyurnina A V, Yu G L, Mishchenko A, Zólyomi V, Morozov S V, Kumar R K, Gorbachev R V, Kudrynskyi Z R, Pezzini S, Kovalyuk Z D, Zeitler U, Novoselov K S, Patanè A, Eaves L, Grigorieva I V, Fal'ko V I, Geim A K and Cao Y 2016 High electron mobility, quantum Hall effect and anomalous optical response in atomically thin InSe *Nature Nanotechnology* **12** 223-7

[12] Tamalampudi S R, Lu Y-Y, Kumar U R, Sankar R, Liao C-D, Moorthy B K, Cheng C-H, Chou F C and Chen Y-T 2014 High Performance and bendable few-layered InSe photodetectors with broad spectral response *Nano letters* **14** 2800-6

[13] Feng W, Zhou X, Tian W Q, Zheng W and Hu P 2015 Performance improvement of multilayer InSe transistors with optimized metal contacts *Phys Chem Chem Phys* **17** 3653-8

[14] Feng W, Zheng W, Cao W and Hu P 2014 Back gated multilayer InSe transistors with enhanced carrier mobilities via the suppression of carrier scattering from a dielectric interface *Advanced materials* **26** 6587-93

[15] Lei S, Wen F, Ge L, Najmaei S, George A, Gong Y, Gao W, Jin Z, Li B, Lou J, Kono J, Vajtai R, Ajayan P and Halas N J 2015 An Atomically Layered InSe Avalanche Photodetector *Nano Lett* **15** 3048-55

[16] Lei S, Ge L, Najmaei S, George A, Kappera R, Lou J, Chhowalla M, Yamaguchi H, Gupta G, Vajtai R, Mohite A D and Ajayan P M 2014 Evolution of the Electronic Band Structure and Efficient Photo-Detection in Atomic Layers of InSe *Acs Nano* **8** 1263-72

[17] Politano A, Chiarello G, Samnakay R, Liu G, Gurbulak B, Duman S, Balandin A A and Boukhvalov D W 2016 The influence of chemical reactivity of surface defects on ambient-stable InSe-based nanodevices *Nanoscale* **8** 8474-9

[18] Balakrishnan N, Kudrynskyi Z R, Smith E F, Fay M W, Makarovsky O, Kovalyuk Z D, Eaves L, Beton P H and Patanè A 2017 Engineering p–n junctions and bandgap tuning of InSe nanolayers by controlled oxidation *2d Mater* **4** 025043

[19] Feng W, Zheng W, Chen X, Liu G and Hu P 2015 Gate Modulation of Threshold Voltage Instability in Multilayer InSe Field Effect Transistors *ACS Appl Mater Interfaces* **7** 26691-5

[20] Kim W, Javey A, Vermesh O, Wang Q, Li Y and Dai H 2003 Hysteresis Caused by Water Molecules in Carbon Nanotube Field-Effect Transistors *Nano Letters* **3** 193-8

[21] Sucharitakul S, Goble N J, Kumar U R, Sankar R, Bogorad Z A, Chou F C, Chen Y T and Gao X P 2015 Intrinsic Electron Mobility Exceeding 10(3) cm(2)/(V s) in Multilayer InSe FETs *Nano Lett* **15** 3815-9

[22] Kang K, Xie S E, Huang L J, Han Y M, Huang P Y, Mak K F, Kim C J, Muller D and Park J 2015 High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity *Nature* **520** 656-60

[23] Zhang B, Li H, Zhang X, Luo Y, Wang Q and Song A 2015 Performance regeneration of InGaZnO transistors with ultra-thin channels *Applied Physics Letters* **106** 093506

[24] Das S, Chen H Y, Penumatcha A V and Appenzeller J 2013 High performance multilayer MoS2 transistors with scandium contacts *Nano Lett* **13** 100-5

[25] Lang O, Pettenkofer C, Sánchez-Royo J F, Segura A, Klein A and Jaegermann W 1999 Thin film growth and band lineup of In2O3 on the layered semiconductor InSe *Journal of Applied Physics* **86** 5687-91

[26] Bickley R I and Stone F S 1973 PHOTOADSORPTION AND PHOTOCATALYSIS AT RUTILE SURFACES .1. PHOTOADSORPTION OF OXYGEN *Journal Of Catalysis* **31** 389-97

[27] Park W, Park J, Jang J, Lee H, Jeong H, Cho K, Hong S and Lee T 2013 Oxygen environmental and passivation effects on molybdenum disulfide field effect transistors *Nanotechnology* **24** 095202

[28] Fuh C-S, Sze S M, Liu P-T, Teng L-F and Chou Y-T 2011 Role of environmental and annealing conditions on the passivation-free in-Ga–Zn–O TFT *Thin Solid Films* **520** 1489-94

[29] Lopes M E, Gomes H L, Medeiros M C R, Barquinha P, Pereira L, Fortunato E, Martins R and Ferreira I 2009 Gate-bias stress in amorphous oxide semiconductors thin-film transistors *Applied Physics Letters* **95** 063502

[30] Liu P-T, Chou Y-T and Teng L-F 2009 Charge pumping method for photosensor application by using amorphous indium-zinc oxide thin film transistors *Applied Physics Letters* **94** 242101

[31] Qiu H, Pan L J, Yao Z N, Li J J, Shi Y and Wang X R 2012 Electrical characterization of back-gated bi-layer MoS2 field-effect transistors and the effect of ambient on their performances *Applied Physics Letters* **100** 123104

[32] Cho K, Park W, Park J, Jeong H, Jang J, Kim T Y, Hong W K, Hong S and Lee T 2013 Electric stress-induced threshold voltage instability of multilayer MoS2 field effect transistors *Acs Nano* **7** 7751-8

[33] Chen Y-C, Chang T-C, Li H-W, Chen S-C, Lu J, Chung W-F, Tai Y-H and Tseng T-Y 2010 Bias-induced oxygen adsorption in zinc tin oxide thin film transistors under dynamic stress *Applied Physics Letters* **96** 262104