New Modulation Scheme for Bidirectional quasi Z-Source Modular Multilevel Converters

Fatma A. Khera*,† Christian Klumpner* Pat W Wheeler*
*Power Electronics, Machines and Control Research Group,
University of Nottingham, Nottingham, UK
† Electrical Power and Machines Engineering Department, Tanta University, Egypt
E-mail: fatma.khera@nottingham.ac.uk, klumpner@ieee.org

Keywords: quasi Z-source, modular multilevel converter.

Abstract

This paper proposes a dedicated modulation scheme for a bidirectional quasi Z-source modular multilevel converter (BqZS-MMC). The operation principle and a suitable PWM method are proposed. The relation between the modulation index and shoot-through duty ratio is derived. A formula for calculating the required value of quasi Z-source capacitance is given. The simulation results presented in the paper validate the operation and the performance of the proposed topology.

1 Introduction

Multilevel inverters (MLIs) are preferred due to their attractive features compared to two-level voltage source inverters (VSIs) [1] such as better AC voltage quality, low voltage stress on semiconductors, possibility to produce significantly higher voltages than a single switch voltage rating. The modular multilevel converter (MMC) is a relatively new competitive concept which has been proposed in 2002 [2]. It provides several features such as modularity, voltage and power scalability and failure management capability in the case of device failures [3]. These advantages favour the MMC for various applications, such as interface to high voltage direct current (HVDC) [4] and flexible AC transmission (FACTs) systems[5], medium-voltage (MV) motor drives applications [3] and connecting renewable energy sources such as photovoltaics [6] and wind energy system [7] to MV grids. The output voltage of most renewable energy sources fluctuates with working conditions, therefore having a converter that can adapt to these fluctuation by being able not only to step down but also to step up the voltage in order to regulate the voltage at the DC-link terminals may be quite useful. Power converter topologies based on the use of impedance network concept have been proposed in [8] which proposes the implementation of a quasi Z-source modular multilevel converter. The basic structure of the quasi Z-source inverter (qZSI) as proposed in [9] is shown in Fig. 1. The operating principle of the qZS network relies on producing a short circuit (shoot-through) at inverter DC-link terminals in order to increase the stored energy in the inductors that is later transferred in the qZS capacitors and finally, this extra voltage adds up to the DC source voltage and provides voltage boosting capability.

There are two operation modes for qZS-network which are shoot-through (ST) and non-shoot-through mode (NST). In ST mode, the DC-link terminals are shorted by gating both the upper and lower devices of at least one inverter leg, which forces the qZS diode *D* to become reverse biased and therefore behave like an open circuit as shown in Fig. 2a. Hence, the stored energy in the capacitors begins to transfer into the inductors. In NST mode, the inverter operates by producing active and null voltage states [11] and then *D* will be forward biased as shown in Fig. 2b, the stored energy in the inductors begins to transfer to the load, which sees $V_{po}=V_{c1}+V_{c2}$ as its DC-link voltage, and qZS capacitors begin to charge.

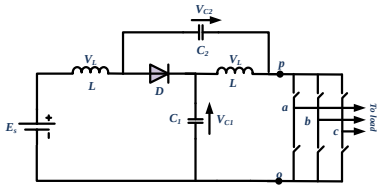

Fig. 1: Equivalent circuit of quasi Z-source inverter (qZSI)

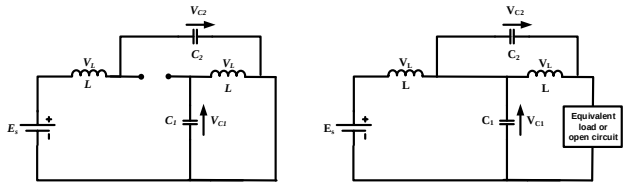

Fig. 2: Equivalent circuit of qZSI, a) shoot-through mode, b) non shoot-through mode

Ref [8] proposed the integration of qZS-network with a single phase MMC to provide voltage boost capability. The proposed circuit faces some limitations which were identified in the same paper and a solution was proposed by modifying the qZS-MMC to be a bidirectional one (BqZS-MMC).

This paper gives a detailed circuit analysis of the proposed BqZS-MMC. The equivalent circuit of the qZS-MMC with the proper implemented sinusoidal pulse width modulation (SPWM) boosting scheme is presented which can be extended to any number of output voltage levels. The relation between modulation index and shoot-through duty ratio for any number of voltage levels is derived. A guideline for choosing the value of qZS capacitance is proposed. Finally, the operation and analysis of the proposed modulation scheme is validated using results simulation from a MATLAB/PLECS model.

2 Operation principles of the bidirectional quasi Z-Source modular multilevel converter

The topology of a single-phase quasi Z-source modular multilevel converter (MMC) is shown in Fig. 3. The MMC leg consists of the upper and lower arms where each arm consists of series-connected sub-modules (SMs), and an arm inductor (L_o). Each sub-module has a half-bridge inverter configuration

with one DC-link capacitor. The two switches (S_a, and S_{ax}) in SM are controlled by complementary gating signals. When S_a is on, SM capacitor is bypassed and SM terminal voltage is zero. If S_a is off, S_{ax} is on, therefore SM terminals voltage is V_c and SM capacitor is inserted into the circuit. Each sub-module capacitor needs to be charged by a fraction of DC bus voltage E/N where N is the number of sub-modules per arm. Therefore, the output voltage (V_{ao}) swings between $-V_{pn}/2$ and $V_{pn}/$ and each arm should aim to produce the reference output voltage potential, as average over one switching period. Output inductors L_o have the role to limit the current ripple caused by the momentary mismatch of voltage produced by the two arms, and also enable the control of circulating current needed to replenish the energy in the SM capacitors. The modulation scheme for generating these states will be explained in § IV.

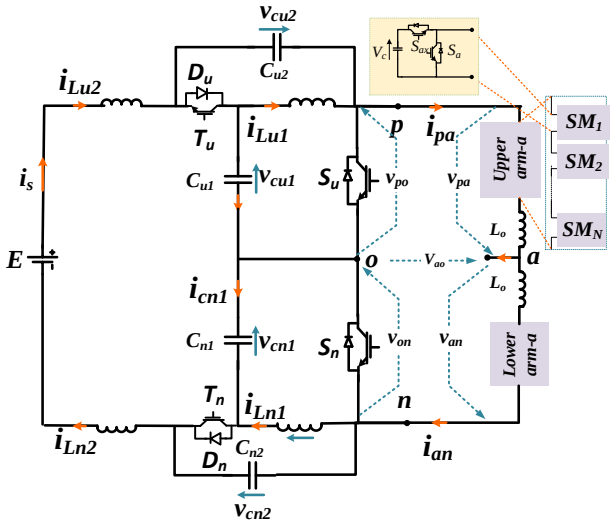

Fig. 3: Typical topology of an N-cell single-phase MMC

The output voltage equation as a function of the upper arm, lower arm and the DC-link voltages are given by:

$$v_{ao} = \frac{v_{an} - v_{pa}}{2} + \frac{v_{po} - v_{on}}{2} \quad (1)$$

From (1), if the upper qZS-network is shorted via S_u, i.e. v_{po}=0, the upper arm voltage v_{pa} should be reduced to keep the required output voltage at certain level which can be achieved by reducing the number of inserted cells in the upper arm by N/2. The same procedure is followed if the lower qZS-network is shorted via S_n. In this study, phase disposition SPWM (PD-SPWM) is used to control the MMC arms [10]. The S_u and S_n have been modulated using the proposed technique as follows.

3 MMC capacitors voltage balancing and modulation scheme

3.1 Capacitor voltage balance

The MMC requires a voltage balancing strategy to balance and keep the sub-modules capacitor voltages at their desired average values. The implementation of balancing strategies depends on the presence of the redundant states in the MMC arm [11]. The redundant switching state with the strongest effect in facilitating voltage balancing is always selected. The MMC arm capacitors balancing can be achieved by different strategies [11]. The most widely used balancing strategy is based on the sorting method [6] which is summarized in four steps as follows:

1) Measure and sort the upper and lower capacitor voltages;
2) From modulation scheme, determine the number of inserted cells (n_p and n_n) from upper and lower arms respectively;
3) If the upper (lower) arm current is positive where current direction shown in Fig. 3 is considered as positive, choose the n_p (n_n) cells with lower voltage to be inserted. Therefore, the corresponding cell capacitor is charged and its voltage increases;
4) If the upper (lower) arm current is negative, choose the n_p (n_n) cell with higher voltage to be inserted. Therefore, the corresponding cell capacitor is discharged and its voltage decreases.

3.2 Modulation scheme

To synthesize n-level voltage waveform at the converter AC-side where n equal 2N-1, phase disposition SPWM (PD-SPWM) with two complementary reference signals (v_{mn} and v_{mu}) is used in this study to control the BqZS-MMC as indicated in Fig. 4. Each carrier is responsible for producing the gating signals of two cells (one from upper and one from lower arm). The reference signals are compared against the carriers to define which leg-switches are conducting. The upper (lower) qZS-networks can be in shoot-through (ST) mode if the number of upper (lower) inserted cells equals or is higher than N/2. Therefore, the number of inserted cells can be reduced by N/2 to obtain the required voltage level. According to this concept, this modulation scheme can be named as reduced number of the inserted cell (RNIC) technique. By considering N =4, the number of output voltage level will be nine as clarified in Fig. 4. Table 1 lists the available voltage levels when N=4 by clarifying the number of inserted SMs in both upper and lower arms for each level before and after introducing ST intervals and which qZS-network switches S_u and S_n should be gated. S_u can be shorted during all output voltage levels except levels 1, 2 and 3 (7, 8 and 9 for S_n) as shown in Table 1 and Fig. 4, because at these levels, the number of inserted cells from the upper (lower) arm is less than two (N/2). Therefore, ST signals of S_u at levels 1, 2 and 3 are set to zero.

Fig. 4 shows the output voltage waveform, ST signals and the gating signals for both S_u and S_n. The upper ST signal ($V_{sh\text{-}u}$) is defined by:

$$V_{sh\_u} = \begin{cases} M_{sh} & 0 < \omega t \le \theta_2;\ \pi - \theta_2 < \omega t \le 2\pi \\ N/2 \times M_{sh} \sin \omega t & \theta_2 < \omega t \le \theta_1;\ \pi - \theta_1 < \omega t \le \pi - \theta_2 \\ 1 & \theta_1 < \omega t \le \pi - \theta_1 \\ 1 - M_{sh} & \pi < \omega t \le 2\pi \end{cases} \quad (2)$$

Where M_{sh} is the ST modulating signal height as shown in Fig. 4. In the range from Θ_1 to π- Θ_1, the number of inserted SMs per arm became lower than $N/2$, where shoot-through interval should set at zero, Θ_1 is defined by:

$$\theta_1 = \sin^{-1}(2/NM_{sh}) \qquad \theta_2 = \sin^{-1}(2/N) \quad (3)$$

The lower ST signal $V_{sh\text{-}n}$ waveform is the same shape as $V_{sh\text{-}u}$ but shifted by 180° as shown in Fig. 4. The pulses of S_u and S_n are generated if carrier signal C_{sh} is higher than $V_{sh\text{-}u}$ and $V_{sh\text{-}n}$ respectively. According to $V_{sh\text{-}u}$ and $V_{sh\text{-}n}$ signals, the output voltage reference waveforms (V_{mu} and V_{mn}) for the upper and lower arms are modified as shown in Fig. 5 in order to provide a reduction in the number of inserted cells during these intervals by two cells (N/2). From (2), the instantaneous value of duty ratio is given by:

$$d_{sh\_u} = \begin{cases} 1\text{-}M_{sh} & 0 < \omega t < \theta_2 ; \pi\text{-}\theta_2 < \omega t < 2\pi \\ 1\text{-}N/2 \times M_{sh} \sin wt & \theta_2 < \omega t < \theta_1 ; \pi\text{-}\theta_1 < \omega t < \pi\text{-}\theta_2 \\ 0 & \theta_1 < \omega t < \pi\text{-}\theta_1 \end{cases} \quad (4)$$

By integrating (4), the average shoot-through duty ratio D_{sh} can be calculated which is given by:

$$D_{sh} = (\pi + 2\theta_2)(1\text{-}M_{sh})/2\pi + (\theta_1\text{-}\theta_2)/\pi + NM_{sh}(\cos\theta_1\text{-}\cos\theta_2)/\pi \quad (5)$$

From (5), The DC-link voltage can be expressed by:

$$V_{pn} = 1/(1 - 2D_{sh}) \times E = \frac{\pi}{2\theta_1 + M_{sh}(2N(\cos\theta_1 - \cos\theta_2) - 2\theta_2 - \pi)} E \quad (6)$$

Fig. 5 shows the normalized peak DC-link voltage versus shoot-through duty ratio M_{sh} when N=2, 4, 6, 8 and 10. By increasing the number of sub-modules, higher M_{sh} is required at the same DC link voltage. The qZS-capacitors voltages are given by:

$$V_{cu1} = V_{cn1} = (1 - D_{sh})V_{pn}/2 ; \quad V_{cu2} = V_{cn2} = D_{sh}V_{pn}/2 \quad (7)$$

For N of SMs per arms, the SMs capacitor voltages are given by:

$$V_{c-arm} = V_{pn}/N \quad (8)$$

From (8), the peak value of the fundamental output voltage is given by:

$$V_m = MNV_{c-arm}/2 = GE/2 \quad (9)$$

Level number	Voltage level	Number of SMs inserted N=4 (Upper, Lower)		(S_u, S_n)
		before	*after*	
1	- V_{pn} /2	4, 0	2, 0	(1, 0)
2	-3 V_{pn} /8	4, 1 3, 0	2, 1 1, 0	(1, 0)
3	- V_{pn} /4	3, 1	1, 1	(1, 0)
4	- V_{pn} /8	3, 2 2, 1	3, 0 0, 1	(0, 1) (1, 0)
5	0	2, 2	0, 2 2, 0	(1, 0) (0, 1)
6	V_{pn} /8	1, 2 2, 3	1, 0 0, 3	(0, 1) (1, 0)
7	V_{pn} /4	1, 3	1, 1	(0, 1)
8	3 V_{pn} /8	1, 4 0, 3	1, 2 0, 1	(0, 1)
9	V_{pn} /2	0, 4	0, 2	(0, 1)

Table 1: The available voltage levels with clarifying the number of inserted SMs in both upper and lower arms

Where G is given as a function of D_{sh} (or M_{sh}) and output voltage modulation index M by:

$$G = M/(1\text{-}2D_{sh}) = 3\pi M/[(4\pi + 6\sqrt{3} - 12\cos\theta_1)M_{sh} - 6\theta_1] \quad (10)$$

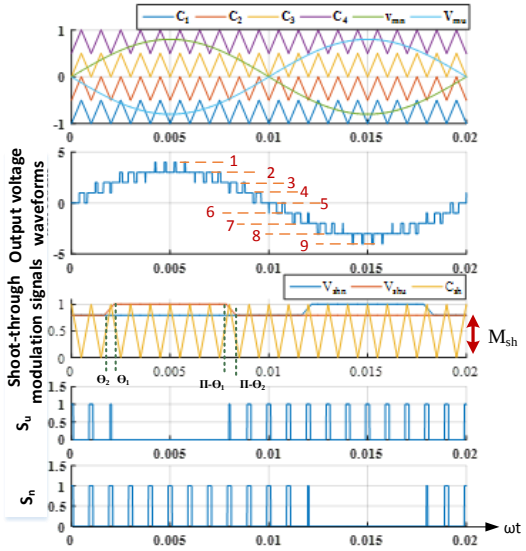

Fig. 4: The PD-PWM with double reference waveforms, the shoot-through modulation signals and the generated pulses for RNIC technique.

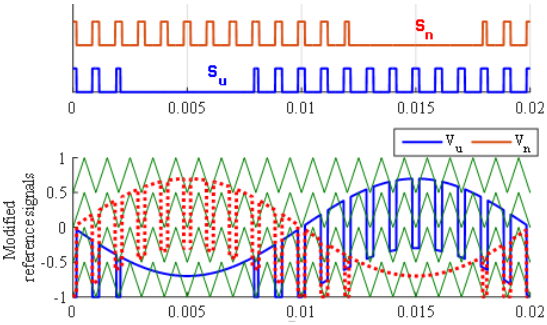

Fig. 5: The modified output voltage reference waveforms according to the shoot-through pulses for RNIC technique.

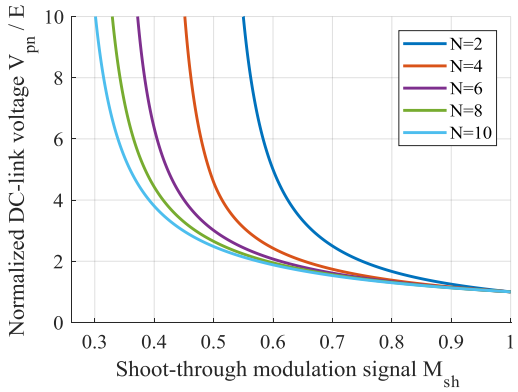

Fig. 6: Normalized DC-link voltage V_{pn}/E, versus shoot through modulation index M_{sh}.

4 Choosing values of passive element

According to [8], using an IGBT in antiparallel to the diode D in the BqZS-network allows the converter to operate with small values of inductance without disturbing the operation of the circuit, being able to completely avoid the undesirable operation modes found in [8], consequently, eliminating any drops in the dc-link voltages that affected the output harmonic distortion. However, the qZS inductance value should be chosen for limiting the ripples to a reasonable level (20%) to reduce the current stress on the converter devices.

The inductance value of the four inductors is chosen according to [12]. The arm inductance and SM capacitance are calculated according to the relevant study and the relations given in [13]. In this section, the general relation for determining the proper qZS-capacitance value has been obtained. According to [8], the qZS-capacitor voltages V_{cu1} and V_{cu2} (V_{cn1} and V_{cn2}) decrease when the arm current value i_{pa} (i_{na}) is higher than average value of inductor current I_L during both ST and NST modes as indicated in Fig. 7. The interval when the arm current is higher than the average inductor current ranges between θ_a and θ_b where θ_a and θ_b are the two instants when the arm current is equal to I_L. The upper and lower arm currents can be expressed by:

$$i_{pa} = i_a/2 + i_{2f} + I_{dc} \;;\; i_{na} = -i_a/2 + i_{2f} + I_{dc} \quad (11)$$

where I_{dc} is the DC component in arm currents which is responsible for transferring real active power from the supply to the load. The, i_{2f} is the second order harmonic usually present in any single phase converters and i_a is the AC load current component. In the following analysis, the value of the 2nd order harmonic is not a significant as i_a, so i_{2f} is not considered and set to zero in (11). From power balance equation, the maximum value of the load current I_a can be calculated by:

$$I_a = \frac{2EI_L}{V_m cos\Phi}\sin(\omega t - \Phi) \quad (12)$$

Where Φ is the load displacement angle, I_{dc} s the DC-component in the arm current which can be calculated as a function of the average value of qZS-inductor current by:

$$I_{dc} = \frac{1-2D_{sh}}{1-D_{sh}} I_L \quad (13)$$

Substituting by (12) and (13) into (11), and equating the resultant equation by I_L, θ_a and θ_b can be calculated by:

$$\theta_a = \sin^{-1}\left(\frac{D_{sh}}{2(1-2D_{sh})}cos\Phi\right) + \Phi$$
$$\theta_b = \pi - \sin^{-1}\left(\frac{D_{sh}}{2(1-2D_{sh})}cos\Phi\right) + \Phi \quad (14)$$

The capacitance C_{u1} can be obtained by:

$$C_{u1} = \frac{I_c \Delta t}{\Delta v_{cu1}} \quad (15)$$

According to Fig. 7, Δt and Δv_{cu1} can be defined as:

$$\Delta v_{cu1} = k_v V_{cu1} \quad \& \quad \Delta t = \frac{\theta_b - \theta_a}{2\pi} * \frac{1}{f_o} \quad (16)$$

Where V_{cu1} is the average value of the qZS capacitor voltage k_v, is the ratio between peak to peak capacitor voltage Δv_{cu1} and V_{cu1} and f_o is the output load frequency. The capacitor current I_c during the interval from θ_a to θ_b is given by:

$$i_c(t) = \begin{cases} I_L - i_{pa} & \text{non-shoot-through mode } (1\text{-}D_{sh}) \\ -I_L & \text{shoot-through mode } D_{sh} \end{cases} \quad (17)$$

The average value of $i_c(t)$ over a switching period is given by:

$$I_{c-sw} = -D_{sh} I_L + (1 - D_{sh})(I_L - i_{pa}(t)) \quad (18)$$

Substituting (11)-(13) into (18), and integrating from θ_a to θ_b, the average value of i_c over the interval from θ_a to θ_b is given by:

$$I_c = \frac{4(1-2D_{sh})\,cos(\theta_2 - \Phi)}{cos\,\Phi\,(\theta_2 - \theta_1)} I_L \quad (19)$$

Substituting (7) and (19) into (15), the minimum required capacitance to provide a kv voltage ripple can be obtained as:

$$C_{u1} \geq \frac{4(1-2D_{sh})^2 \cos(\theta_b - \Phi) P}{\pi K_v f_o \cos\Phi (1-D_{sh}) E^2} \quad (20)$$

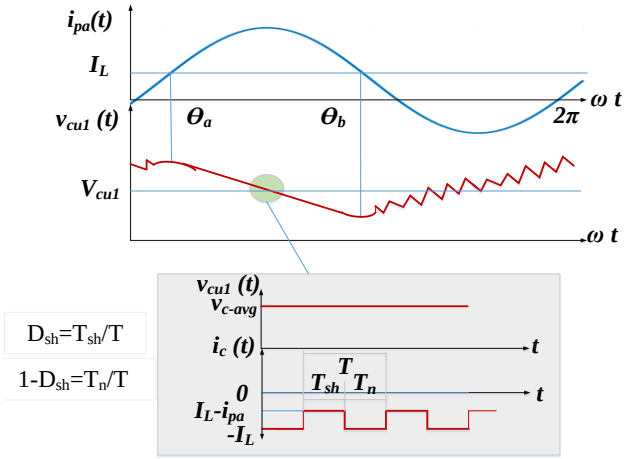

Fig. 7: a) The upper arm current, the qZS capacitor voltage waveform, the zooming of capacitor voltage and currnt waveform

5 Simulation results

To verify the validity of the proposed modulation scheme for the BqZS-MMC, a simulation model is implemented in MATLAB/PLECS for the proposed configuration shown in Fig. 2 with a number of SMs equal to 6. The parameters used in the simulation models are given in Table 2. The simulation study has been carried out using a passive (R+L) load and considering that all system components and switches are ideal.

The optimum qZS-capacitors (C_{u1} and C_{n1}) were calculated in order to provide the voltage ripple factor k_v of about 10%. Based on the parameters in Table 2, the required value of the qZS-capacitor is around 3.15 mF which is calculated by (20).

The converter modulation index M is set at 1 and the shoot-through modulation index M_{sh} is set to 0.8 (boost), 0.6 (boost) and 1 (buck) and consequently the shoot-through duty ratio D_{sh} is equal 0.124, 0.256 and zero respectively.Fig. 8 and Fig. 9 shows the upper, lower and overall DC link voltage, and their zooming respectively. By lowering M_{sh} from 0.8 to 0.6, the peak value of overall DC-link voltage is increased from 4kV to 6.2kV. Also, to check the operation in buck mode, M_{sh} is set at 1, where the peak value of overall DC-link voltage becomes 3kV that equal the DC source voltage E.

The simulation results of qZS-network capacitor (V_{cu1}, V_{cn1}, V_{cu2} and V_{cn2}) and arm capacitor voltages are shown in Fig. 10 and Fig. 11 illustrates their zooming. These capacitors are charged according to the relations given in (7) and (8). The ripple factor k_v of V_{cu1} and V_{cn1} is around to 10% which confirm the validity of the proposed capacitance formula. Load voltage and current are shown in Fig 12. For the proposed BqZS-MMC, by lowering M_{sh} from 0.8 to 0.6, the peak value of output voltage fundamental component is increased from 2kV to 3.1kV. However, for traditional MMC, the peak value of the output voltage is limited to half value of supply voltage ($E/2$=1500V). The output current shown in Fig. 12 does not show low order harmonics, which is a sign that the proposed modulation works as expected.

Source voltage E	3kV	Load inductance and resistance	14 mH, 13 Ω
qZS-networks inductances	10 mH	qZS-networks Capacitances	3.3 mF
MMC-arm inductance	5mH	MMC-arm capacitances	3.3 mF
Switching frequency	2 kHz	Output frequency f_o	50 Hz

Table 2: ZSI simulation model parameters

6 Conclusion

This paper proposed a modulation scheme for bidirectional quasi Z-source modular multilevel converter topology that is able to achieve buck and boost voltage capabilities. The relation between modulation index and average shoot-through duty ratio has been derived and verified by simulation at different modulation indexes in both buck and boost mode. An analytical design methodology for calculating the required values of quasi Z-source capacitors has been proposed and the resulting ripples in the simulation match the ripple imposed in the design.

References

[1] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-Voltage Multilevel Converters-State of the Art, Challenges, and Requirements in Industrial Applications," *IEEE Transactions on Industrial Electronics*, vol. 57, pp. 2581-2596, 2010.

[2] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna Power Tech Conference Proceedings*, 2003, p. 6 pp. Vol.3.

[3] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," *IEEE Transactions on Power Electronics*, vol. 30, pp. 37-53, 2015.

[4] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system," in *2011 IEEE Power and Energy Society General Meeting*, 2011, pp. 1-1.

[5] A. U. Lawan, H. Abbas, J. G. Khor, and A. A. Karim, "Dynamic performance improvement of MMC inverter with STATCOM capability interfacing PMSG wind turbines with grid," in *2015 IEEE Conference on Energy Conversion (CENCON)*, 2015, pp. 492-497.

[6] R. Guruambeth and R. Ramabadran, "Fuzzy logic controller for partial shaded photovoltaic array fed modular multilevel converter," *IET Power Electronics*, vol. 9, pp. 1694-1702, 2016.

[7] T. Nakanishi, K. Orikawa, and J. i. Itoh, "Modular Multilevel Converter for wind power generation system connected to micro-grid," in *2014 International Conference on Renewable Energy Research and Application (ICRERA)*, 2014, pp. 653-658.

[8] F. A. Khera, C. Klumpner, and P. W. Wheeler, "Operation Principles of Quasi Z-Source Modular Multilevel Converters", in *2017 IEEE 3nd Annual Southern Power Electronics Conference (SPEC)*, 2017.

[9] J. Anderson and F. Z. Peng, "A Class of Quasi-Z-Source Inverters," in *2008 IEEE Industry Applications Society Annual Meeting*, 2008, pp. 1-7.

[10] X. Shi, Z. Wang, L. M. Tolbert, and F. Wang, "A comparison of phase disposition and phase shift PWM strategies for modular multilevel converters," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 4089-4096.

[11] G. P. Adam, O. Anaya-Lara, G. M. Burt, D. Telford, B. W. Williams, and J. R. Mcdonald, "Modular multilevel inverter: Pulse width modulation and capacitor balancing technique," *IET Power Electronics*, vol. 3, pp. 702-715, 2010.

[12] S. Rajakaruna and L. Jayawickrama, "Steady-State Analysis and Designing Impedance Network of Z-Source Inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, pp. 2483-2491, 2010.

[13] M. Zygmanowski, B. Grzesik, and R. Nalepa, "Capacitance and inductance selection of the modular multilevel converter," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1-10.

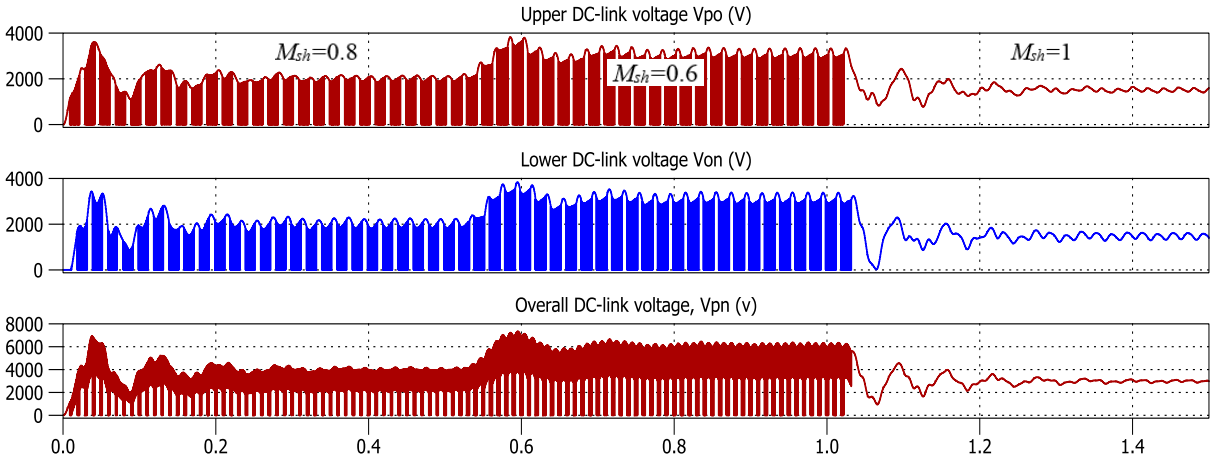

Fig. 8: The upper, lower and and overall DC link voltage at M_{sh}=0.8, 0.6 and 1 from left to right respectively.

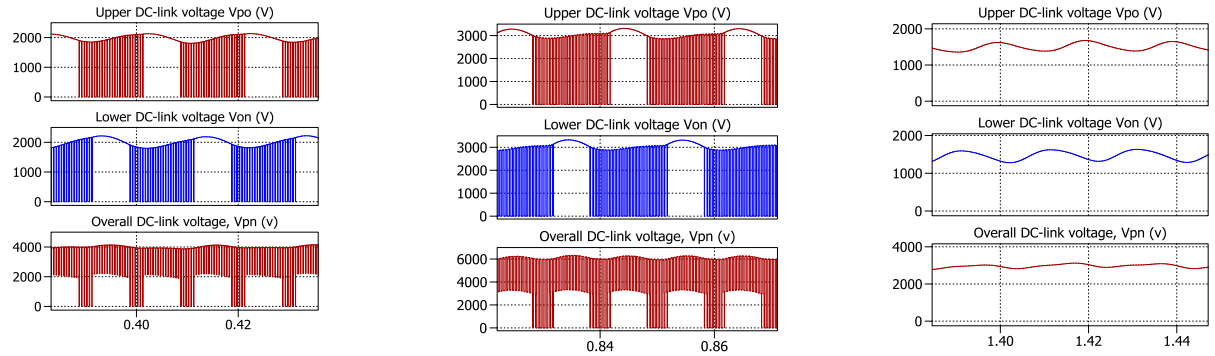

Fig. 9: Zooming of the upper, lower and and overall DC link voltage at M_{sh}=0.8, 0.6 and 1 from left to right respectively.

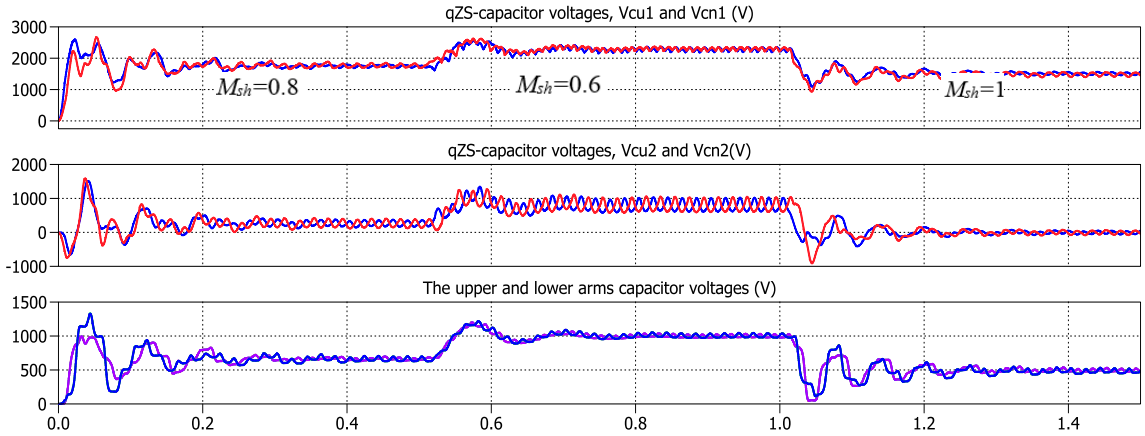

Fig. 10: The qZS-network capacitor and arm capacitor voltages at M_{sh}=0.8, 0.6 and 1 from left to right respectively

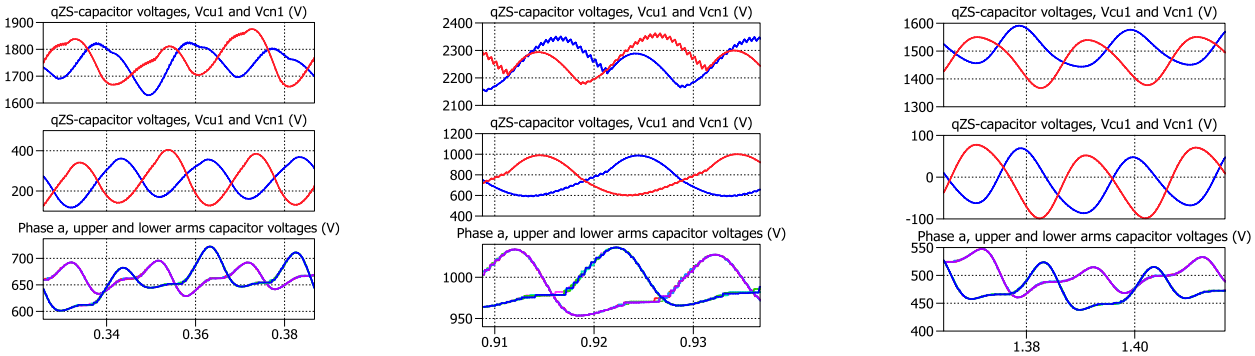

Fig. 11: Zooming of the qZS-network capacitor and arm capacitor voltages at M_{sh}=0.8, 0.6 and 1 from left to righrespectively

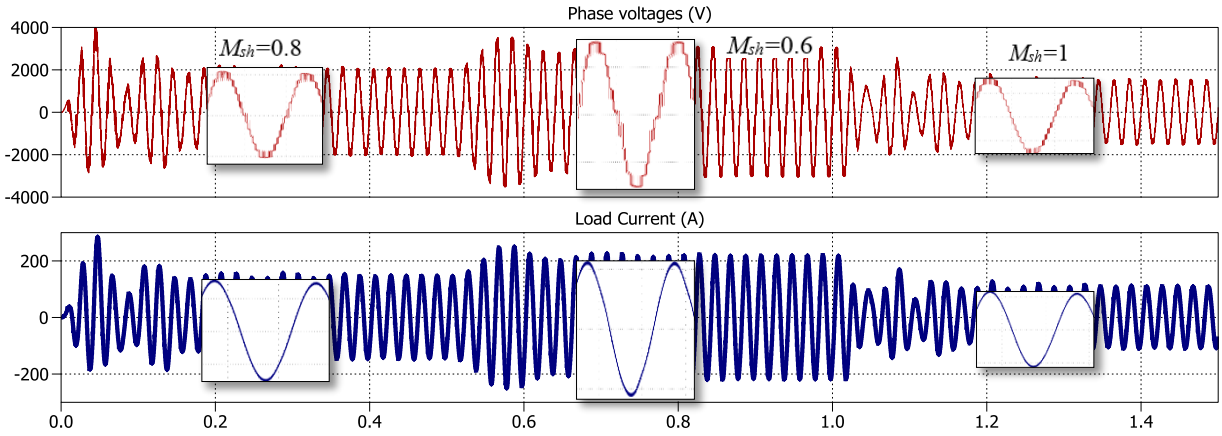

Fig. 12: Load voltage and current at M_{sh}=0.8, 0.6 and 1 from left to right respectively