Design Considerations For A High-power Dual Active Bridge DC-DC Converter With Galvanically Isolated Transformer

Youngsil Lee, Alan. J. Watson, Gaurang Vakil, Patrick W. Wheeler
Power Electronics, Machines and Control Research Group
The University of Nottingham
Nottingham, UK
Youngsil.Lee@nottingham.ac.uk

***Abstract*—Multi-megawatt scale isolated DC-DC converters are likely to become increasingly popular as means to interconnect the MVDC grids of different voltage levels. Three-phase dual active bridge DC-DC (3DAB) converters operating with the zero-voltage switching (ZVS) is a promising candidate for the target multi-megawatt application. This paper presents a systematic approach of the design considerations for a 3DAB converter. Firstly, the use of snubber capacitors in medium voltage and medium frequency operating conditions is proposed. Snubber capacitor influence on turn-off current levels and ZVS operating range are introduced and analyzed. In addition, details of thermal management design are introduced. It is established through power loss analysis that the proposed design method reduces the semiconductor losses substantially at full load conditions. Finally, the proposed method has been validated from a 10kW simulation model using PLECS software package.**

Keywords— Dual active bridge, DC-DC, snubber capacitor, thermal management, power losses, ZVS, MVDC

I. INTRODUCTION

High-power DC-DC converters are one of the primary technologies for the interconnection of MVDC grids. High-power DC-DC converters must be galvanically isolated from the MVDC line to the low-voltage direct current (LVDC) line for safety reasons. Galvanic isolation is also required for several converter modules of modular topologies to operate in series or parallel connection. Many DC-DC converter topologies have previously been presented in various fields such as the automotive industry, urban railway substations, renewable energy sources and DC grid collectors [1]-[7]. They can be divided into the categories of "those with galvanic isolation" and "those without galvanic isolation". When high-voltage conversion ratios are needed, galvanic isolated converters can achieve a higher conversion efficiency than converters that are not galvanically isolated.

It leads to a voltage drop across the stray inductances, which results in a current being introduced by a six-step voltage generated at the transformer. The power can be transferred by the phase shift angle φ .

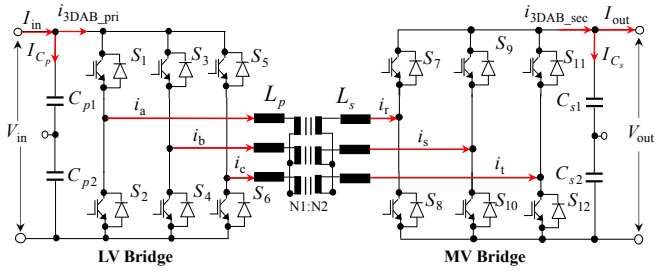

Fig. 1. A 3DAB converter topology

A Three-phase dual active bridge DC-DC (3DAB) converter suitable for high-power applications has been studied in [8]-[12]. The topology of the 3DAB converter is illustrated in Fig. 1. The 3DAB converter offers a higher power capability and smaller passive filtering parts than the single-phase dual-active bridge (1DAB) type [13]-[14]. Dynamic control strategies for the 3DAB have recently been introduced in [12]. The 3DAB converter involves two active voltage sourced bridges which are magnetically connected by a medium-frequency (MF) transformer. The primary side bridge converts the DC input voltage into a medium-frequency AC voltage which is applied to the MF transformer; the voltage at the secondary terminals of the transformer is then rectified by the secondary side bridge. The three-phase legs operate with a 120° phase shift from each other at the fundamental switching frequency. The 3DAB converter is suitable for bi-directional power flow and buck-and-boost converter applications, in which the transformer has a different turns ratio. One of key components of the 3DAB converter is a high-power galvanic transformer which enables isolation from the MV line for safety reasons and also contributes to soft-switching control, which can dramatically reduce the switching losses. The MF transformer provides galvanic isolation. The phase shift angle, φ introduces a load angle between the primary and secondary windings of the transformer.

In [15], the basic principle and an analytical modelling of the 3DAB converter for MVDC applications has been

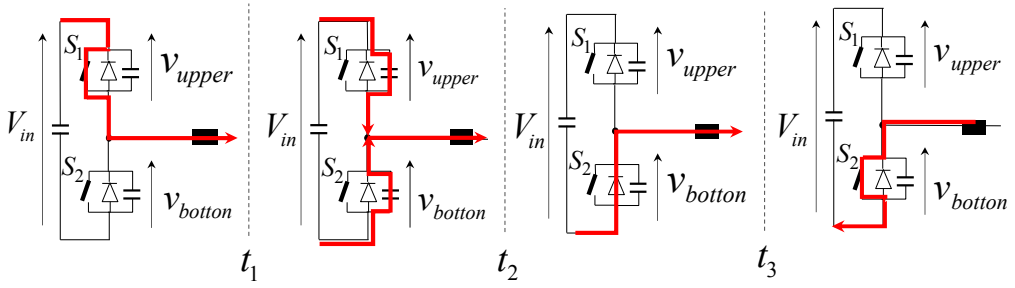

Fig. 2. Commutation in a half-bridge of a 3DAB converter

presented. The models have been used to derive an estimation method for RMS current values for the 3DAB converter.

In [15], the basic principle and an analytical modelling of the 3DAB converter for MVDC applications has been presented. The models have been used to derive an estimation method for RMS current values for the 3DAB converter.

This paper presents an optimal design approach for the snubber capacitance value of a 3DAB converter using parallel connected lossless snubber circuits. In addition, a thermal design and implementation of the 3DAB converter is included in this paper. In Section II, snubber capacitor sizing and their influence are introduced. A detailed overview of the physical principles of heat transfer and power losses is described in Section III. A 10kW proposed converter with the optimized parameters is simulated using PLECS software. In Section IV, simulation results are discussed. Finally, the conclusions are presented in Section V.

II. LOSSLESS SNUBBER CIRCUIT DESIGN

A. *Snubber capacitor circuit commutations*

The general commutation characterizing of ZVS operation of a 3DAB converter half-bridge with lossless snubber capacitor is illustrated in Fig. 2. In the case of a high voltage system, a series connection of several switches per switch branch is required to operate with a high dc-link voltage. The snubber capacitor is connected in parallel with each power semiconductor switch. A brief description is given in the following:

- At the beginning of the commutation cycle, the upper switch S_1 is turned-on. Assuming the S_1 is in the on state from the upper diode interval, the S_1 is conducting the switched current.
- At t_1, the high side switch S_1 is switched-off. The turn-off of the current forces the load current to commutate entirely to the upper snubber capacitor.
- At the stage (t_1 - t_2), the upper snubber capacitor begins to charge while the bottom capacitor starts to discharge. The dv/dt slope on the switch is determined by the size of the stray inductance of the transformer which is large enough to maintain the output current and by the size of the snubber capacitor during the commutation. Furthermore, if the size of the snubber capacitor is sufficiently large, the switch current will have decreased rapidly until it reaches zero during the increase of the power semiconductor voltage. At that time, the turn-off losses are significantly reduced compared to a hard switching operation.
- At t_2, the lower snubber capacitor is fully discharged. Afterwards, the lower antiparallel diode is formed as forward biased. Hence, the conducting current of the diode is flowing into the stray inductance of the transformer. During the switching commutation, the low side switch S_2 is turn-on with ZVS condition. Thereby, the turn-on losses are theoretically zero during the ZVS. The switched transformer current is negative when the low side diode is conducting.
- At t_3, the polarity of the transformer current is forced to change while the lower diode is conducting and the low side switch S_2 is gated on. After the process, S_2 is already conducting the current and one switching cycle is completed.

The ZVS operation can be achieved with sufficiently large snubber capacitances to reduce switching losses. In addition, snubber capacitor to minimize the effect of turn-off commutation dv/dt time. The dv/dt increases with the turn-off current (I_{OFF}) of the converter. The sizing of the snubber capacitor can be carried out by the initial maximum turn-off current conditions in an ideal snubberless converter circuit. Maximum turn-off currents on primary and secondary side converter in case of ideal snubberless 3DAB Converter under the condition that the phase shift angle range is limited to $\varphi \le \pi/3(60^{\circ})$ can be calculated using (1) and (2)[11]

$$I_{\mathrm{OFF\_max\_p}} = \left(\frac{2\pi}{3} \cdot V_{\mathrm{pri}} - \left(\frac{2\pi}{3} - |\varphi| \right) \cdot n \cdot V_{\mathrm{sec}} \right) \Big/ 6\pi f_{sw} \cdot L_{\sigma} \quad (1)$$

$$I_{\mathrm{OFF\_max\_s}} = \left(\frac{2\pi}{3} \cdot n \cdot V_{\mathrm{sec}} - \left(\frac{2\pi}{3} - |\varphi| \right) \cdot V_{\mathrm{pri}} \right) \Big/ 6\pi f_{sw} \cdot L_{\sigma} \quad (2)$$

Where, n is turn ratio between the primary side and secondary side of the ac-link transformer. The maximum currents for each bridge is calculated by the maximum voltage of the primary side, minimum value of the secondary bridge voltage, and phase shift angle, φ corresponding to nominal

power transfer. The calculated turn-off currents are used to estimate the sizing of the resonant snubber capacitances.

B. Snubber capacitor sizing

A simplified equivalent circuit of the commutation from half-bridge switch of 'phase a' on the primary bridge converter is derived in Fig. 3.

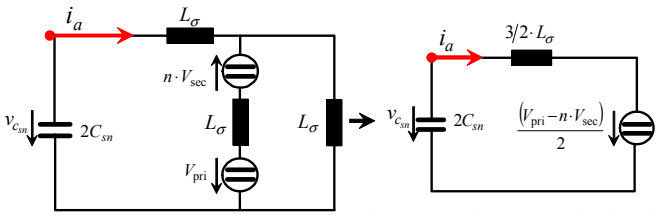

Fig. 3. Equivalent circuit of half-bridge 'phase a' on the primary bridge of 3DAB converter

In the representative circuit, the 3DAB converter is limited to operate with a phase shift angle of $0 \le \varphi \le \pi/3(60°)$. The parallel-connected snubber capacitors have been comprised with twice the size of the capacitance. At the beginning of the switching cycle, the $v_{c_{sn}}$ is zero and the one switching cycle is completed when the $v_{c_{sn}}$ becomes equal with the input dc-link voltage. The switching commutation cycle of the 3DAB converter is represented by six time intervals. Finally, the simplified secondary circuit has a constant series-connected voltage. The value of the comprised series voltage is dependent on the transformer turn ratio or the charging time of the $2C_{sn}$ during switching commutation. The equivalent circuit shows that the switching cycle is determined by an oscillation between the $2C_{sn}$ and the resonant inductance of $(3/2) \cdot L_\sigma$. Using the diagram, the associated resonant characteristics are calculated as

$$\omega_{r\_p,s} = \frac{1}{\sqrt{\frac{3}{2} \cdot L_\sigma \cdot 2C_{sn\_p,s}}} = \frac{1}{\sqrt{3 \cdot L_\sigma \cdot C_{sn\_p,s}}} \tag{3}$$

$$Z_{r\_p,s} = \frac{3}{2} \cdot L_\sigma \cdot \omega_{r\_p,s} = \sqrt{\frac{3L_\sigma}{4C_{sn\_p,s}}} \tag{4}$$

Where, $\omega_{r\_p,s}$ is resonant frequency and $Z_{r\_p,s}$ is resonant impedance. The snubber capacitor must be designed to obtain a certain voltage slope rate across the switches because the limitation of the *dv/dt* increases turn-off commutation times. Hence, the required minimum commutation time at maximum turn-off currents will be assumed by the allowed duration of the maximum voltage slopes across the switches. With the identical maximum level of $I_{\mathrm{OFF|max}}$, the value of C_{sn} that leads to minimum turn-off commutation time, $t_{\mathrm{off|min}}$, can be considered at the calculated $I_{\mathrm{OFF|max}}$

$$C_{sn\_\min} \approx \frac{t_{\mathrm{off|min}}}{\Delta V_{\mathrm{Tmax}}} \cdot I_{\mathrm{OFF\_max}} \tag{5}$$

A simple sizing of the capacitance can be used by assuming linear *dv/dt* slopes and a constant value of turn-off commutation currents.

C. Minimizing turn-off commutation of 3DAB

In general, a certain value of snubber capacitor has influence on the limitation of *dv/dt* slopes and the increase of commutation times on the switch branches. Hence, these have great impact on the operated waveform's characteristics of 3DAB converter with sunbber capacitor circuits. A comparison of theoretical ac-link transformer voltage and current waveforms of a 3DAB converter operated under boost operation is illustrated in Fig. 4.

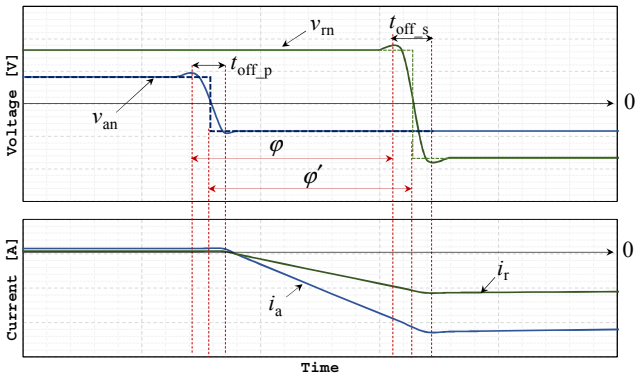

Fig. 4. Comparison of simulated ac-link transformer voltage and current waveforms of a 3DAB converter in case of turn-off commutation resulting from boost mode

As can be seen, the ramp-shaped voltages have been defined as linear for illustration. On the contrary, the voltage slopes in real converter, have a high frequency damped oscillation caused by parasitic components during the turn-off commutation, which has been neglected for the ideal illustration purpose. Besides, the commutation times as well as the value of the snubber capacitors may be generally different between the primary and secondary bridges in a real converter system, unless the converter is operating under unity ratio conditions. For that reason, the individual turn-off times $t_{\mathrm{off\_p}}$ and $t_{\mathrm{off\_s}}$ are determined for the each bridge.

Since the secondary bridge voltage has been set higher than the primary voltage, the ac-link transformer current is negative at the turn-off commutation stage to ensure ZVS. For a good analytical approach into the snubber influence, the ramp-shaped ac-link currents can be placed in the center of these waveforms. With the centering of the ramp-shaped voltages, the current waveforms may not differ also between the commutation intervals. On the other hand, the step changes may leads to the peaking of the ac-link currents in the middle of the commutation intervals. In addition, it should be noted that the centering of the ramp-shaped voltages leads to

different phase shift angle compared to the value of the ideal waveform, unless the turn-off times, $t_{\text{off\_p}}$ and $t_{\text{off\_s}}$ are equal. Consequently, this modified angle results in the shifted gate signal in reference to the beginning of the switching intervals of primary and secondary side converter.

Snubber capacitances lead to different commutation times for the primary and secondary side converters, which results in a different phase shift angle. From Fig. 3, a substitute phase shift angle φ' is introduced as the delay between the centers of the each commutation. Hence, using knowing $\varphi, t_{\text{off\_p}}$ and $t_{\text{off\_s}}$, the calibrated new φ' can be calculated as follows

$$\varphi' = \varphi + \Delta\varphi = \varphi + \omega_{sw} \cdot \left(t_{\text{off\_s}} - t_{\text{off\_p}}\right) \tag{6}$$

Where, initial control angle can be calculated as follows

$$\varphi = \frac{2\pi}{3} - \sqrt{\left(\frac{2\pi}{3}\right)^2 - 2\pi \cdot \frac{P_o \cdot \omega \cdot L_\sigma}{V_{in} \cdot V'_{out}}} \tag{7}$$

Considering the snubber capacitance increases the turn-off *dv/dt* resulting from the increased capacitor current, the maximum turn-off current should be carried out in reference to the specified capacitor circuit conditions. Thus, the maximum turn-off current for the ideal snuberless 3DAB converter provided in (1) and (2) can be rewritten as follows.

$$I'_{\text{OFF\_p}|\max} = \left(\frac{2\pi}{3} \cdot V_{\text{pri}} - \left(\frac{2\pi}{3} - |\varphi'|\right) \cdot n \cdot V_{\text{sec}}\right) \Big/ 6\pi f_{sw} \cdot L_\sigma \tag{8}$$

$$I'_{\text{OFF\_s}|\max} = \left(\frac{2\pi}{3} \cdot n \cdot V_{\text{sec}} - \left(\frac{2\pi}{3} - |\varphi'|\right) \cdot V_{\text{pri}}\right) \Big/ 6\pi f_{sw} \cdot L_\sigma \tag{9}$$

Under this condition, a negative turn-off current is indicating the outside of ZVS boundary on the primary and secondary side devices.

For a more accurate turn-off commutation, the initial negative phase current of the ac-link transformer initiating the unassisted turn-off commutation is leading to a charging of the snubber capacitors. As a consequence, the time based description of the capacitor voltage is valid during the turn-off commutation for any cases of $V_{\text{pri}}, V_{\text{sec}} > 0$ that can be defined.

For an assessment of the sensitivity of the turn-off currents on the turn-off commutation intervals, Fig. 5 shows $t_{\text{off\_p}|\min}$ and $t_{\text{off\_s}|\min}$ characteristics that have been numerically calculated for several combinations of snubber capacitors. These plots have been obtained from the ideal step-up 3DAB converter model employing a 5.2kV primary voltage and a 40kV secondary voltage, corresponding to a 4MW nominal power rating. As can be seen, smaller capacitances than the base value C_{sn_b} lead generally to a reduction of the commutation times for each side. It is found that employing higher capacitances contributes to a further power dissipation, resulting from longer commutation duration. Since the negative turn-off current are conducted on the primary side, fig. 5(a) indicates the ZVS operation of the primary bridge cannot be maintained under all conducted current levels. In contrast, the ZVS mode in the secondary bridge can be performed at all load conditions. While the larger absolute values of minimum currents decrease the turn-off interval times on the primary side, the effect of the current level is rather moderate on the secondary converter.

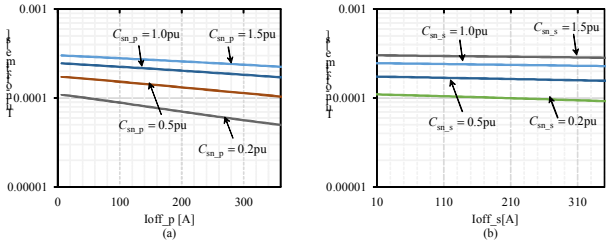

Fig. 5. Turn-off commutation time characteristics versus minimum turn-off currents of 4MW 3DAB converter by use of different snubber capacitors: (a) 5.2kV primary bridge and (b) 40kV secondary bridge converter

III. COOLING DESIGN AND POWER LOSSES

A. *Thermal modelling and power losses*

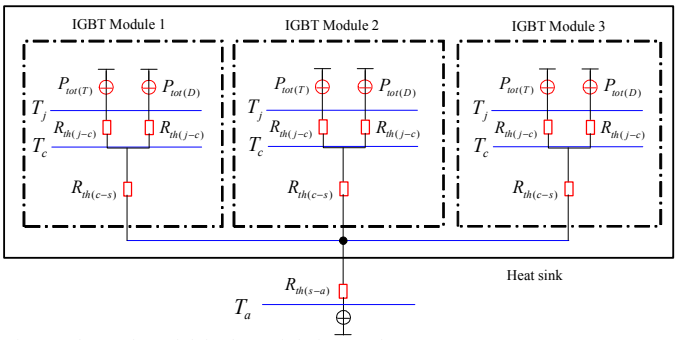

Fig. 6. Thermal model for heat sink for a 10kW 3DAB converter

The heat conduction of a semiconductor can be simulated as an electric circuits as shown in Fig. 6. The thermal model shown in Fig. 6 is the same for both bridge heat sinks. Using the equivalent circuit, the heat sink, case, and junction temperature can be calculated using the following thermal equation. By knowing the power losses of each IGBT and diode, the dissipated power in the thermal resistances is known.

Heat sink temperature

$$T_s = \left(P_{tot(T)} + P_{tot(D)}\right) \cdot R_{th(s-a)} + T_a \tag{10}$$

Case Temperature

$$T_c = \left(P_{tot(T)} + P_{tot(D)}\right) \cdot R_{th(c-s)} + T_s \tag{11}$$

Junction Temperature

$$T_{j(T)} = P_{tot(T)} \cdot R_{th(c-s)} + T_c \tag{12}$$

Where, $R_{th(j-c)}$ is junction- case, $R_{th(c-s)}$ is case-heat sink, and $R_{th(s-a)}$ is heat sink-ambient thermal resistance. The

consideration of power loss sources in the modules and on the heat sink is determined as following equations.

$$T_c = n_2 \cdot \left(P_{tot(T)} + P_{tot(D)}\right) \cdot R_{th(c-s)} + T_s \quad (13)$$

$$T_s = n_1 \cdot \left(P_{tot(T)} + P_{tot(D)}\right) \cdot R_{th(s-a)} + T_a \quad (14)$$

Where, n1 represents all components of power loss on the heatsink. The amount of IGBT modules on the heatsink. n_2 is all components of power loss in the module. The average conduction losses in the IGBT module are can be calculated by

$$P_{avg\_con\_igbt}(t) = \frac{1}{T_{sw}} \int_0^{T_{sw}} (v_{CE0} \cdot i_s(t) + r_0 \cdot i_s^2(t))dt \quad (15)$$

$$= v_{CE0} \cdot I_{avg\_igbt} + r_0 \cdot I^2_{rms\_igbt}$$

$$P_{avg\_con\_diode}(t) = \frac{1}{T_{sw}} \int_0^{T_{sw}} (v_{D0} \cdot i_D(t) + r_0 \cdot i_D^2(t))dt \quad (16)$$

$$= v_{D0} \cdot I_{avg\_diode} + r_0 \cdot I^2_{rms\_diode}$$

Where, r_0 is the slope resistances of the IGBT and diode, v_{CE0} is the collector-emitter voltage at zero current of the IGBT, and v_{D0} is the threshold voltage across the diode. If the 3DAB converter operates in the ZCS range, turn-on losses of the semi-conductors can be neglected. Turn-off loss is calculated from the turn-off energy loss curve given in the datasheet for the corresponding turn-off current and voltage. Average switching loss is calculated from

$$P_{sw} = n\left[(E_{OFF\_igct} + E_{OFF\_diode}) \times f_{sw} \times \frac{V_{CE}}{V_{CC}}\right] \quad (17)$$

Where, n is the number of devices, f_{sw} is the switching frequency, V_{CE} is the operating voltage, and V_{CC} is the maximum voltage defined from the energy loss curves.

B. Heat sink design

Fig. 7 shows the proposed design flow chart for the heat sink. The goal of the heat sink design is to calculate the thermal resistance of the heat sink. In the design process, the semiconductor junction temperatures, $T_{j(T)}$ should not exceed their designed temperature limits under worst-case operating conditions. The heat sink temperature, T_s is selected as the reference point for the worst-case operating point of the converter, since it maintains a relatively constant temperature compared to the IGBT and diode junctions. The design process involves calculating the IGBT module losses under full load conditions for the chosen surface temperature of heat sink with the desirable cooling method, then calculating the required heat sink-ambient thermal resistance, $R_{th(s-a)}$ to allow the heat sink to maintain the surface temperature at the full load.

As a starting point, assume an ambient temperature of 40°C. Using the manufacturer's datasheet, determine the maximum temperatures of the semiconductors. Also set the junction-case thermal resistance, $R_{th(j-c)}$ and case-heat sink thermal resistance, $R_{th(c-s)}$. The number of heat sources spread across the heat sink has a crucial impact on the $R_{th(s-a)}$. Therefore, it is important that the number of heat sources n is specified in the design process. Also a semiconductor device may consist of a parallel connection of several chosen components. This must also be defined. In this case, a three phase converter comprising 3 half-bridge modules is applied into the primary and secondary bridges. As a consequence, 6 switches are mounted on the each bridge heat sink without parallel connection.

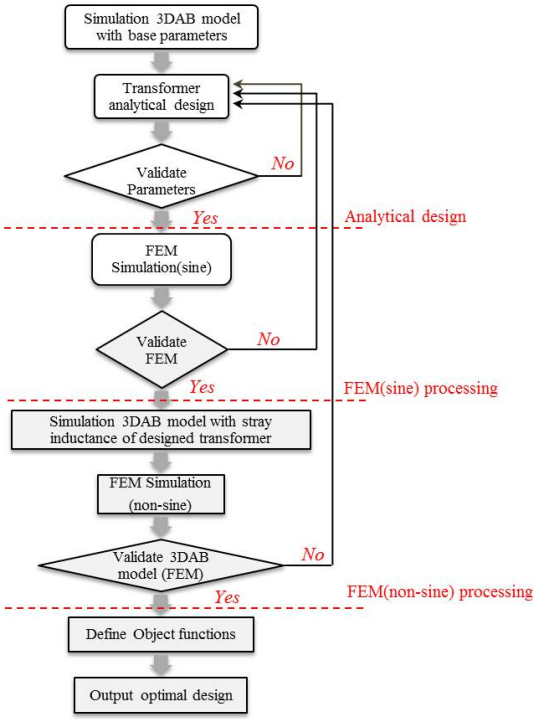

Fig. 7. Design flow chart of the heat sink

Natural air cooling is used in low power application up to 50W and even high power applications if sufficiently large cooling surfaces are available. The heat sink temperature is usually higher than with forced cooling system. For example, the heat sink temperature is about 90-100°C with natural air cooling whereas the rated surface temperature of forced air-cooled heat sink should not exceed 80-90°C.

Using the calculated losses, we can determine the thermal resistance that is required to keep the heat sink temperature at or below the chosen cooling system and also the junction temperatures of the IGBT and diode. The calculated junction temperatures should not exceed the maximum values for $T_{j(T)}$ given from the manufacturer. For example, in case of the SKM75GB176D IGBT module, the maximum temperature $T_{j(T)}$ is 150°C.

To verify the design, simulate the combined electrical-thermal model of the 3DAB Converter and measure the heat sink and junction temperatures for each component The

resulting $R_{th(c-s)}$ from the thermal design to find the heat sink dimensions regarding the calculated value of the $R_{th(c-s)}$. From the design, the allowed value of 0.43 °C/W for $R_{th(c-s)}$ is calculated.

IV. SIMULATION AND LOSS ANALYSIS

For validation, a 10kVA converter model has been simulated using PLECS software. The converter model is validated with 10nF snubber capacitors in the primary side and 6.8nF snubber capacitors in the secondary side. The converter uses SKM75GB176D Trench IGBT modules from SEMIKRON and is operating at a switching frequency of 1kHz. The input dc-link voltage is set to 500V. The stray inductance was measured to be around $L_\sigma = 92uH$. The turns ratio of the transformer is 1:2, hence, the output dc-link voltage is set to 1000V. In the validation, the control phase shift angle is set to $\varphi = 3.0°$. The expected results for the ac link voltages and currents from the simulation model are presented in Fig. 8 and 9 respectively. These results show six step square- waves at the primary and secondary windings of the transformer acting as ac magnetic coupling.

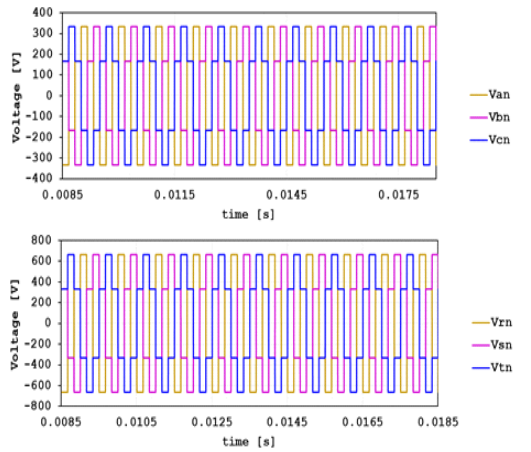

Fig. 8. Simulation results of the 3DAB converter at 9.5kW during boost mode: voltages generated by the primary and secondary bridges

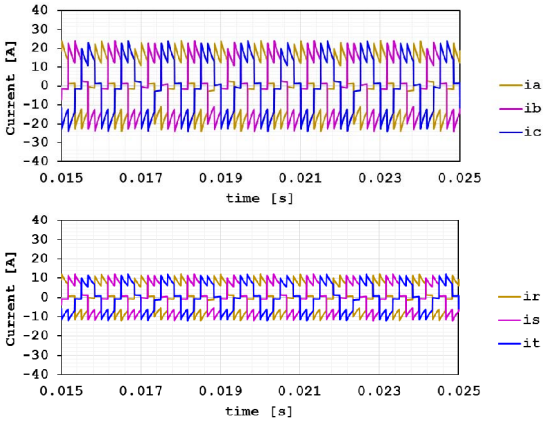

Fig. 9. Simulation results of the 3DAB converter at 9.5kW during boost mode: currents through the primary and secondary bridges

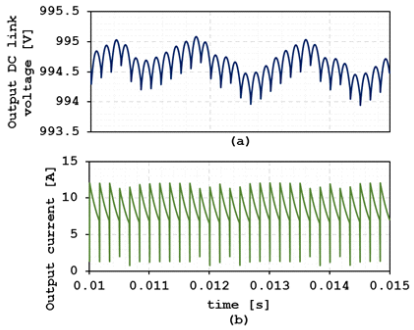

Fig. 10. Evaluated waveforms of the 1000 V output DC link in the 10kW simulation model at full load condition: (a) the DC link capacitor voltage and (b) the DC current

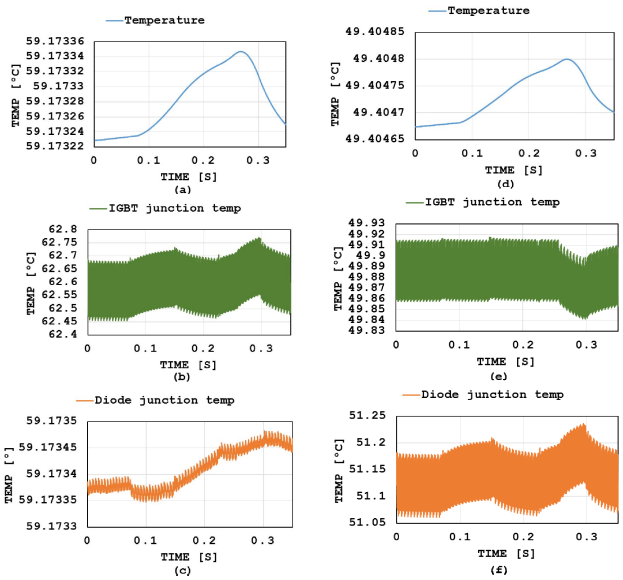

Fig. 11. Steady-state analysis results with natural air cooling: (a) heat sink temperature of the primary bridge, (b) IGBT's junction temperature of the primary bridge, (c) junction temperature of diode in the primary bridge, (d) heat sink temperature of the secondary bridge, (e) IGBT's junction temperature of the secondary bridge, (f) junction temperature of diode in the secondary bridge

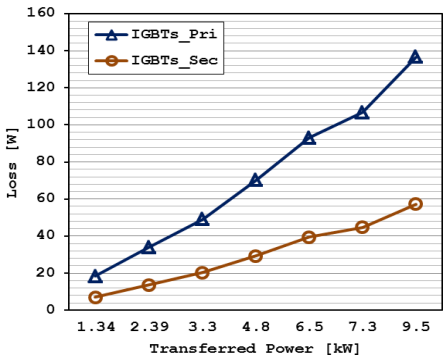

Fig. 12. Power losses distribution of the 10kW 3DAB converter

The simulation results of the DC voltages and currents of the output terminals are shown in Fig. 10. The capacitor has the effect of smoothing the DC voltage. In the 10kW model, the capacitances C_{dc} are connected in parallel to the DC resistance load. Within this work, C_{dc}=500 µF is assumed. It can be seen that the dc link capacitance of the secondary side is 500 µF ensuring to be less than 5 %, so the ripple would be satisfactory for the application.

To verify the chosen heat sink, the PLECS simulation is run for steady-state analysis and the heat sink are measured temperature and junction temperatures of the diodes and IGBTs. The measured temperatures of the chosen heat sink and the semiconductors for the final converter are given in Fig. 11. The maximum junction temperatures of the IGBT's and diodes for the primary and the secondary bridge are simulated for an ambient temperature of 45°C. Accordingly, the maximum junction temperature of the secondary bridge semiconductors is lower than the one of the primary bridge semiconductors. Considering the worst case heatsink temperature of 90° for natural air cooling, the results are allowing the requirements. Loss distribution with different transferred power ratings are shown in Fig. 12. It is found that the IGBT device losses of the secondary bridge show by far the lowest losses compared to the IGBT devices of the primary bridge.

V. CONCLUSION

This paper presents an investigation of a snubber circuit topology for the high-power 3DAB converter that utilize the advantages of the aforementioned ZVS switching scheme. The snubber capacitors are required in order to achieve the desired reduction in voltage transients during turn-off switching commutation. Analysis revealed how snubber capacitor size must be adjusted to a specified minimum commutation time for each bridge, while employing higher capacitances led to extra power dissipation due to longer voltage transients. This paper also deals with a design and thermal management of a 10kVA 3DAB converter, having 500 and 1000VDC rated input & output voltages. The implementation was proved effective during the validation of the simulation model on a 1000V supply system at powers upto 10kW. Simulation results were presented with which to validate the operation of the 3DAB converter. Based on these results, a snubber capacitor of 10nF was selected for the primary side bridge, with a 6.8nF capacitance for the secondary bridge producing an optimal value for the corresponding power transfer. The power loss characteristics of the prototype converter obtained using the optimized snubber capacitances were then discussed. A converter efficiency of 94.2% was recorded at the full load amount to 9.5kW, while a maximum efficiency of 94.88% was achieved at 4.8kW load using the optimized snubber capacitors.

REFERENCES

[1] M. Stieneker and R. W. De Doncker, "Dual-active bridge dc-dc converter systems for medium-voltage DC distribution grids," *2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC)*, Fortaleza, 2015, pp. 1-6.

[2] A. Gómez-Expósito, J. M. Mauricio and J. M. Maza-Ortega, "VSC-Based MVDC Railway Electrification System," in *IEEE Transactions on Power Delivery*, vol. 29, no. 1, pp. 422-431, Feb. 2014.

[3] I. M. de Alegría, V. Santamarıa, A. Madariaga, J. L. Martín and S. Ceballos, "High power high voltage DC/DC converter for MVDC distribution applications," *International Symposium on Power Electronics Power Electronics, Electrical Drives, Automation and Motion*, Sorrento, 2012, pp. 1314-1319.

[4] Y. Lian, G. P. Adam, D. Holliday and S. J. Finney, "Medium-voltage DC/DC converter for offshore wind collection grid," in *IET Renewable Power Generation*, vol. 10, no. 5, pp. 651-660, 5 2016.

[5] J. Echeverría, S. Kouro, M. Pérez and H. Abu-rub, "Multi-modular cascaded DC-DC converter for HVDC grid connection of large-scale photovoltaic power systems," *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, Vienna, 2013, pp. 6999-7005.

[6] J. Echeverría, S. Kouro, M. Pérez and H. Abu-rub, "Multi-modular cascaded DC-DC converter for HVDC grid connection of large-scale photovoltaic power systems," *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, Vienna, 2013, pp. 6999-7005.

[7] H. Cha, R. Ding, Q. Tang, and F.Z. Peng,"Design and Development of High-Power DC-DC Converter for Metro Vehicle System,"in *IEEE Transactions on Industry Applications,* vol.44, no.6, pp.1795-1804, Nov/Dec 2008.

[8] R. De doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," in *IEEE Transactions on Industry Applications*, vol. 27, pp. 63-73, Jan-Feb 1991.

[9] G.J. Su and L. Tang "A Three-Phase Bidirectional DC-DC Converter for Automotive Applications," in Proc. *Industry Applications Society Annual Meeting 2008, IAS'08*, pp. 1-7,2008.

[10] N. Soltau, H. Stagge, R. W. De Doncker and O. Apeldoorn, "Development and demonstration of a medium-voltage high-power DC-DC converter for DC distribution systems," *2014 IEEE 5th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Galway, 2014, pp. 1-8.

[11] Y. Lee, G. Vakil, R. Feldman, A. J. Watson and P. W. Wheeler, "A high-power DC-DC converter based dual active bridge for MVDC grids on offshore wind farms," *2016 18th European Conference on Power Electronics and Applications* (EPE'16 ECCE Europe), Karlsruhe, 2016, pp. 1-10.

[12] S.P. Engel, N.Soltau, H.Stagge and R.W. De Doncker,"Improved Instantaneous Current Control for High-Power Three-Phase Dual-Active Bridge DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol.29, no.8, pp.4067-4077, Nov 2013.

[13] A. J. Watson, P. W. Wheeler and J. C. Clare, "Field programmable gate array based control of Dual Active Bridge DC/DC Converter for the UNIFLEX-PM project," *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, Birmingham, 2011, pp. 1-9.

[14] F. Krismer and J. W. Kolar, "Efficiency-Optimized High-Current Dual Active Bridge Converter for Automotive Applications," in *IEEE Transactions on Industrial Electronics*, vol. 59, no. 7, pp. 2745-2760, July 2012.

[15] Y. Lee, G. Vakil, A. J. Watson and P. W. Wheeler, "An analytical modeling and estimating losses of power semiconductors in a three-phase dual active bridge converter for MVDC grids," *2017 IEEE Power and Energy Conference at Illinois (PECI)*, Champaign, IL, USA, 2017, pp.1-8.