Using Multi Time-Scale Electro-thermal Simulation Approach to Evaluate SiC-MOSFET Power Converter in Virtual Prototyping Design Tool

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***Abstract*—Using virtual prototyping (VP) design tool to evaluate power converter electro-thermal performance can help designers to validate prototype in a quick way. However, different system time-scale requires efficient electro-thermal simulation techniques. Thus, an approach by using average power losses of one switching cycle is presented in the paper to decouple electrical and thermal simulation so as to evaluate the influence of the parasitic inductance on device junction temperature quickly. This approach is validated by comparing with a method to obtain device junction temperature by using instantaneous power losses. By implementing it in the VP design tool, where a SiC-MOSFET behavioural model is developed and validated, it is shown the parasitic inductance influence on power converter electro-thermal waveforms. Thus, designers can evaluate power converter electro-thermal performance more quickly than other commercial software.**

***Keywords*—Virtual prototyping; Multi time-scale; Electro-thermal simulation; SiC-MOSFET; Parasitic inductance; Switching losses**

I. Introduction

With high operation temperature, fast switching transition and low ON-state resistance, wide bandgap power semiconductor devices can help power electronics engineers to design high power-density power converters. The ability of evaluating power converter electro-thermal performance in simulation tool is important, because it helps designers to choose power converter EMI filter and cooling system size in a quick way.

An important requirement for this kind of virtual prototyping (VP) design tool is that it can predict accurate power semiconductor device switching transitions, which is important to design EMI filter and to obtain device losses. Meanwhile, it can predict accurate device thermal path, which is important to obtain device temperature.

There are following methods to obtain device electro-thermal waveforms: one method is to use device instantaneous power losses as that presented in [1]. The advantage of this method is that device junction temperature T_{j} and the influence of device switching losses on T_{j} can be accurately observed. However, time-scale of wide bandgap device switching transition can be as short as a few nanoseconds. In contrary, power converter thermal constant can be as long as a few minutes. This system time-scale mismatch requires a huge quantities of simulation data and simulation time.

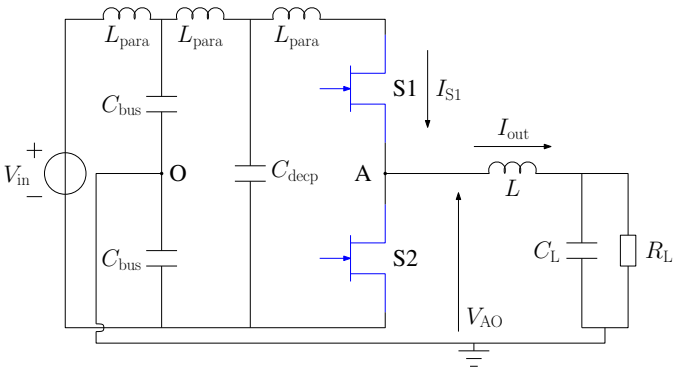
To accelerate simulation speed, one method is to use an average power losses of one switching cycle as that presented by authors in [2], [3]. The advantage of this method is that time scale can be increased to microseconds or milliseconds, so fewer points and time are needed than the previous method. However, as device switching losses is averaged, its influence on device T_{j} can not be observed. Furthermore, in [2], [3], power losses are predetermined and used in a lookup table, in which the influence of converter parasitic inductances L_{para} on T_{j} is not considered.

In order to overcome the drawback of the above methods, another method using instantaneous power losses for power devices and averaged power losses to determine system heat convection coefficient is presented by authors in [4]. It is focused on optimizing chip size of used power semiconductor devices in this work, where the influence of L_{para} on device losses is not presented.

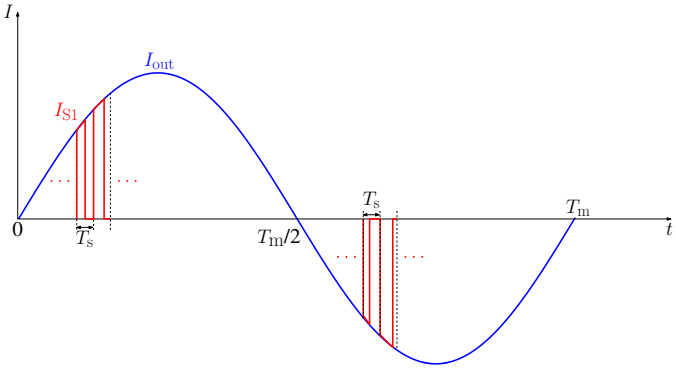
In the above literatures, silicon power semiconductor devices are chosen as experimental demonstrations. L_{para} may not be critical to consider as device switches slowly. However, for wide bandgap power semiconductor devices, they switch much faster than Si devices, therefore L_{para} may play an important role on device switching losses [5]. Thus, an efficient electro-thermal simulation technique to consider the influence of L_{para} on device switching losses and on device T_{j} is important in VP design tool, where a reliable power semiconductor device model with 3D electro-thermal geometry is necessary to be simulated in VP design tool. Therefore, designers can evaluate power converter electro-thermal performance by using the VP design tool.

Previous work on VP design tool frame and modelling power semiconductor device in it have been reported by authors in [6], [7], where it is shown that both thermal impedance and parasitic impedance can be accurately extracted in the proposed VP design tool. Thus, device switching losses can be accurately obtained. Based on those results, in this paper, it is focused on how to obtain device thermal waveforms in VP design tool in an efficient way.

The paper is structured with the following parts: a proposed approach by using average power losses of one switching cycle to solve multi time-scale simulation problem, which is at first presented and validated. Afterwards, the approach is

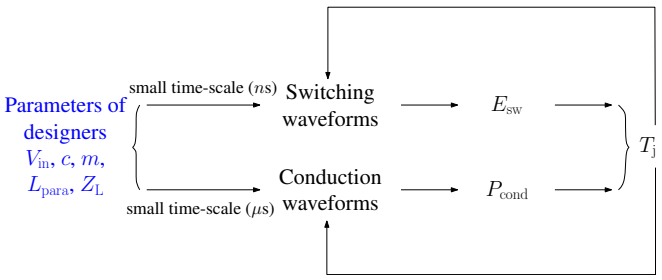


(a) Electrical circuit

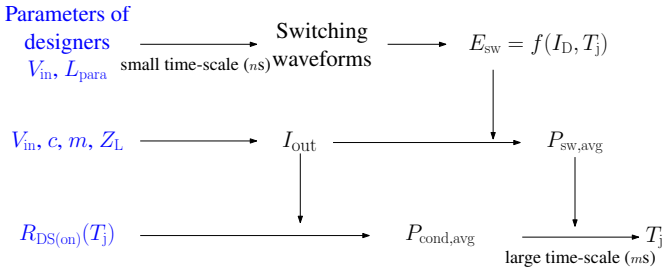


(b) Current waveforms

Fig. 1: Electrical circuit using to obtain device electro-thermal waveforms



(a) Method using instantaneous power losses



(b) Proposed method

Fig. 2: Flowchart to obtain device T_{j} by different methods

implemented in the VP design tool, where a SiC-MOSFET model is presented. Device switching and thermal waveforms are validated by the measurements. The influence of L_{para} on its electro-thermal waveforms is then shown when device operates in a single-phase sinusoidal PWM inverter. Conclusions are followed after those results at last.

II. Multi Time-Scale Electro-Thermal Simulation Approach

A. Proposed approach

An electrical circuit using to obtain device electro-thermal waveforms is shown in Fig. 1a, where it is a half bridge circuit with two SiC-MOSFETs (C2M0040120D, 1200V/60A). The switching unit is constituted by devices S1, S2 and decoupling capacitance C_{decp}. There exists parasitic inductance L_{para} of the switching unit due to the PCB tracks and device packaging. When applying sinusoidal PWM control signals, the circuit can be used as a single-phase inverter with near sinusoidal output current waveforms shown in Fig. 1b.

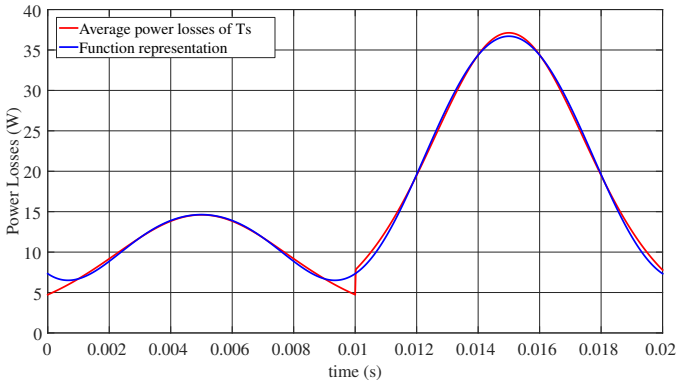
One method to obtain device junction temperature T_{j} is shown by the flowchart in Fig. 2a, where the input of the simulation tool is the parameters of the designers, such as input voltage V_{in}, load values Z_{L} (R, L, C), carrier waveform c with switching frequency f_{sw}, modulation waveform m with modulation frequency f_{out} and parasitic inductance L_{para}. Device power losses are obtained by instantaneous electrical simulation results, where device switching losses E_{sw} are obtained by using a small time-scale of a few ns to get accurate switching waveforms and conduction losses P_{cond} are obtained by using time-scale of a few μs to get device conduction waveforms. Device power losses are then used to estimate T_{j} , so thermal simulation is coupled with electrical simulation result.

It is to be noted that this method is used in the circuit simulator such as SPICE and in the system simulator such as PLECS, where the simulation time is limited to time-scale to obtain switching waveforms for the former type of the software and to conduction waveforms for the latter type of the software (where device switching losses are in a look-up table versus switching current). Nevertheless, the above time-scales are far below power electronics system thermal constant, which is usually superior to a few tens of seconds. As presented previously, the time-scale mismatch requires a huge quantity of data and simulation time to obtain device T_{j} when system reaches thermal steady-state.

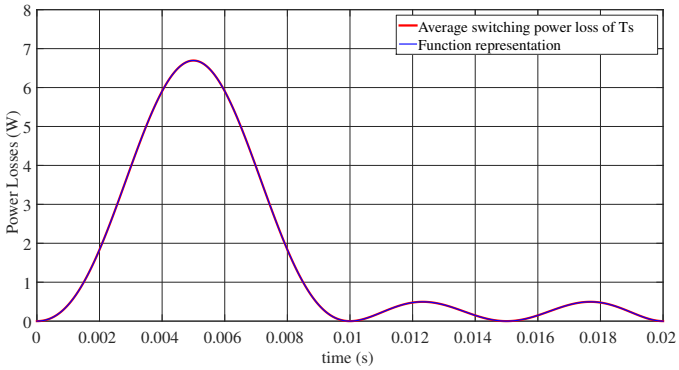
To accelerate simulation time, electro-thermal simulation is decoupled by the proposed method shown in the flowchart in Fig. 2b, where a small time-scale simulation of nanoseconds is running at first to determine device switching losses (turn-ON switching losses $E_{\text{sw,ON}}$ and turn-OFF switching losses $E_{\text{sw,OFF}}$) under different currents I_{D} and T_{j}. Therefore, a function showing the relation between device E_{sw} and I_{D}, T_{j} can be obtained:

$$E_{\text{sw}} = f(I_{\text{D}}, T_{\text{j}}) \tag{1}$$

By knowing designer parameters c and m of the control signals, device duty cycle $D(t)$ can be obtained by the



(a) Device S1 average switching losses



(b) Device S1 average conduction losses

Fig. 3: Device S1 averaged switching losses and conduction losses waveform of one T_{m}

equation below if devices are modulated by SPWM signals (M is modulation index).

$$D(t) = \frac{M}{2} sin(2 \cdot pi \cdot f_{\mathrm{mod}} \cdot t) + \frac{1}{2} \tag{2}$$

Thus, by combining with V_{in} and Z_{L}, I_{out} can be obtained by following equation:

$$I_{\mathrm{out}} = \frac{V_{\mathrm{AO}}}{Z_{\mathrm{L}}} = \frac{V_{\mathrm{in}} \cdot D(t) - \frac{V_{\mathrm{in}}}{2}}{Z_{\mathrm{L}}} \tag{3}$$

As illustrated in Fig. 1b, once I_{out} is known, device S1 and S2 switching current I_{S1} and I_{S2} of each switching cycle can be obtained. By combining the above two equations, device average switching losses $P_{\mathrm{sw,avg}}$ of one switching period T_{s} can be obtained by following equation:

$$\begin{aligned} P_{\mathrm{sw,avg}}(t) &= E_{\mathrm{sw}}(t) \cdot f_{\mathrm{sw}} \\ &= f(I_{\mathrm{out}}(t)) \cdot f_{\mathrm{sw}}, \qquad t = n \cdot T_{\mathrm{s}} \end{aligned} \tag{4}$$

By knowing device ON-state resistance $R_{\mathrm{DS(on)}}$ value, which is also a function of T_{j}, average conduction losses $P_{\mathrm{cond,avg}}$ of one T_{s} can be obtained by the following equation.

$$P_{\mathrm{cond,avg}}(t) = I_{\mathrm{out}}(t)^2 \cdot D(t) \cdot R_{\mathrm{DS(on)}}, \qquad t = n \cdot T_{\mathrm{s}} \tag{5}$$

Thus, device total average power losses $P_{\mathrm{total,avg}}$, which is with the same frequency f_{mod} as modulation wave, can be obtained, so a large time-scale of a few ms is used to obtain device T_{j}. It is to be noted that the influence of T_{j} on E_{sw} and P_{loss} is also included in the obtained $P_{\mathrm{total,avg}}$. In the proposed method, thermal simulation is decoupled from small time-scale simulation to get switching waveforms, so T_{j} can be obtained in a quicker way and the influence of L_{para} on device E_{sw} and T_{j} can be considered.

B. Validation

In order to validate the proposed approach, the above electrical circuit shown in Fig. 1 is simulated in LTSpice using SiC-MOSFET manufacturer model. Following parameter are used in the simulation: $V_{\mathrm{in}} = 600$V, $L = 380\mu$H, $C_{\mathrm{L}} = 2\mu$F, $R_{\mathrm{L}} = 22\Omega$, $f_{\mathrm{sw}} = 50k$Hz, $f_{\mathrm{mod}} = 50$Hz and $L_{\mathrm{para}} = 10n$H.

As shown in Fig. 1b the current waveforms of output current I_{out} and device S1 current I_{S1}, in the first half cycle from 0-$\frac{T_{\mathrm{m}}}{2}$, MOSFET S1 switches at different I_{out} and I_{S1} flows through MOSFET channel. While in the second half cycle from $\frac{T_{\mathrm{m}}}{2}$-T_{m}, body diode of S1 switches at different I_{out} and I_{S1} flows through body diode, yielding different switching and conduction losses.

By averaging device power losses of one T_{s}, the obtained S1 power losses waveforms are shown in Fig. 3 for a period of T_{m}. The obtained power losses can then be represented by the mathematical functions in the form of a series of sinusoidal functions plus DC component in order to be used in the simulation. The amplitude of each sinusoidal function is T_{j} dependent to include its influence on device power losses.

Device T_{j} can then be obtained, where the comparison between the above two methods is shown in Fig. 4, which shows that device T_{j} obtained by the proposed method using average power loss corresponds well with the results when it is obtained by small time-scale simulation on instantaneous power losses. The time to obtain the above results by using instantaneous power losses is about 1600s while the time using proposed method is a few seconds, which proves the effectiveness of the proposed method. It is also shown in the results that the influence of device E_{sw} on its T_{j} is small (less than 0.2°C). Therefore, the proposed method is suitable for wide bandgap power semiconductor devices, whose E_{sw} is much smaller than Si devices.

The proposed approach is then implemented in the VP design tool, where SiC-MOSFET electro-thermal waveforms are presented.

III. SiC-MOSFET Power Converter Electro-Thermal Performance Evaluation in Virtual Prototyping Design Tool

A. SiC-MOSFET modelling in virtual prototyping design tool

Power electronics systems can be virtually represented in the VP design tool. Different components of the half-bridge circuit shown in Fig. 1a are modelled by different modelling techniques in the VP design tool. For the parts like PCBs and heatsinks, they are represented by their physical models

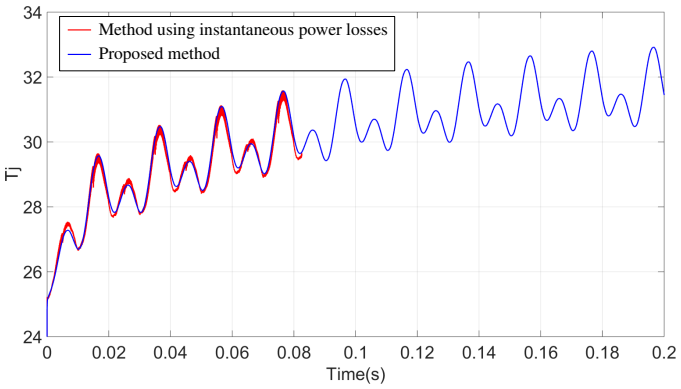
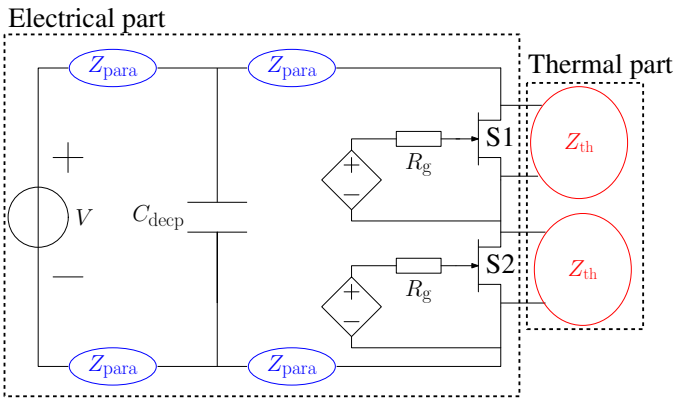
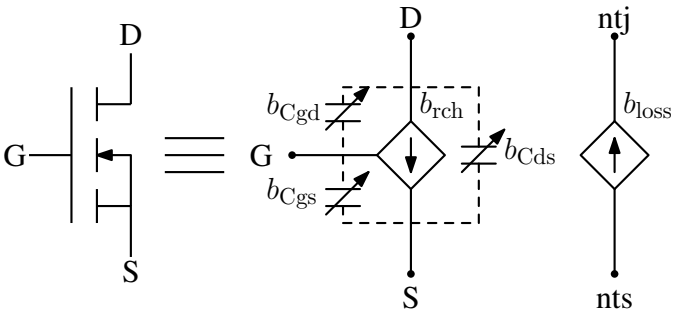


Fig. 4: Device T_{j} comparison by different methods



(a) Z_{para} and Z_{th} modelling



(b) SiC-MOSFET modelling

Fig. 5: Modelling a half-bridge circuit in VP design tool

which capture their 3D geometry and materials, because they can determine both parasitic impedance (Z_{para}) and thermal impedance (Z_{th}) of the system, which influence further power converter electro-thermal performance. In the developed VP design tool, Partial Element Equivalent Circuit (PEEC) method is used for electromagnetic simulation while Finite-Difference Method (FDM) is used for thermal simulation.

For the passive device such as capacitor and active device such as power semiconductor device and their gate drivers, they can be represented by behavioural models, because their dimensions are normally fixed. A 1200V/60A SiC-MOSFET (C2M0040120D) is modelled in the design tool by using a behavioural model as that presented in [7], where an equivalent

TABLE I: Parameters using in eq.(6) to model device I_{D}-V_{DS} characteristics (various units without physical meaning)

a	b	c	d	e	f	g
15.09	7.52	2.25	0.004	1.49	0.9	1

TABLE II: Parameters using in eq.(7) to model device C-V_{DS} characteristics (various units without physical meaning)

ac	bc	cc	dc	ec	fc	gc	hc
8.57×10^{-10}	18.1	0.27	7.53	0.5	1.9×10^{-9}	2	0.47

circuit is shown in Fig. 5b. Branches $b_{\mathrm{C_{gd}}}$, $b_{\mathrm{C_{gs}}}$, $b_{\mathrm{C_{ds}}}$ and b_{rch} with electrical nodes D, G and S represent device electrical characteristics; while branch b_{loss} with electrical nodes ntj and nts represent device thermal characteristics.

Following equations are used to express device I_{D}-V_{DS} and C-V_{DS} characteristics, where the parameters in those equations can be obtained by fitting method and they are given in TABLE I and TABLE II.

$$\begin{aligned} I_{\mathrm{d1}} &= a \cdot log(1 + exp(\frac{V_{\mathrm{GS}} - b}{c}))^{e} \cdot (1 + d \cdot V_{\mathrm{DS}}) \\ I_{\mathrm{d2}} &= -a \cdot log(1 + exp(\frac{V_{\mathrm{GS}} - b - f \cdot (V_{\mathrm{DS}})^{g}}{c}))^{e} \\ &\quad \cdot (1 + d \cdot V_{\mathrm{DS}}) \\ I_{\mathrm{D}} &= I_{\mathrm{d1}} + I_{\mathrm{d2}} \end{aligned} \tag{6}$$

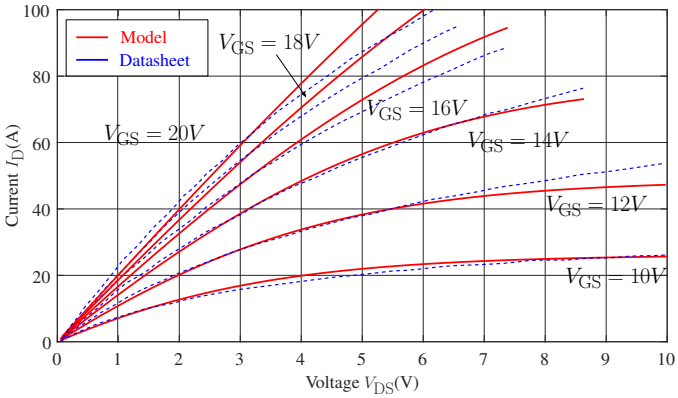
$$\begin{aligned} C_{\mathrm{gd}} &= ac \cdot \\ &\quad (1 + V_{\mathrm{DS}} \cdot (1 + bc * \frac{1 + tanh(cc * (V_{\mathrm{DS}} - V_{\mathrm{GS}}) - dc)}{2}))^{-ec} \\ &\quad + 1e - 12 \\ C_{\mathrm{ds}} &= \frac{fc}{(1 + \frac{V_{\mathrm{DS}}}{gc})^{hc}} \\ C_{\mathrm{gs}} &= 1.88 \times 10^{-9} \end{aligned} \tag{7}$$

The comparison between the model and datasheet values on device characteristics are shown in Fig. 6, where they are represented generally well by the model.

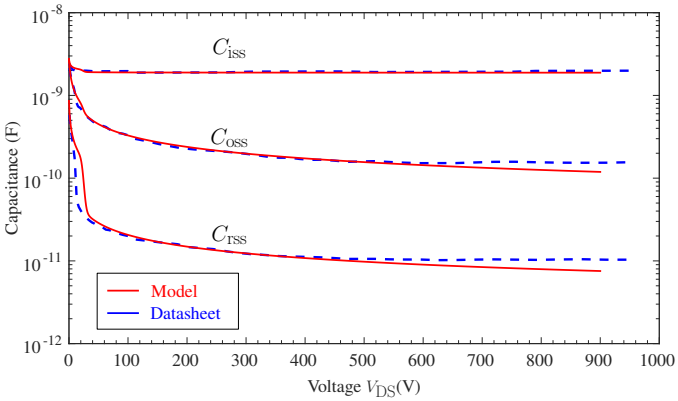
Behavioural and physical models in the VP design tool are linked by electrical and thermal boundaries for electrical and thermal simulation. Model order reduction (MOR) technique is applied to reduce the number of equations generated by the physical model in order to accelerate simulation speed [6]. It is applied a PRIMA algorithm [8] for electromagnetic order reduction and an Arnoldi MOR algorithm [9] for thermal order reduction.

B. SiC-MOSFET model validation

As shown in Fig. 7, a virtual prototype of SiC-MOSFET half bridge circuit is built in the VP design tool to represent the real prototype. PCB tracks, heatsink and device packages are modelled by giving their geometries in the VP design tool. Other parts such as C_{bus}, load, SiC-MOSFETs and their

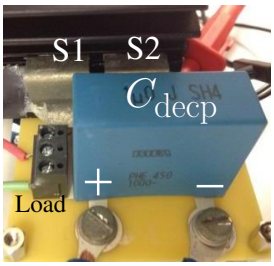


(a) I_D-V_{DS} characteristics

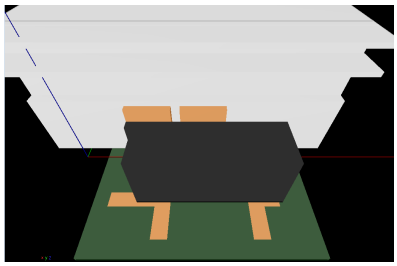


(b) C-V_{DS}

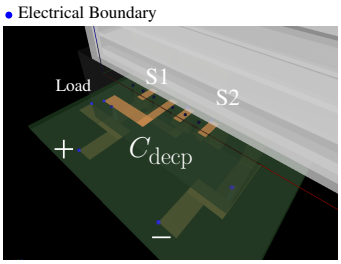
Fig. 6: Comparison between the model and the datasheet values on device I_D-V_{DS} and C-V_{DS} characteristics



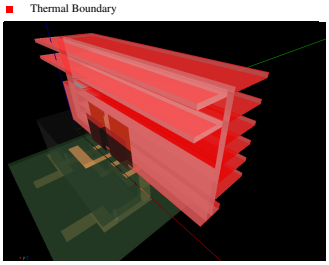
(a) Real prototype



(b) Virtual prototype



(c) Electrical boundaries linking physical model and behavioural model



(d) Thermal boundaries linking physical model and behavioural model

Fig. 7: SiC-MOSFET half bridge real prototype and virtual prototype

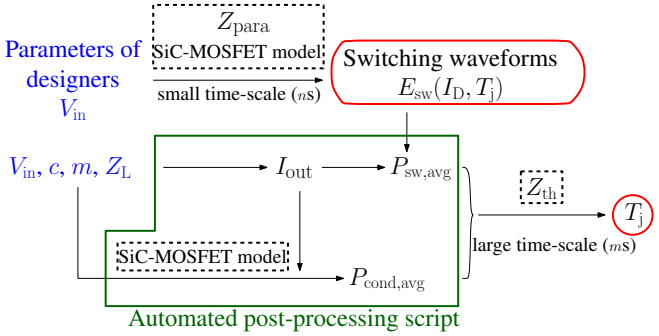


Fig. 8: Flowchart to obtain power converter electro-thermal waveforms in VP design tool

associated gate drivers are modelled by using behavioural models in the form of the equivalent circuits.

As shown in Fig. 7c and in Fig. 7d, electrical boundaries and thermal boundaries are used to link physical model and behavioural model for electro-thermal simulation.

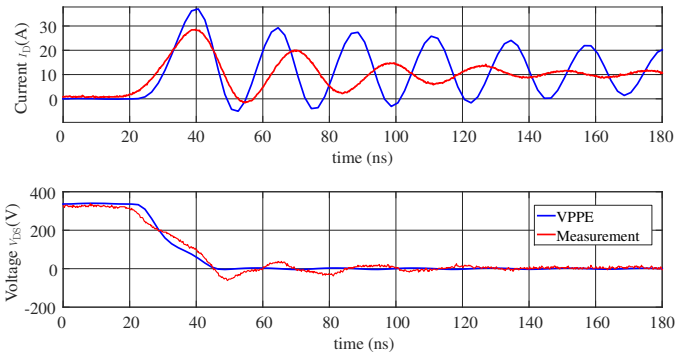
The flowchart to obtain power converter electro-thermal waveforms in VP design tool is illustrated in Fig. 8. VP design tool is able to generate Z_{para} of the switching loop (mainly parasitic inductance L_{para} is considered). Using the presented SiC-MOSFET model, device electrical switching waveforms can be obtained under different I_{out} by a small time-scale simulation. An automated post-processing script using the presented multi time-scale approach is applied to obtain $P_{\text{sw,avg}}$ and $P_{\text{cond,avg}}$, whose values are used in thermal branch b_{loss} of the model (see Fig. 5b). Therefore, a large time-scale is used to obtain device T_{j} waveforms by using Z_{th} generated by the VP design tool.

When $V_{\text{in}} = 300$V, the comparison between the simulation and measurement on device switching waveforms when it switches at $I_{\text{D}} = 10$A (external gate resistance is 10Ω) and $I_{\text{D}} = 15$A (external gate resistance is 0Ω) is shown in Fig. 9 and in Fig. 10 respectively, where good switching transitions and resonance frequency are represented, which shows a reliable device model and accurate extraction of switching loop L_{para} in the design tool.

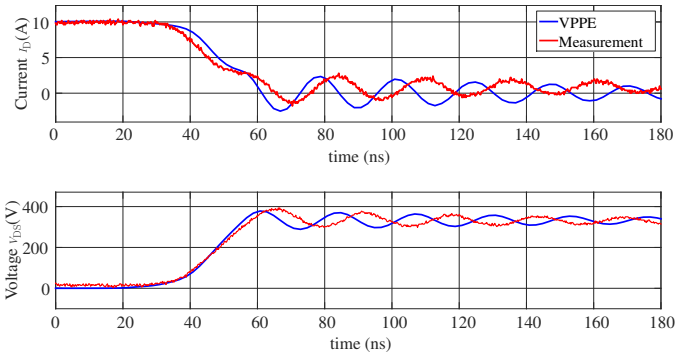
When external gate resistance is 10 Ω, devices total switching losses when it switches at 200V and 300V can then be obtained. It is shown in Fig. 11 the comparison between the measurement and the simulation, where E_{sw} of the measurement is estimated accurately in the VP design tool.

In order to validate device thermal waveforms, the presented power converter is operated in buck mode, in which S1 is in hard turn-ON and turn-OFF switching and S2 serves as a synchronous rectifier. device S1 is switched at 50kHz and with a constant duty cycle 25%. Dead time of control signals of S1 and S2 is set to be $150ns$. Power losses of S1 is estimated to be $P_{\text{loss,S1}} = P_{\text{loss,sw}} + P_{\text{loss,cond}} = 1 + 0.25 = 1.25$W and Power losses of S2 is estimated to be $P_{\text{loss,S2}} = P_{\text{loss,sw}} + P_{\text{loss,cond}} = 1 + 0.9 = 1.9$W (including the influence of dead time).

The comparison between the measurement and the sim-

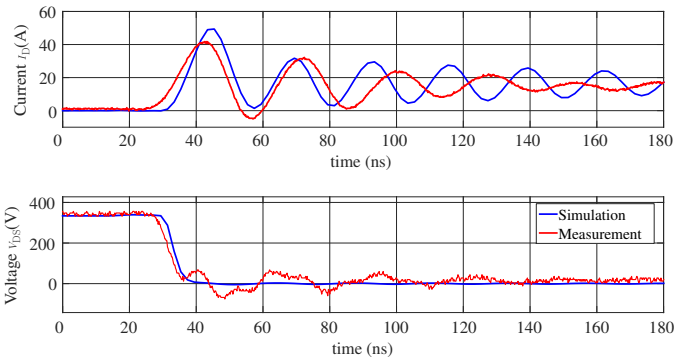


(a) Turn-ON switching at $V_{\mathrm{DS}} = 300\mathrm{V}$, $I_{\mathrm{D}} = 10\mathrm{A}$

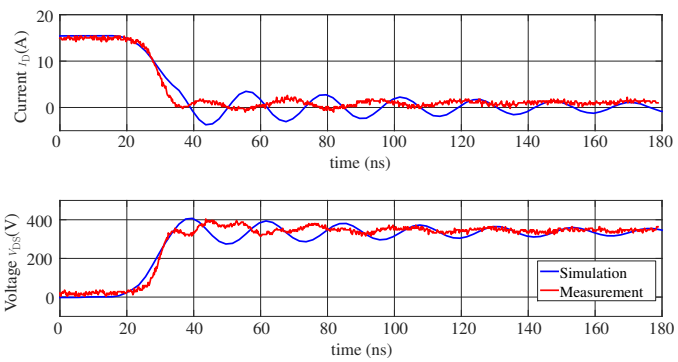


(b) Turn-OFF switching at $V_{\mathrm{DS}} = 300\mathrm{V}$, $I_{\mathrm{D}} = 10\mathrm{A}$

Fig. 9: Comparison between the simulation and measurement when device switches at $V_{\mathrm{DS}} = 300\mathrm{V}$, $I_{\mathrm{D}} = 10\mathrm{A}$



(a) Turn-ON switching



(b) Turn-OFF switching

Fig. 10: Comparison between the simulation and measurement when device switches at $V_{\mathrm{DS}} = 300\mathrm{V}$, $I_{\mathrm{D}} = 15\mathrm{A}$

ulation on device and using heatsink temperature is shown in Fig. 12b, where temperature is measured by an infrared thermal camera in experiment and boundary condition is set to be natural cooling in simulation (with convection coefficient $10\mathrm{W}/\mathrm{m}^2{\cdot}^\circ\mathrm{C}$). As shown in the mapping temperature colour-bar, the difference between the measurement and simulation on obtained device and heatsink temperature is within 2°C, which shows an accurate estimation of heatsink thermal impedance Z_{th}. In order to compare packaging temperature with the measurement, detailed device packaging as that shown in [10] can be modelled in the VP design tool.

C. L_{para} influence on power converter electro-thermal performance

In order to investigate on L_{para} influence on power converter electro-thermal performance, device electro-thermal waveforms of two positions are compared. In position 2, distance between S1 and S2 is increased to 1cm more than its original position (position 1) shown in Fig. 7a.

When $V_{\mathrm{in}} = 600\mathrm{V}$ and $I_{\mathrm{out}} = 10\mathrm{A}$, device switching waveforms of the two positions are compared in Fig. 13, where it is shown that as distance between devices S1 and S2 increases, the L_{para} of the switching unit increases, causing a slower switching transition and LC resonance frequency. Device switching losses are then compared in Fig. 14 between the two positions. In position 2, as L_{para} increases, device V_{DS} voltage drop increases during turn-ON transition. Therefore,

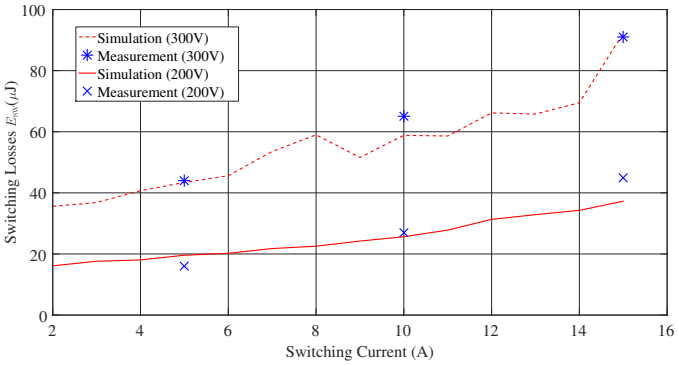
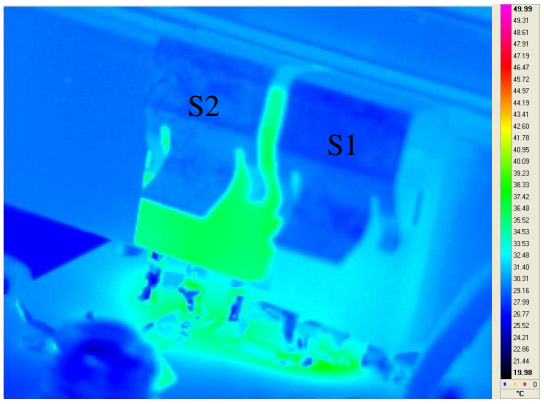


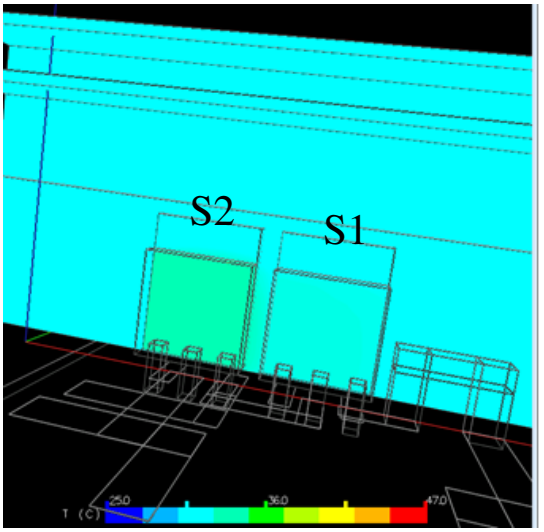
Fig. 11: E_{sw} comparison between the simulation and the measurement

turn-ON switching losses ($E_{\mathrm{sw,ON}}$) due to the overlap of V_{DS} and I_{D} decreases in position 2 because of this snubber effect of L_{para}.

Device losses and its T_{j} of the two positions are then compared when they are operated in a sinusoidal PWM modulated DC-AC inverter (same parameters as presented in section II-B), in which the results are presented in Fig. 15. As two devices operate in a sinusoidal PWM inverter, one device has more losses than the other at one half period of modulation wave. As devices have less E_{sw} in position



(a) Measurement results



(b) Simulation results

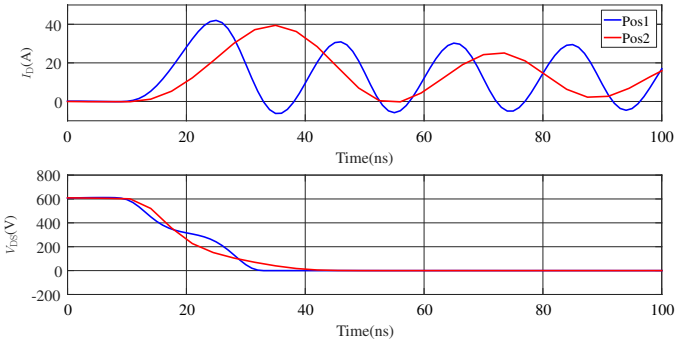
Fig. 12: Comparison on device temperature between the measurement and the simulation

2, their T_{j} are estimated to be 8°C less than position 1. Obtained device T_{j} and heatsink temperature in the VP design tool of the two positions are illustrated in Fig. 16. Even though the increase of L_{para} in the switching unit lowers down device T_{j} and heatsink temperature, it might lead to electromagnetic interference problem, which will be analyzed in future communications.

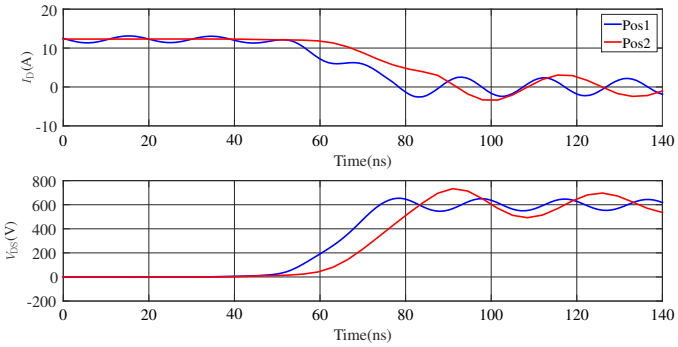
Simulation time to obtain the above electro-thermal waveforms are about 6mins, which includes generating electro-thermal equations, applying MOR to reduce equation size, $1ns$ time-scale to obtain device switching losses under different currents and $1ms$ time-scale to get device T_{j} waveform until thermal steady state (1000s). This helps designers to obtain results more quickly than SPICE-type (Z_{para} and Z_{th} need to be predetermined) and Ansys-type (device losses need to be predetermined) simulation software.

IV. Conclusion

A multi time-scale simulation approach is proposed in the paper to decouple electrical and thermal simulation. In this approach, device switching losses E_{sw} by taking into account of the influence of parasitic inductance L_{para} is at first obtained by a small time-scale simulation. Afterwards, device power losses waveform, which is as the same frequency as power converter modulation waveform, can be obtained by averaging its switching losses and conduction losses of one switching period. Therefore, thermal simulation is decoupled from electrical simulation, so simulation speed is accelerated to obtain power converter electro-thermal waveforms. This approach is validated to estimate device junction temperature



(a) Turn-ON switching



(b) Turn-OFF switching

Fig. 13: Comparison between the device switching waveforms of different positions at $V_{\mathrm{DS}} = 600\mathrm{V}$, $I_{\mathrm{D}} = 10\mathrm{A}$ in VP design tool

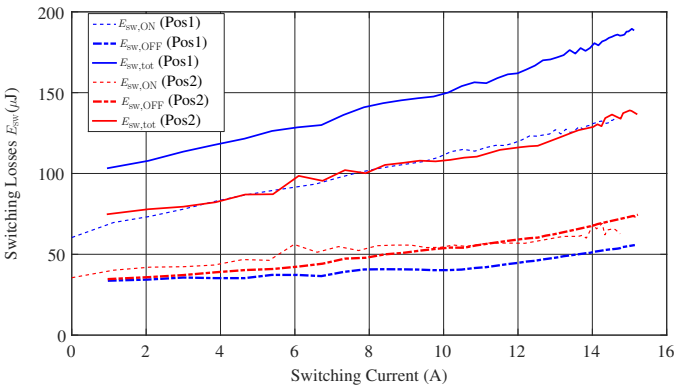


Fig. 14: Device switching losses comparison of different positions in VP design tool

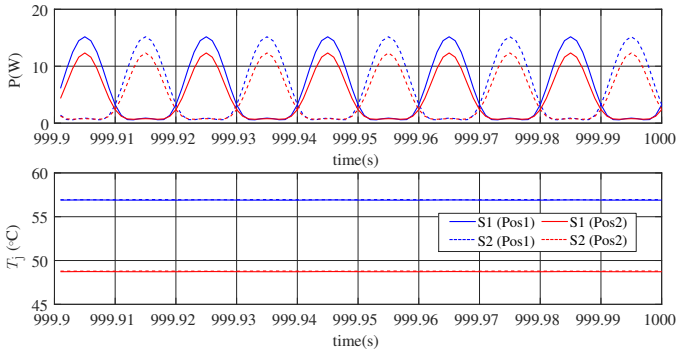


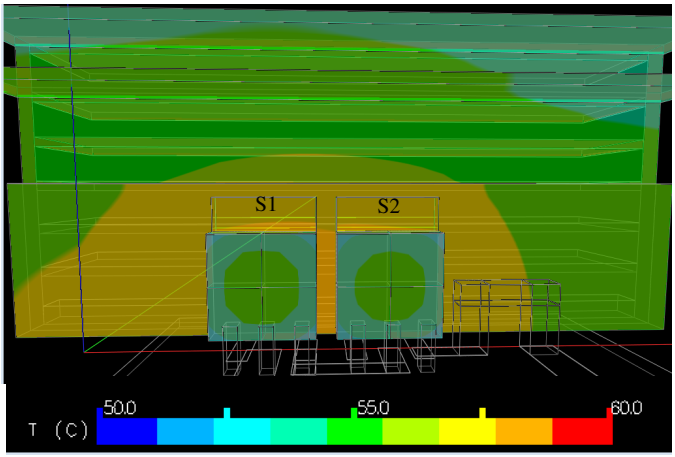
Fig. 15: Estimated device $P_{\text{total,avg}}$ and T_{j} in VP design tool

T_{j} by comparing with a method, where thermal result is based on device instantaneous power losses of electrical simulation.

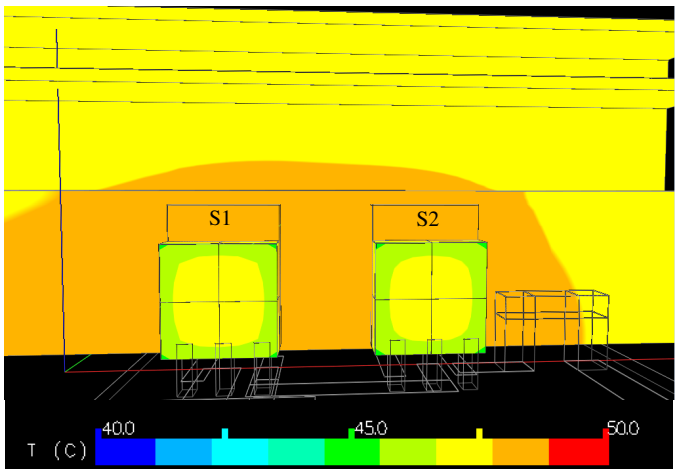
The approach is then implemented in a virtual prototyping (VP) design tool, in which a SiC-MOSFET behavioural model is developed. By comparing with the measurement on device switching waveforms and device temperature, it is shown that the presented SiC-MOSFET device model together with the 3D electro-thermal geometry is reliable to estimate power converter electro-thermal waveforms in the VP design tool.

Following by that, a SiC-MOSFET sinusoidal PWM modulated DC-AC inverter is evaluated by using the developed VP design tool. Distances between two devices in the switching unit is increased to 1cm more than their original positions, which brings more L_{para} in the switching unit. When L_{para} increases, device E_{sw} decreases because of this snubber effect, resulting in lower T_{j} and heatsink temperature when system reaches thermal steady-state.

By using the proposed multi time-scale approach in the VP design tool, simulation time to obtain power converter electro-thermal waveforms are faster than SPICE-type and Ansys-type simulation softwares.



(a) Position 1



(b) Position 2

Fig. 16: Comparison on device T_{j} and heatsink temperature of different positions

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