Chip-on-Board assembly of 800V Si L-IGBTs for high performance ultra-compact LED drivers

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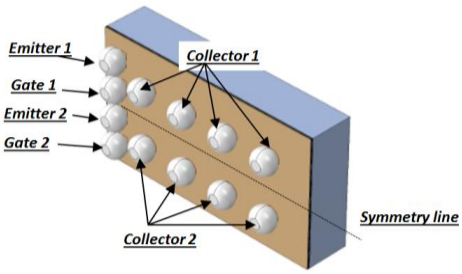
***Abstract*— This paper presents a novel chip on board assembly design for an integrated power switch, based on high power density 800V silicon lateral insulated-gate bipolar transistor (Si LIGBT) technology. LIGBTs offer much higher current densities (5-10X), significantly lower leakage currents, and lower parasitic device capacitances and, gate charge compared to conventional vertical MOSFETs commonly used in LED drivers. The higher voltage ratings offered (up to 1kV), the development of high voltage interconnection between parallel IGBTs, self-isolated nature and absence of termination region unlike in a vertical MOSFET makes these devices ideal for ultra-compact, low bill of materials (BOM) count LED drives. Chip on-board LIGBTs also offer significant advantages over MOSFETs due to high ambient temperatures seen on most of the LED lamps as the LIGBTs on-state losses increase only marginally with temperature. The design is based on a built-in reliability approach which focuses on a compact LED driver as a case-study of a cost-sensitive large volume production item.**

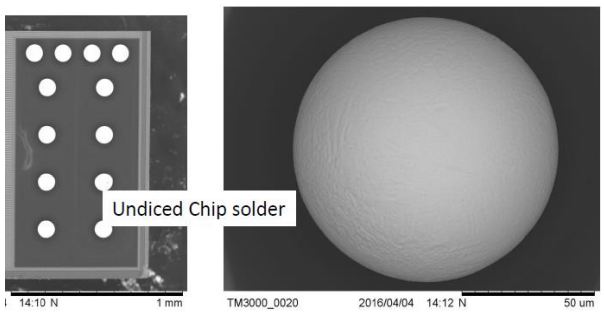
Keywords—chip-on-board; lateral IGBT; LED drivers; packaging; reliability.

I. INTRODUCTION

The semiconductor device design advances state-of-the-art by enabling realisation of significantly more compact solutions in size sensitive products such as LED lighting, mobile phones, implantable cardioverter defibrillators (ICDs) and tablet chargers[1, 2]. The advantage of high current density, low power losses and reduced device footprint has led to an increased attention towards these devices in high voltage low power applications [3]. To match the level of advancement associated with the chip technology and enable the full exploitation of its potential at application level, the assembly exercise targets the structural and functional integration of design elements to yield optimised electrical and thermal management of the chip. The significance of the contribution is: it delivers a methodology for developing highly integrated, reliable and cost-effective lateral Si-based power switches. As far as we are aware, this is the first time the lateral smart integrated chip together with a chip on board assembly are



(a)



(b)

Fig.1: (a) Terminal layout of two identical LIGBTs with a fully populated solder ball matrix on a silicon based substrate (b) scanning electron microscope (SEM) image of the LIGBT and solder balls

employed in an LED driver. The layout of the LIGBT device considered in this work is shown in Fig.1(a). An electron microscope is used capture the image of the device as shown in Fig.1(b). The size of the device is 744μm x 1345μm with the deposited solder balls that has a radius of just above 50 μm. This poses obvious thermal and electrical challenges, which need to be analysed in order to ensure reliable performance.

The layout of the fabricated LIGBT developed in 0.6μm/5V bulk silicon technology is shown in Fig.2(a). The cross section along A in Fig.2(a) reveals the 3 dimensional schematic of the

LIGBT device structure presented in Fig. 2(b). The LIGBT possesses a new design feature which is a floating N^+ layer

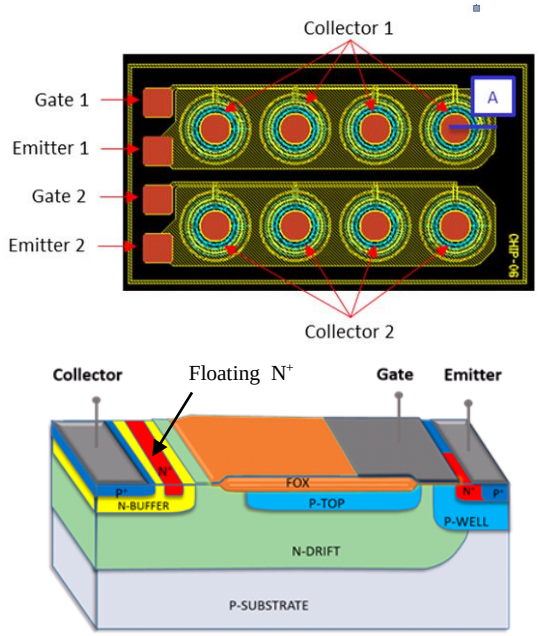


Fig.2: (a) Fabricated LIGBT in 0.6µm bulk silicon technology layout (b) 3D cross-section along A

next to collector P^+ [3]. This feature allows layout based tuning and minimisation of device losses based on the application. Based on this, an 800V LIGBT for high frequency, low-cost applications has been developed and implemented in low power high efficiency switch mode power supply (SMPS) systems[3]. This makes the LIGBT devices suitable for LED drivers.

II. PACKAGE THERMAL DESIGN

The ambient temperature in LED lamps makes it imperative to have an effective thermal package design for the devices. Just as it is important to ensure that the temperature of the devices is kept within limits, it is also of importance to ensure the heat generation in the device doesn't significantly increase the ambient temperature. This is due to the fact that the LED optical output is significantly affected by the temperature as presented in [4, 5]. In [5] the optical output was while altering the ambient temperature. The results show that the higher the ambient temperature the higher the number of non-radiative recombination of carriers and subsequently diminishing the light intensity[6, 7]. This emphasises the importance of a good thermal design.

Two possibilities were explored to package the LIGBT, the use of printed circuit boards (PCB) with modifications and the use of insulated metal substrate (IMS). The PCB package design for an effective cooling of the LIGBT is presented in Fig.3(a). The package is designed for optimal thermal performance using vias linking the device solder balls and top PCB copper layer to the base which can be used for cooling. An additional copper foil is used as a heatsink to extract heat from the backside of the device and the PCB copper layer.

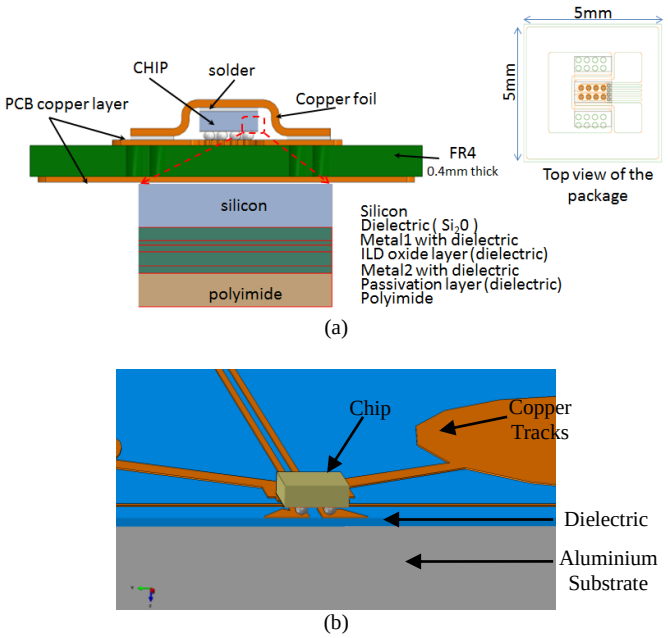


Fig.3: (a) PCB design for an effective cooling of LIGBT (b) IMS design for an effective cooling of LIGBT

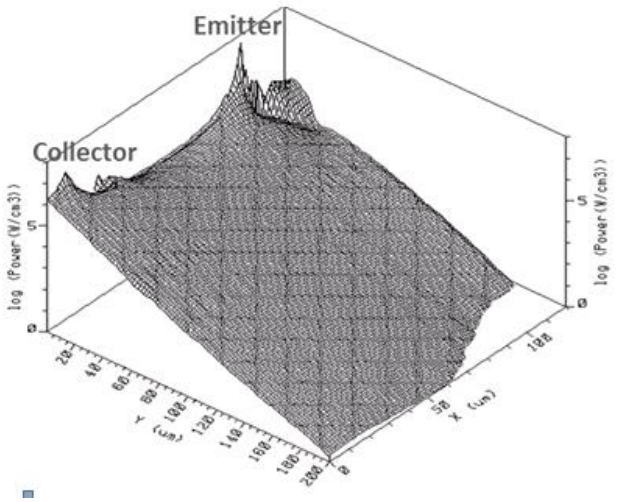


Fig.4: 3D plot of heat generation

Solder is used to attach the copper foil to the device backside to improve thermal performance. An alternative to PCB of reduced complexity is the insulated metal substrate (IMS) which is shown in Fig.3(b). The IMS consists of a copper layer which is used for electrical connection and also aids by thermally conducting the heat generated by the device. A dielectric material of typical thickness of 100µm is used to isolate the copper tracks electrically from the aluminium substrate. The aluminium substrate can be used as a heatsink.

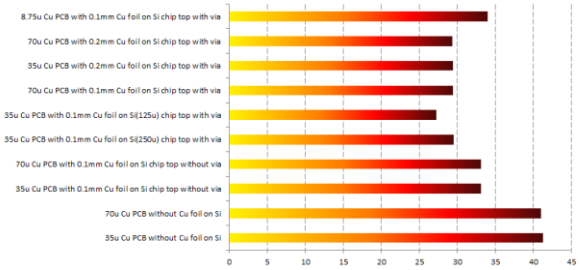
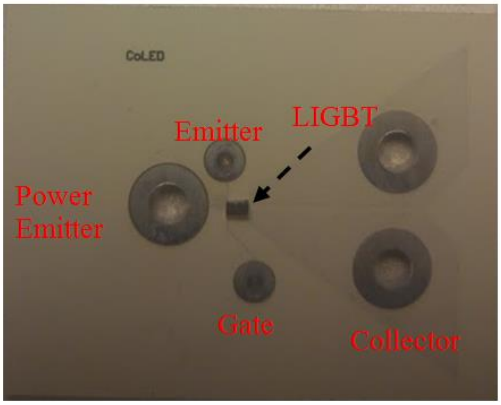
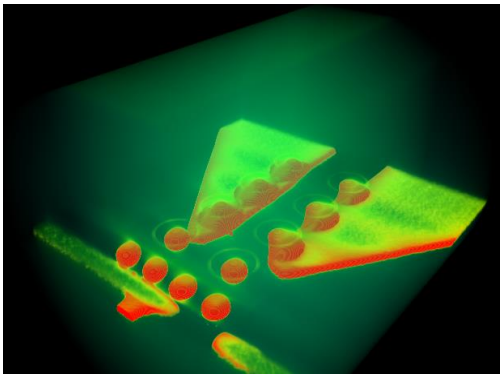


Fig.5: Steady state thermal simulation results on a linearly distributed body heat flux (applied across the thickness of silicon) for different packaging configurations.

An extraction of the heat generation profile shows that heat generation is highest at the terminals and linearly decreases as it moves deeper away from the device terminals as shown in Fig.4. By applying the heat profile in finite element analysis (FEA), different packaging configurations have been analysed by including and varying vias, copper foil as heat sink and the thickness of the PCB copper track thickness. The best thermal performance is achieved with 35µ PCB copper thickness, 0.1 mm copper foil and the inclusion of vias as shown in Fig.5. Design by static thermal simulation has produced very low device temperature (See Fig.5). The device is soldered on IMS using a die bonder by heating the IMS as well as the solder balls and camera aids to align the pads to the balls accurately (See Fig.6).



(a)



(b)

Fig.6: (a)Test sample soldered on IMS (b) X-ray image of the solder balls

III. THERMO-MECHANICAL MODELLING

Thermo-mechanical modelling of package structure of four circle LIGBT device was undertaken in order to predict the strain and stresses in the solder. The package components consists of four circle LIGBT device (device consist of aluminum metal layers, polyimide, SiO2 and Si substrate as in Fig 7.

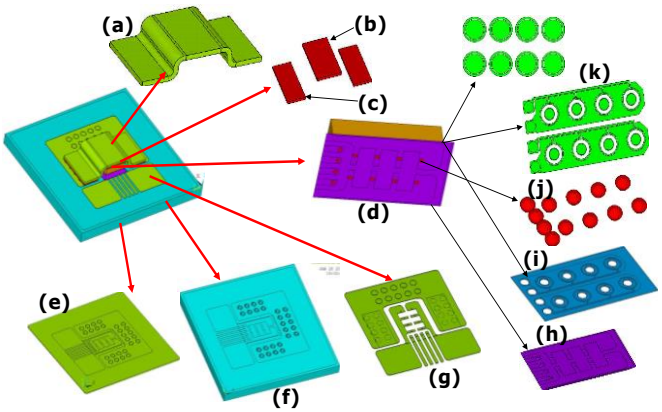


Fig.7: Components of package structure (a) Copper foil, (b) solder layer between copper foil and die, (c) solder layer between copper foil and PCB, (d) chip package, (e) copper layer on the bottom of the PCB, (f) PCB, (g) coper layer on top of the PCB, (h) underfill, (i) polyimide, (j) solder bump, and (k) aluminum layer

The solder viscoplastic properties were extracted from Cheng et al [8]. The standard temperature cycling with ramp and dwell time of 3 and 15 minutes with range of (-25, 125) was imposed on the model. The package structure was structurally restricted with three point structural boundary restriction constraint. Plastic strain distributions of solder were extracted from the numerical simulation. The plastic strain distribution of solder bump is shown in Fig 8. Accumulated plastic strain of solder bump, solder layer between copper foil and PCB, and the solder layer between copper foil and the silicon substrate were evaluated by volume weighted averaging of thin layer (10 µm) of the total volume. A Coffin Manson fatigue model [9] was utilised for lifetime of solder. It was noted that solder layer between copper foil and the silicon substrate has the worst lifetime with 1797 cycles to failure. This highlights one of the advantages of using the IMS over the PCB package.

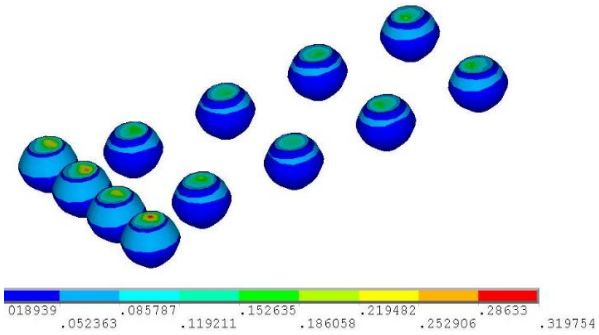


Fig.8: Plastic strain distribution on the solder bump

IV. UNDERFILL ELECTRIC FIELD MODELLING

The choice of under fill for flip-chip assembly is also important in the context of overall reliability. In order to optimise overall package construction detailed finite element models have been built to assess electric field distributions in the underfill for 'off' state of the package structure. The governing equation (Poisson equation) of the electro-static analysis is

$$\begin{aligned} \nabla E &= \frac{\rho}{\varepsilon} \\ \nabla \times E &= 0 \quad \Rightarrow \quad \nabla(\nabla V) = -\frac{\rho}{\varepsilon} \\ E &= -\nabla V \end{aligned} \tag{1}$$

Where E- electric field, V-electric potential, ε – permittivity of the medium, ρ- electric charge density. The material properties of device were sourced from public domain [10] for initial study. The permittivity values of underfill, solder (Sn3.5Ag), polyimide, SiO2, aluminum, Si die are respectively 3.6, 2, 3.2, 3.9, 1.6, and 11.8. The high voltage (600V) was applied on the collector and solder bumps and ground voltage (0V) was applied on the gate of the device. Higher electric field distribution was concentrated in the region close to polyimide/solder/underfill interface as in Fig.9(c) and 10(c). For underfill relative permittivity value of 3.6 F/m, the maximum electric field vector sum value of 27.5 V/μm was observed in the modelling as in Fig 9 (a).

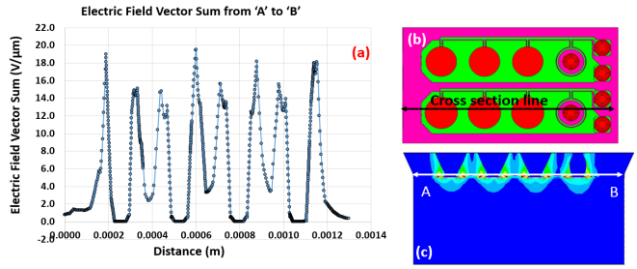


Fig 9: (a) Electric field vector sum versus distance from 'A' to 'B' across the solder bumps with 203.7μm PCB opening, (b) Top view of the cross section line, (c) electric field vector sum distribution on the side view.

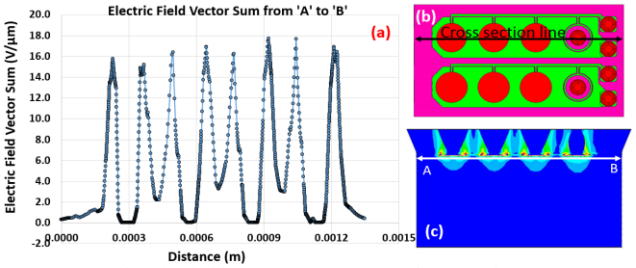


Fig 10: (a) Electric field vector sum versus distance from 'A' to 'B' across solder bumps with 192.3 μm PCB opening, (b) Top view of the cross section line, (c) electric field vector sum distribution on the side view

Two solder bump dimensions ((1) width (base) of 41.6 μm, and PCB opening of 192.3 μm, and (2) width (base) 57.2 μm, and PCB opening of 203.7 μm) measured in the experiment were modelled for electric static analysis. It was noted that the underfill region around the larger solder bump exhibit higher electric field distribution as in Fig 9 (a) and 10 (a). In addition, increase in relative permittivity value decrease the electric field in the underfill. If the maximum electric field is less than dielectric strength of the underfill then the underfill can withstand the breakdown failure. Two of the commercial underfill (manufactured by Henkel [11]) such as Loctite 3565 and Loctite 3563 are capable of withstanding dielectric breakdown failure to the extreme electric fields generated in the FEA model.

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