Full SiC Version of the EDA5 Inverter

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Abstract— **Recently, a novel hybrid multilevel inverter topology, the EDA5, was presented. The novel inverter topology comprises of two floating capacitors and 16 active switches to achieve five-level output voltage waveform and achieves higher efficiency at low-modulation index compared to a five-level Active Neural Point Clamped (5L-ANPC) converter. In this work, a full SiC MOSFET version of the inverter is presented, using commercially available 1200V rated devices. A balanced mix of simulation and experimental results are presented to point out the salient features of the topology. The topology is compared with 5L-ANPC inverter in simulation, and experimentally demonstrated up to 12kW output power with 1kV DC link voltage.**

Keywords—SiC MOSFETs; multilevel converter; hybrid single phase converter.

I. INTRODUCTION

Electricity generation from renewable energy sources such as wind, tidal, wave and solar has been one of the trending topics in power conversion research in order to reduce carbon emissions and dependency to limited fossil fuel supplies. Generating electricity by using photovoltaic panels and wind turbines has been one of the most studied topics. One of the main aims of the research in this area is increasing efficiency of the power electronics system that delivers the generated power from renewable sources to the grid.

Multilevel inverters have been discussed in literature as good candidates for high power conversion systems due to improved output voltage distortion, reduced voltage stress across power semiconductors and reduced filtering requirements [1-3]. The first multilevel converter designs were based on neutral point clamped (NPC) and flying capacitor (FC) based topologies. These two approaches have been proposed for three and higher number of voltage levels [2, 4]. At high number of voltage levels (five and more), NPC based inverters suffer from high semiconductor count, high conduction losses and asymmetrical semiconductor switching loss. On the other hand, FC based topologies require complex control schemes for balancing flying capacitors and high energy storage in floating capacitors [1, 2]. Due to the limitations of NPC and FC based topologies for high number voltage levels (five and above), various hybrid topologies have been introduced [5]. One of the most popular hybrid topologies is five-level active neutral point clamped (ANPC) inverter.

ANPC is a member of half-bridge neutral point clamped inverter family and it was introduced in [6] as an alternative to three-level NPC inverter for improved loss balancing and better utilization of semiconductor chip areas in the inverter. Replacing diodes in NPC inverters with active switches provides additional zero states, and at the same time different modulation strategies can be applied with a flexible utilization of the redundant switching states. The three-level ANPC topology is extended to five-level ANPC (5L-ANPC) in [7-9] and presented in Fig. 1. In Fig. 1 the 5L-ANPC converter is formed by 12 active switches and a floating capacitor C_{f1}, where the voltage of the floating DC link capacitor is maintained at one fourth of the main DC link voltage. Addition of the floating capacitor along with active clamping switches the topology can achieve five voltage levels (*+2E, +E, 0, -E, -2E*) across the load.

Similar hybrid five-level topology based on two floating capacitors and 14 active switches has been introduced in literature [10]. The floating capacitor voltages are kept at one fourth of DC link voltage and an inductor is used for limiting inrush current between DC link capacitors and floating capacitors due to voltage variation across floating capacitors. Another hybrid multilevel inverter concept called `Stacked Multicell Converter` (SMC) is discussed in [11, 12]. The concept is based on increasing number of voltage levels at the output of the converter by introducing floating capacitor and active switch based cells. In all three inverters discussed here has four series connected switching devices for every commutation loop thus the blocking voltage requirement of the power semiconductor devices reduced to one fourth of the main DC link voltage.

In this paper, a new five-level hybrid converter is presented. The converter topology comprise of 16 active switches, two floating capacitors and can achieve five level output voltage waveform across the load. The converter topology achieves higher efficiency than 5-level ANPC converter at lower modulation index due to redundant switching states. The proposed converter system is compared with 5-level ANPC converter using simulation platform along with the experimental results to validate the findings.

II. PROPOSED INVERTER TOPOLOGY

The proposed five-level inverter topology in this paper is based on a hybrid configuration of neutral-point-clamp and floating capacitors. The topology is named as 'Efficiency and Dense Architecture: EDA5' and filed for patent application [13]. The topology is formed by 16 active switches S_1-S_{10}, two floating capacitors C_{f1-2} and two DC-link capacitors C_{DC1-2}.

The schematic of EDA5 is shown in Fig. 2. Each switch in the converter is rated at E, one-fourth of the total DC link voltage *4E*. The charge state of floating capacitors C_{f1-2} is controlled by utilizing redundant states in order to keep capacitor voltages at E to achieve five-level output voltage waveform (*2E, E, 0, −E* and *−2E*).

A. Switching States

The switching states of the converter based on unity power factor operation are presented in Table I. Series connected switches such as S_{X1} and S_{X2} are switched on and off simultaneously, and therefore are represented as a single switch S_X in the switching state table. Single state is available for *+2E* and *−2E* output voltage levels while two states are available for *+E* and *−E* output voltage levels and three states are available for zero output state. The two switching states for *+E* and *−E* levels are achieved by introducing floating capacitors to the path of output current I_{OUT}. Depending on the polarity of output current and voltage, the floating capacitors are charged or discharged.
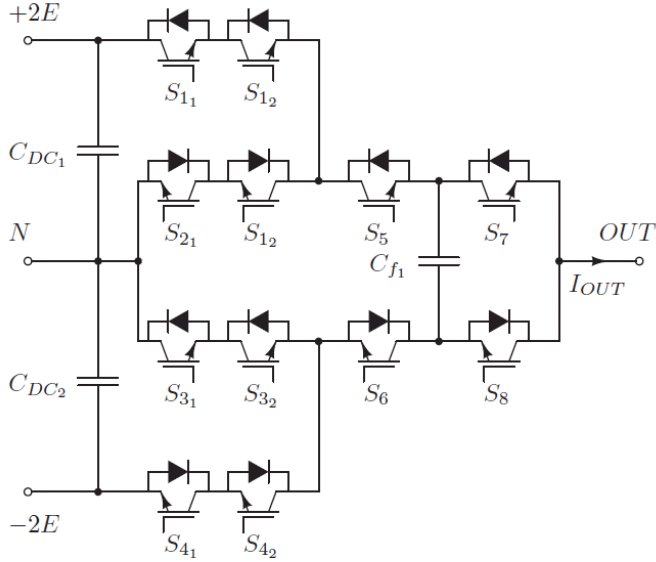

Fig. 1.   Active neutral point clamped five level converter.

In Table I, the switching states E_C and E_D define the charging and discharging states respectively for floating capacitors at unity power factor operation and inverter mode. To achieve zero output voltage, three possible states can be used: first, upper path 0_P can be formed by S_3, S_7 and S_9. The second path 0_N formed by S_4, S_8 and S_{10} finally, parallel path 0_X formed by simultaneous conduction of upper path 0_P and lower path 0_N. The main benefit of parallel zero state path 0_X is the reduction of conduction losses in the power cell during low modulation indexes or higher DC link voltages, where zero state conduction is dominant.

The current paths for four different switching states during positive half of output voltage for inverter mode are shown in Fig. 3. It can be seen from Fig. 2 and from Fig. 3 that four devices are conducting during all switching states except zero state 0_X where the output current is divided into two zero state branches. Charging or discharging state can be selected during *+E* and *−E* states in order to control the floating capacitor voltage to one fourth of the main DC link capacitor voltage. For example, during unity power factor operation for inverter mode, at *+E_C* state, switches S_1, S_3 and S_9 are turned-on in order to apply *+E* state to the output by subtracting floating capacitor voltage E from DC link capacitor voltage *+2E* while charging the floating capacitor. During *+E_D* state, the voltage across floating capacitor is applied to the output of the converter by turning on S_5 and S_7 switches. The charging or discharging status of a switching state can be defined by polarity of output voltage and direction of output current.
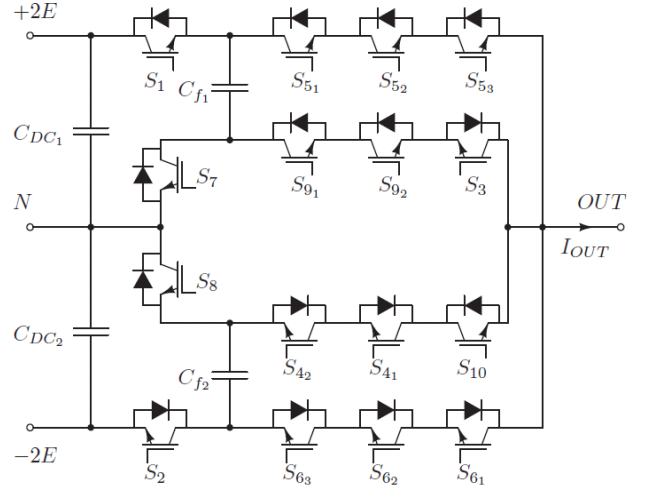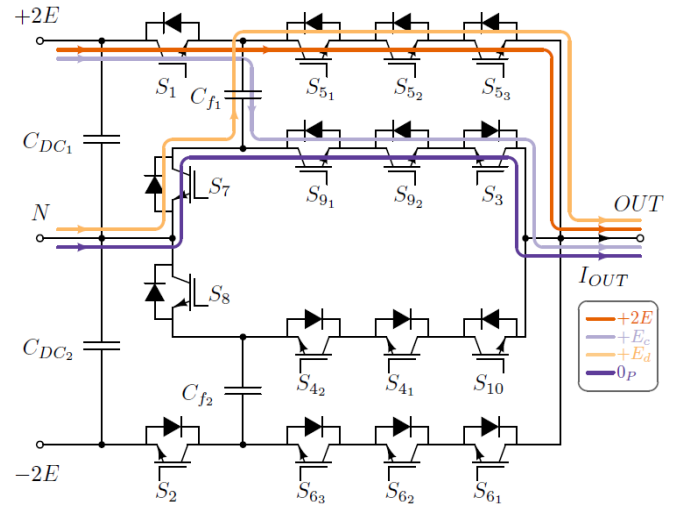

Fig. 2.   Proposed five level converter: EDA5.

Fig. 3.   Current paths for different switching states during positive half of the output voltage.

III.   COMMUTATION SCHEME

The commutation procedure between switching states, which are shown in Table I, has to be determined for transition of continuous output current from one state to another. The

possible commutation schemes for the positive half of the output voltage for positive and negative output current are shown in Fig. 4. The blue and red curves for V_{OUT} represents output voltage with positive and negative output currents respectively. Due to the nature of the topology, suitable commutations can be realized between $+2E$ and $+E_D$ or $+E_C$ and 0_P states. The commutation between $+E_C$ and $+E_D$ is not possible without clamping the output to another voltage state. In the first commutation scenario from $+2E$ to $+E_C$ in Fig. 4(a), S_9 switch is turned-on first, and after the dead-time period t_{dt}, S_5 is switched-off and finally S_3 switch is turned on. Depending on the direction of output current, the output voltage changes from $+2E$ to $+E_C$ state after t_{dt} or $2t_{dt}$. Commutation schemes in Fig. 4 (b), (c) and (d) have similar structure with Fig. 4 (a), and all of the schemes can be realised by applying logic gates to PWM signals coming from the controller.
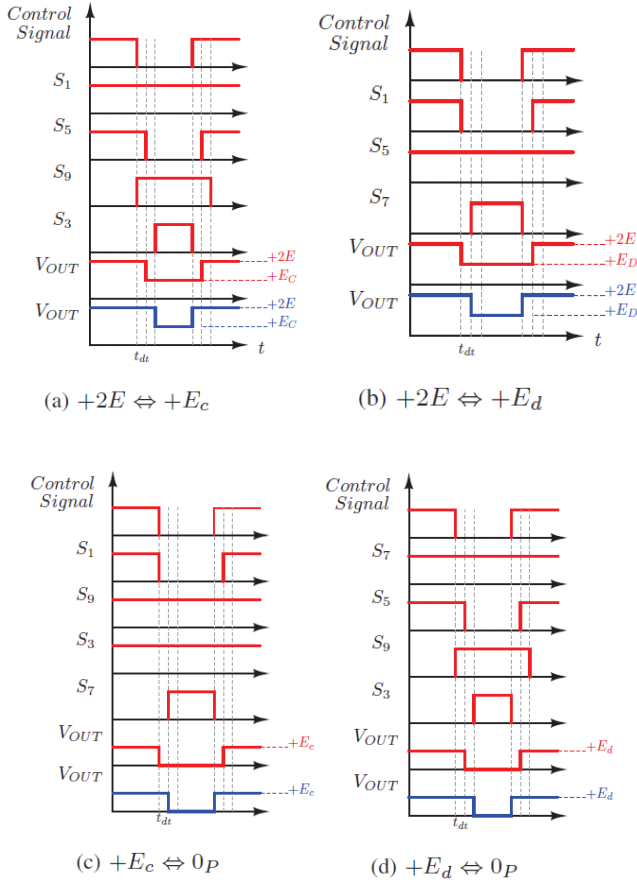

(a) $+2E \Leftrightarrow +E_c$ (b) $+2E \Leftrightarrow +E_d$

(c) $+E_c \Leftrightarrow 0_P$ (d) $+E_d \Leftrightarrow 0_P$

Fig. 4. Commutation scheme for EDA5 converter.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The proposed topology was simulated using PLECS simulation platform. To achieve results the main DC link voltage was set to 1kV and the floating inverters reference voltages were set to 250V. Switching frequency was set to 10kHz for all the operation points of the converter. The results are shown in Fig. 5 where a five level phase voltage can be seen along with the load current. The main and floating DC link voltages are shown in Fig. 6. It can be seen from the

results that the converter system is able to control the floating capacitor voltage and can achieve multilevel output voltage waveform. The semiconductor losses including conduction and switching losses were also calculated by fixing the modulation index and by varying output power from 1kW to 10kW, and the semiconductor losses are presented in Fig. 7. Finally, efficiency results of the power cell with these two topologies are also compared with varying modulation index and shown in Fig. 8. It can be seen from the figure that the proposed topology EDA5 has almost the same performance with 5L-ANPC topology with fixed modulation index, as shown in Fig. 7 and EDA5 provides higher efficiency at lower modulation index due to parallel conduction of SiC MOSFETs at zero states. The paralleling of devices at zero states brings the conduction losses by a factor of 4 as the conduction losses increase with the square of device current in unipolar devices, SiC MOSFET in this case. It should be noted that the dead-time between complimentary switches, which is 500ns in this case, is small in comparison to switching period (100µs), and therefore body diode conduction losses can be neglected.
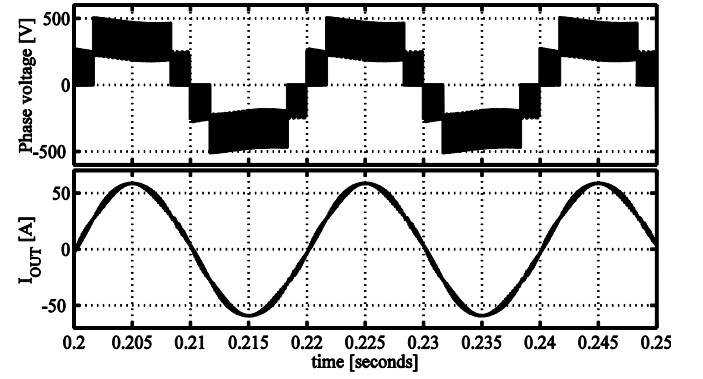

Fig. 5. Output voltage and current of the converter at 12kW output power.
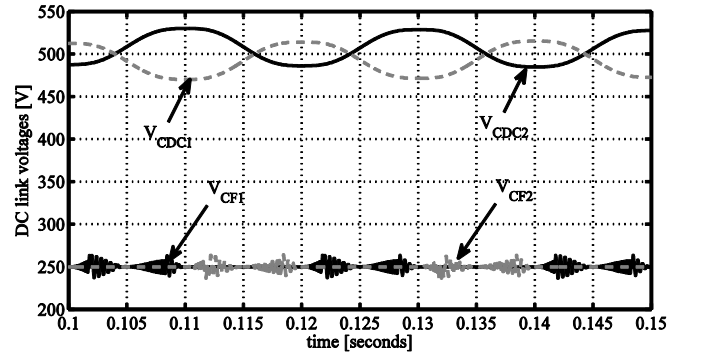

Fig. 6. Main and floating DC link voltages of the converter at 12kW output power.

To validate the theory and simulation results, single phase prototype with 12 kW continuous output power has been build, and shown in Fig. 9. It can be seen from the figure that the experimental converters has RC snubbers and balancing resistors to achieve dynamic and static voltage sharing between series connected devices. The prototype parameters are presented in Table II. In order to achieve results using experimental rig, the main DC link voltage was supplied with a constant DC voltage source and the main DC link voltage was set to 1kV. The modulation index was set to 0.8 and the

converter was operated with an RL load to achieve continuous output current. A 1200V SiC MOSFET (C2M0040120D) with 40mΩ on-state resistance has been selected for the prototype[14]. It should be noted that the blocking voltage rating of the selected devices is much higher than required rating due to lack of available 650V SiC MOSFETs at required current rating. Ideally, devices at 400V or 600V blocking class can be used to operate the converter with 1kV DC link voltage as each device will be subject to 250V blocking voltage with 150V or 350V safety margin.
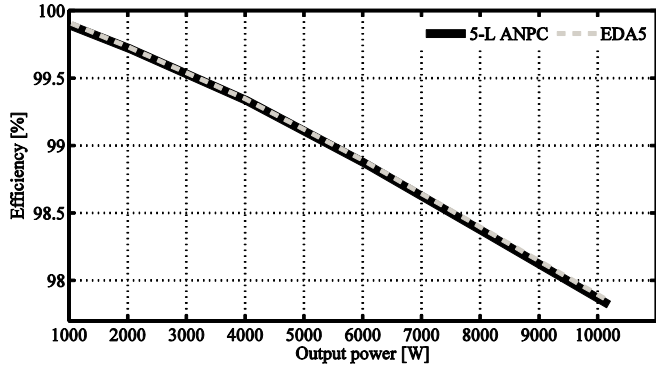

Fig. 7. Efficiency comparison of EDA5 in contrast with 5-L ANPC converter with a fixed modulation of 0.8.
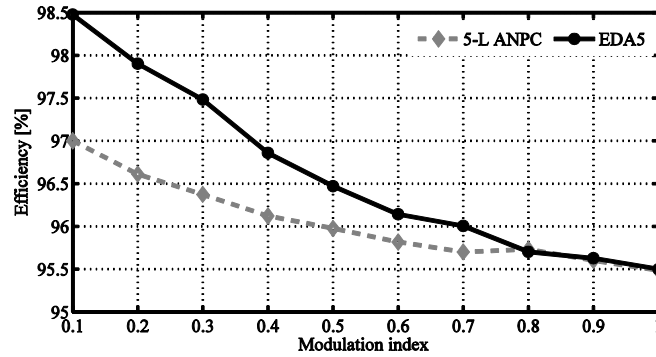

Fig. 8. Efficiency comparison of EDA5 in contrast with 5-L ANPC converter with varying modulation index.
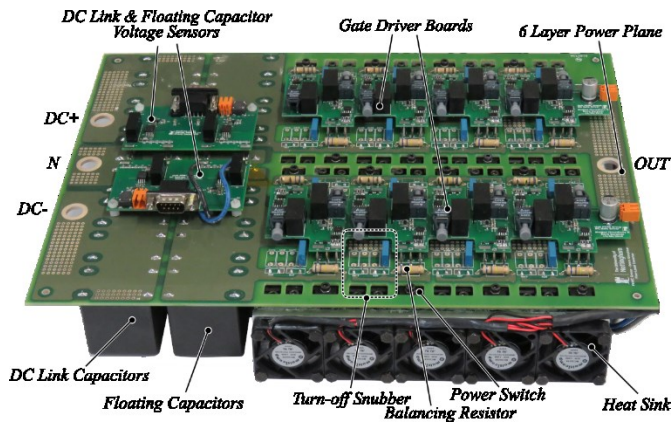

Fig. 9. Single phase 12kW prototype.

The output voltage and the load current is shown in Fig. 11, where the converter was operating at 2.5kW. The main and floating DC link voltages are shown in Fig. 12. It is evident from the figures that the converter topology can control the floating capacitor voltages and can achieve multilevel output voltage waveform successfully. The loss curve of the experimental prototype under different load conditions is presented in Fig. 10, with two operating conditions where the converter was supplied with 800V and 1kV DC link voltages respectively. It can be seen from the efficiency results that the converter is less efficient with lower DC link voltage.
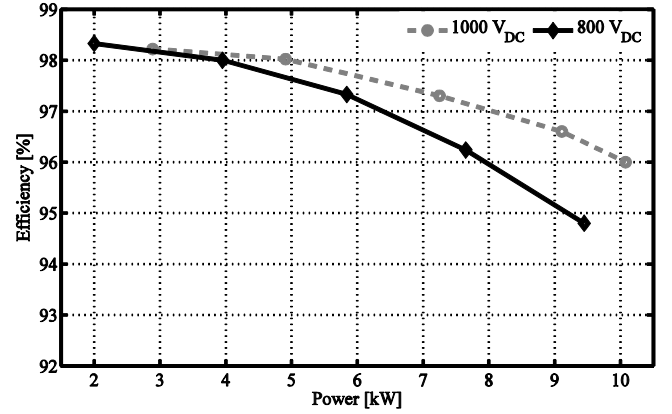

Fig. 10. Efficiency of the experimental prototype.

TABLE I.   SWITCHING STATES

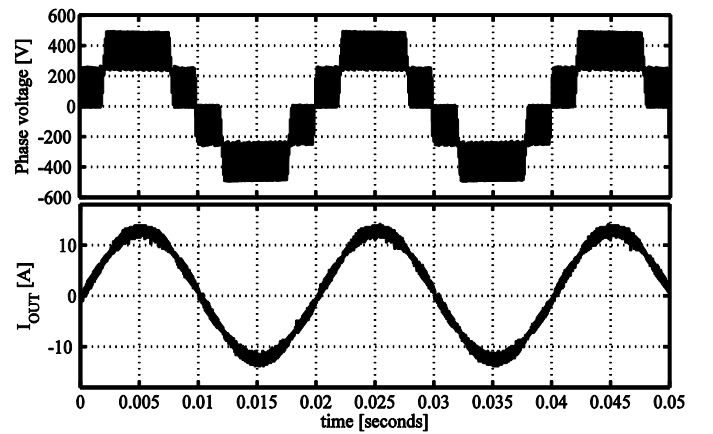| State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
+2E	1	0	0	0	1	0	0	0	0	0
$+E_C$	1	0	1	0	0	0	0	0	1	0
$+E_D$	0	0	0	0	1	0	1	0	0	0
0_P	0	0	1	0	0	0	1	0	1	0
0_N	0	0	0	1	0	0	0	1	0	1
0_X	0	0	1	1	0	0	1	1	1	1
$-E_D$	0	0	0	0	0	1	0	1	0	0
$-E_C$	0	1	0	1	0	0	0	0	0	1
-2E	0	1	0	0	0	1	0	0	0	0

Fig. 11. Output voltage and current of the experimental converter at 2.5kW output power.
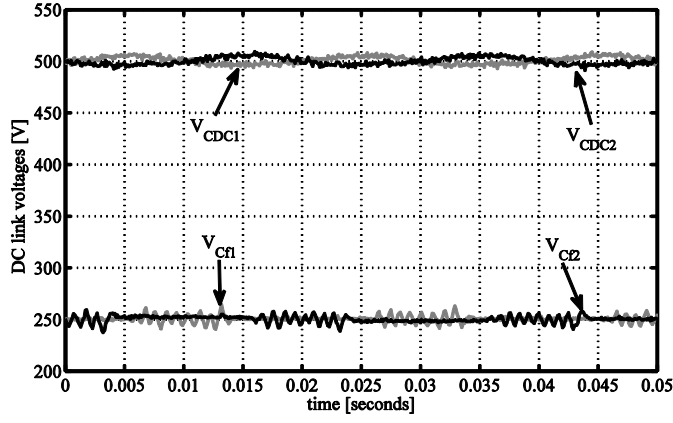
Fig. 12. Main and floating DC link voltages of the experimental converter at 2.5kW output power.
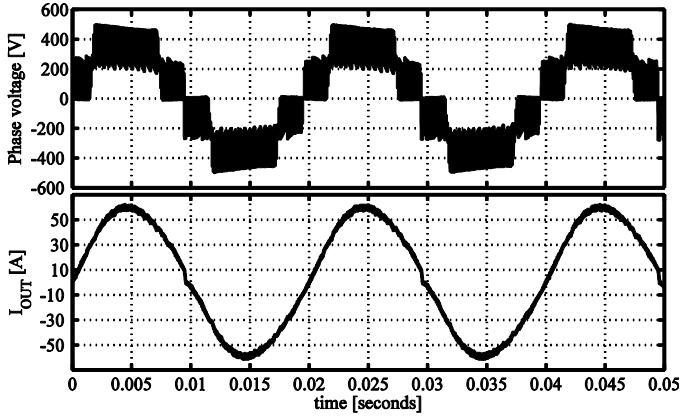

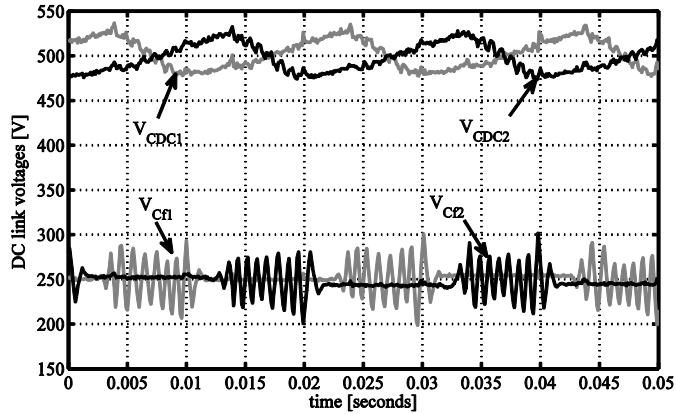Fig. 13. Output voltage and current of the experimental converter at 12kW output power.

Fig. 14. Main and floating DC link voltages of the experimental converter at 12kW output power.

The lower efficiency with lower DC link voltage suggest that the converter losses are governed by the increased conduction losses of the devices for varying output power rating. Output voltage and current of the converter along with the DC link voltages are shown in Fig. 13 and in Fig. 14 respectively at 12kW output power. From Fig .14, It can be seen that at higher load, the floating DC link voltage fluctuations increase due to higher load demand. The SiC based

EDA5 converter shown in this paper has much higher efficiency than the Si IGBT based converter shown in [15]. In the paper the maximum efficiency of 96% was attained using Si IGBTs in contrast with 97.5% with SiC MOSFETs at 6kW output power. It is evident from the experimental results that the SiC based EDA5 converter can achieve much higher efficiency than Si IGBT based converter due to superior properties of SiC MOSFETs.

TABLE II.   EXPERIMENTAL PARAMETERS

Parameter	Symbol	Value
DC link voltage	V_{DC}	$1kV$
Output power	P_{OUT}	$10kW$
Switching frequency	f_{sw}	$10kHz$
Interlocking dead time	t_{DT}	$500ns$
Floating DC link capacitance	C_{f1-f2}	$200\mu F$
Switching device	S_{1-10}	$1.2kV, 40A\ MOSFETs$
Device on state resistance	R_{DS_ON}	$40m\Omega\ (25^o\ C)$ $62m\Omega\ (100^o\ C)$
Load inductance	L_f	$1.5mH$

V.   CONCLUSION

In this paper, a novel five-level hybrid inverter topology has been presented. The proposed topology is compared with state-of-the-art hybrid multilevel topologies in simulation. Simulation results show that EDA5 converter is able to control the floating capacitor and can achieve five level output voltage waveform. Moreover, the proposed converter shows higher efficiency in comparison to 5L-ANPC, especially at lighter load conditions under same operating conditions. A 12kW prototype has been built using SiC devices for experimental validation. The experimental results suggests that the converter can control floating capacitor voltage and also achieves multilevel output voltage waveform with high efficiency.

VI.   REFERENCES

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