A Novel Multi-Modular Series HVDC Tap

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Abstract

Tapping energy from a HVDC transmission line to serve small remote communities has been considered by researchers and HVDC manufacturers since the 1960s. Many HVDC taps proposed consider the performance of diodes, Thyristors and GTOs and the utilization of bulky and expensive high voltage transformers. This paper proposes a novel HVDC tap topology, the n-phase multi-modular series tap (MMST), which utilises capacitors to decouple HV voltage and IGBT H-bridge sub-modules typically found in modular multilevel converters to transfer HVDC to MVAC. The number of phases and operating frequency can be picked according to the requirement of the application. The feasibility of n-phase MMST has been verified by the results from simulation carried out in PLECS software.

1 Introduction

Small remote communities benefit from an external electricity connection to ensure their energy demands can be reliably met. Unfortunately, in some of these cases the use of a dedicated AC transmission may be uneconomical and unaffordable. Under such circumstances being able to connect directly to a nearby bulk power HVDC transmission network would be desirable [1]. For this reason an inexpensive and efficient HVDC-MVAC conversion method is required- this type of connection is referred to here as a HVDC Tap. The main requirements of HVDC tap are [2, 10]:

1. Sufficiently small power rating compared with the main HVDC system, typically 1%~10% [3].
2. Negligible impact on the reliability of the main HVDC system, i.e. the fault on the HVDC tap cannot shut the whole HVDC system down.
3. Individual control system of HVDC tap which doesn't interface with the main HVDC system control.
4. Reduced fixed cost and limited volume.

The proposed HVDC taps in literature can be separated into two categories: series and parallel taps [3]. A series tap inserts a DC voltage in-line with HVDC transmission line. The interaction with the regular transmission current and this voltage result in power being transferred from the line. A parallel tap utilises the full HVDC voltage such that a relatively small additional current is drawn by the tap. The typical diagrams of series and parallel taps are shown in Fig 1.

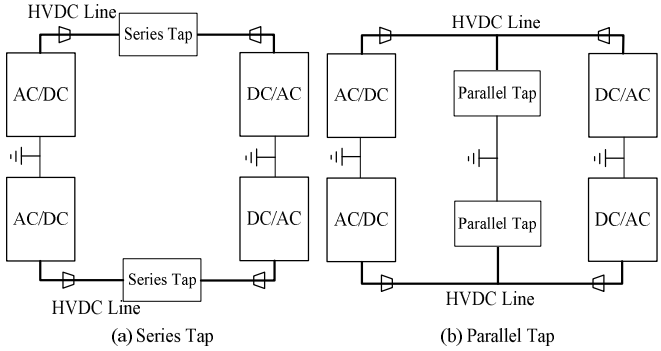


Fig1: Series tap & Parallel tap

Benefiting from flexible design and relatively low cost, the series tap has become popular since 1960s. In early research, only the diodes and Thyristors can be picked in topology design due to the lack of high-power controllable switches such as IGBTs. Different types of tap topologies are proposed in [6-12], but they are all line commutated. The priority of the design is to be able to turn the Thyristors off by connecting transformers and capacitors differently.

A typical series tap proposed in [7] is a DC-AC-DC-AC system. Three converters, 2 transformers and 1 capacitor are needed to transfer energy from the HVDC system to the AC loads. Excessive converters, complex control and uneconomic cost of this tap cannot be avoided due to the large number of switching devices and the HV rated transformer.

A similar series tap topology to [7] is proposed in [8]. The middle of the HVDC-AC H-bridge inverter includes a capacitor which is designed to resonate with the air-core transformer. The Thyristors can be forced to turn off by the capacitor voltage with proper LC design, achieving a higher operating frequency and more controllable power transmission. [9] considers a soft-switching tap topology with LC resonance which can reduce the switching losses. However they both have the disadvantages of complicated control and parameter design.

Most of the proposed HVDC taps are series taps due to some drawbacks associated with parallel taps including [10]:

1. Parallel tap operates under the full HVDC voltages and high voltage step-down ratios. It leads to excessive use of devices, and a relatively low operating current which is challenging for reasonable use of device ratings.
2. A tap DC fault may affect the main HVDC system.
3. If Thyristors are used, the power flow direction cannot be reversed. And a commutation failure on the tap results in excessive currents being drawn from the other HVDC converters.

One parallel HVDC tap scheme, the unidirectional DC transformer, is presented in [11]. The DC transformer is a topology that can achieve high step-up ratio within MW level power transfers. The converter is composed of two resonant circuits which share a common AC capacitor. The LC resonance in the source side circuit creates a high AC voltage on the common capacitor. With the proper operation of the load side circuit, the DC transformer can achieve high step-up ratio. The bidirectional DC transformer is presented in [12].

[13] proposes four DC/DC converters adopting a modular multilevel structure for a parallel tap, including both a direct connection and a transformer-coupled connection. The topologies with direct connection are not suitable for interfacing small amounts of power to HVDC system, while the transformer-interfaced topologies are more power flexible due to variable transformer ratio.

Since series taps are not rated for the full HVDC line voltage they offer advantages in control, cost and volume compared with parallel taps. This paper proposes a novel series HVDC tap referred to here as, an *N-phase Modular Multilevel Series Tap* (MMST), as shown in Fig 2. As there is no requirement for a HV rated transformer, it is anticipated that the installation cost would be reduced. In addition, the structure utilises sub-modules found in MMC HVDC converters such that additional development and production costs are reduced.

2 MMST topology

The modular multilevel series tap is a type of bidirectional series HVDC tap that utilises the full bridge sub-modules which can be typically found in modular multilevel converters for HVDC power transmission. It is a poly-phase converter which requires a minimum of two phases. The phase connection of MMST on HVDC transmission line is demonstrated in Fig 2.

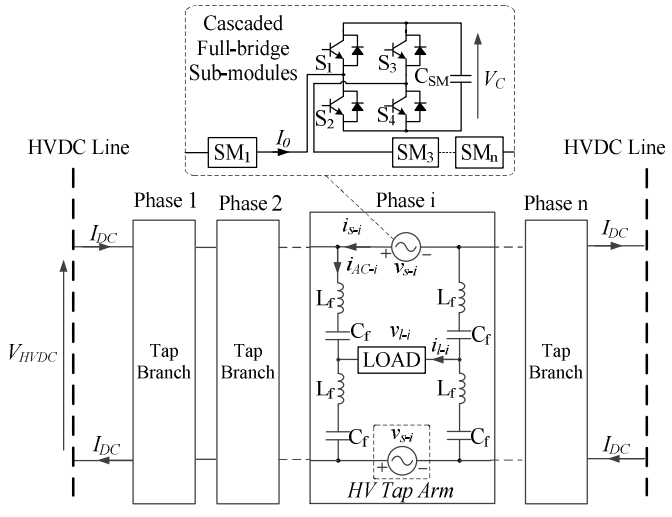


Fig 2: Topology of N-phase MMST

In each phase AC current is actively circulated around the tap and load, and power is transferred between the HVDC transmission line and MV load sides by the insertion of AC voltage in the tap and load branch. To ensure that there is no net energy exchange from the HV side tap arms, a DC bias voltage is added into sub-module string to recharge the sub-module capacitors from the DC line current. The branch impedance is used to block the HV voltage between the HVDC line and ground (load), while filtering the AC current at the same time. In this manner it is possible to capacitively couple the connection to the MV connection removing the need for a HV rated isolation transformer. The insertion of a resonant inductor in series with the blocking capacitor reduces the voltage drop across the impedance for a given AC current and capacitor size, thus a smaller blocking capacitor can be utilised.

It is proposed that the n-phase MMST, shown in Fig 2, is operated such that symmetrical sinusoidal voltages with DC offset are produced at the HV tap arms, as described by Equation (1). The use of symmetrical AC voltage components with no AC zero sequence component means that the AC voltage sums to zero and is not seen by the the HVDC bus. Although a small DC voltage ripple caused by the modulation difference of each HV tap arm always exists, it can be filtered by the HVDC cable. The total tap DC voltage seen by the transmission line is given by Equation (2) and must be overcome by the difference in converter station voltages.

$$v_{s-i} = V_{DC} + \hat{V}_{AC-i} \cdot \sin\left(\omega t + \frac{2\pi}{n_{ph}} \cdot i\right) \quad i = 1,2,3... \quad (1)$$

$$v_{DC-total} = 2n_{ph}V_{DC} \quad (2)$$

By control of the AC component of the tap voltage, v_{AC}, with respect to the AC load voltage v_l, current can be circulated between the tap branches and the load branch, such that the tap current is given by Equation (3). As can be seen the tap current also includes the DC current that flows in the transmission line. The load current, i_l contains twice the AC tap current as in Equation (4).

$$i_{s-i} = I_{DC} + \hat{I}_{AC-i} \cdot \sin\left(\omega t + \frac{2\pi}{n_{ph}} \cdot i + \theta\right) \quad i = 1,2,3... \quad (3)$$

$$i_{l-i} = 2\hat{I}_{AC-i} \cdot \sin\left(\omega t + \frac{2\pi}{n_{ph}} \cdot i + \theta\right) \quad i = 1,2,3... \quad (4)$$

The instantaneous power of single tap arm, p_s, is given by Equation (5). In order to ensure there is no net energy exchange in the tap arm the DC component voltage is selected such that there is zero net power in the HV tap arm, as in Equation (6).

$$\begin{aligned} p_{s-i} = {} & V_{DC} \cdot I_{DC} + \frac{\hat{V}_{AC-i} \cdot \hat{I}_{AC-i} \cdot \cos\theta}{2} \\ & + V_{DC} \cdot \hat{I}_{AC-i} \cdot \sin\left(\omega t + \frac{2\pi}{n_{ph}} \cdot i + \theta\right) \\ & + I_{DC} \cdot \hat{V}_{AC-i} \cdot \sin\left(\omega t + \frac{2\pi}{n_{ph}} \cdot i\right) \\ & - \hat{V}_{AC-i} \cdot \hat{I}_{AC-i} \cdot \cos\left(2\omega t + \frac{4\pi}{n_{ph}} \cdot i + \theta\right) \quad i = 1,2,3... \end{aligned} \quad (5)$$

$$V_{DC} = -\frac{\hat{V}_{AC-i} \cdot \hat{I}_{AC-i} \cdot \cos\theta}{2I_{DC}} \quad (6)$$

The total DC power exchanged between the HVDC transmission line and the MMST is therefore given by Equation (7). The AC power exchanged between the MMST and the load is given by Equation (8)

$$P_{DC} = 2n_{ph} \cdot V_{DC} \cdot I_{DC} \quad (7)$$

$$P_{AC} = n_{ph} \cdot \hat{V}_{AC} \cdot \hat{I}_{AC} \cdot \cos\theta \quad (8)$$

In the operation of MMST the choice of DC voltage and current are respectively fixed by the power demand of the tap and the instantaneous current in the HVDC line. However if it is assumed that the load as it appears to the tap is perfectly decoupled from the MV network by means of an additional MV power converter, then the AC voltage, current and frequency are flexible and degrees of freedom for the system designer.

In this work only a three-phase MMST is considered. The load is designed as an MVAC-AC converter with an isolated transformer, which can be regarded as a controlled voltage source with fixed frequency and phase angle in initial analysis.

3 Control method

As the load is regarded as a voltage source the power transmission from HVDC line to the load is controlled by AC phase current. It is more suitable to implement the DQ transformation to control three-phase AC currents, but the mean capacitor voltage control of each HV tap arm is challenging. Therefore a regulator that can control single-phase load current should be selected.

For regulating a single-phase AC current the proportional-integral (PI) regulator is not the first option because the bandwidth of PI regulator cannot guarantee the gain at AC frequency high enough, i.e. the steady-state error cannot be eliminated. Instead the use of a Proportional Resonant (PR) regulator is considered for the three phase MMST. The mean capacitor voltage regulator and load power regulator are not considered in detail.

3.1 PR regulator

The PR regulator is widely applied in single-phase AC control systems. It is utilised for harmonic detection and elimination as well. The PR regulator is capable of following the AC reference at the certain frequency, eliminating the steady-state error and maintaining good transient response [14].

A major objective for stationary PR regulator is to achieve zero magnitude and phase errors. Therefore, based on a conventional integrator $G_{DC}(\mathrm{s}) = k_p + \frac{k_i}{s}$, the equivalent AC controller would have an open loop transfer function of [15]:

$$G_{AC}(\mathrm{s}) = k_p + \frac{2k_r s}{s^2 + \omega_0^2} \quad (9)$$

In the initial system design, the PR regulator given in Equation (9) is adopted.

3.2 Dynamic model of current control

Each phase in the system is longitudinally symmetrical, so the dynamic model can be simplified to one loop, as shown in Fig 3.

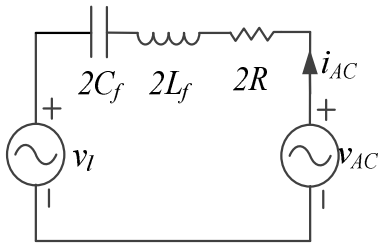


Fig 3: Simplified model of two-phase MMST

The source and load voltages can be expressed as [16]:

$$v_l(t) = \hat{V}_l \cos(\omega_0 t + \theta_0) \quad (10)$$

where $\hat{V}_l$ is the peak value, ω_0 is the frequency, and θ_0 is the initial phase of load voltage.

The dynamic model can be given by

$$v_{AC} = 2R \cdot i_{AC} + 2L_f \frac{di_{AC}}{dt} + \int \frac{1}{2C_f} i_{AC} dt + \hat{V}_l \cos(\omega_0 t + \theta_0) \quad (11)$$

which describes a second-order linear system that is excited by a fixed AC output $v_l(t)$. Thus, if v_{AC} is an AC variable with the same frequency, ω_0, i_{AC} is also an AC variable with the same frequency and a certain phase shift.

Based on these equations, the function for the steady-state operating condition is:

$$2L_f \frac{di_{AC}}{dt} + \int \frac{1}{2C_f} i_{AC} dt = -2R \cdot i_{AC} + V_{AC} - V_l \quad (12)$$

In Equation (12), i_{AC} is the state variable, V_{AC} is the control input, and V_l is the disturbance input. V_{AC} is generated from the sub-modules in the tap arm, which can output from $-V_{SM}$ to V_{SM}. Then V_s can be expressed as:

$$V_{AC} = V_{SM} \cdot m(t) \quad (13)$$

where the modulation ratio $m(t)$ is determined by:

$$m = \frac{1}{V_{SM}}(u + V_l) \quad (14)$$

where u is defined as a new control input, which can be deduced as:

$$u = 2L_f \frac{di_{AC}}{dt} + \int \frac{1}{2C_f} i_{AC} dt + 2R \cdot i_{AC} \quad (15)$$

Equation (15) describes a Type 0, second-order, linear system. i_{AC} can be controlled by varying u.

3.3 PR control loop design

According to Equation (13) & (14) V_s is given by

$$V_{AC} = u + V_l \tag{16}$$

which actually expresses the AC component of source voltage V_s. Based on the topology principle described in Section 2, a DC bias voltage is required on V_s to inject energy into tap arms and keep no net energy change in sub-module capacitors, given by Equation (6). Due to reverse DC current directions in upper and lower arms, the DC bias voltage applied on them are equal but opposite, given by:

$$V_s = u + V_l \pm V_{DC} \tag{17}$$

The diagram of AC current control loop of a single phase of an MMST is shown in Fig 4.

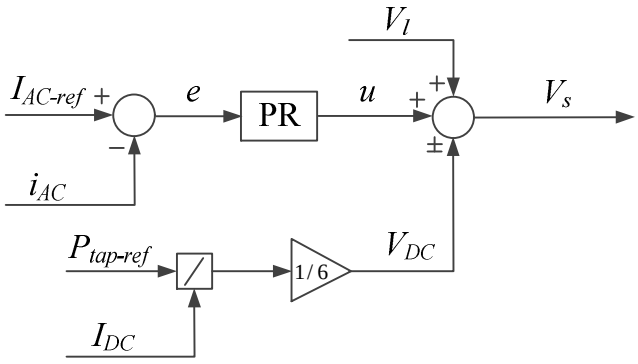


Fig 4: Diagram of PR current regulator

3.4 Capacitor voltage balancing for HV tap arm

As for all the converters utilising modular multilevel structures, the energy in the sub-module capacitors has to be maintained throughout the operation. Since the tap arm voltage and current may both have the positive and negative period in real application, the charging and discharging time is determined by the real-time power flow direction, calculated from arm voltage multiplied by arm current. When the power is injected into the tap arm, the sub-module with the lowest capacitor voltage is turned on to charge. On the contrary, when the power flows out of the tap arm, the sub-module with the highest capacitor voltage is turned on to discharge [17]. The sub-module switches on or off only when the modulation index changes in order to reduce the switching losses.

The control loop of the capacitor voltage balancing is applied as well to cooperate with the sub-module modulation and balancing. A PI regulator is utilised to maintain the mean capacitor voltage of one tap arm as constant and calibrate the reference of phase AC current.

4 Simulation Results

Based on the presented analysis, a case study has been performed based on the South-West Link in Sweden presently under construction. The steady-state simulation of three-phase MMST has been developed to verify its feasibility in the PLECS software. The diagram of MMST topology in simulation is shown in Fig 5.

The parameters for the case study are listed in Table 1. A 20MW three-phase MMST is designed with 11kV line-to-line voltage.The operating frequency is initially set at 300Hz in order to reduce the value of branch inductor which resonates with the branch capacitor. The switching frequency of each sub-module is chosen as 1kHz such that the switching frequency of one tap arm is 7kHz.

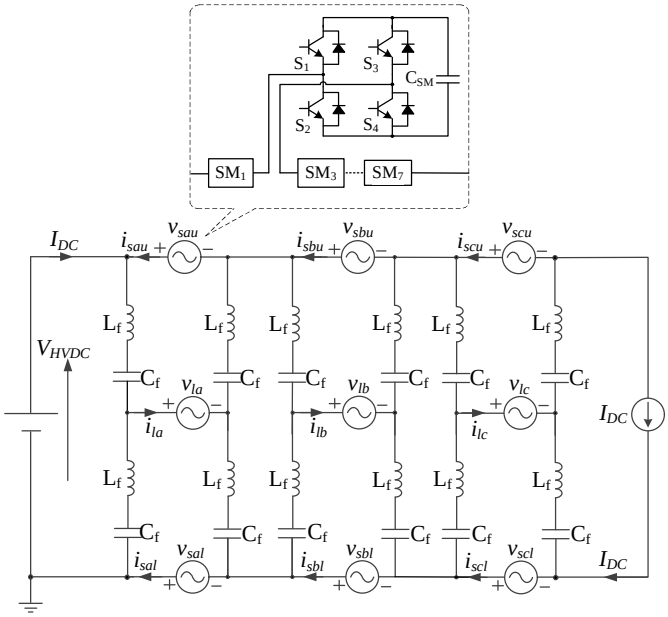


Fig 5: Circuit diagram in simulation

Parameter	Value
HVDC Voltage	±300kV
HVDC Current	1000A
Tap Power	20MW
Load Voltage	11kV (l-l)
Numbers of Sub-modules	42 (7 each)
Modulation Level	2000(V)
Mean Capacitor Voltage	2000V
Fundamental Frequency	300Hz
Switching Frequency	7kHz

Table 1: Key parameters in PLECS simulation

Fig 6 shows the waveforms of the three-phase load voltages and currents. The load is replaced with an AC voltage source, so that the load voltage, shown in Fig 6.(a), is sinusoidal. The load current, shown in Fig 6.(b) is filtered by LC blocking branch, with the THD as less than 0.1%.

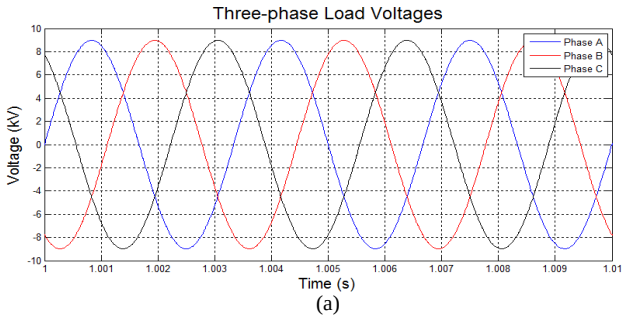
Fig 7 shows the currents that flow through upper and lower tap arms. It is clear that all the currents consist of DC component (HVDC current) and AC component. The upper and lower tap arms in each phase generate the same AC current to the load, so the AC components are identical. The THDs of AC components are approximately 1%.

Fig 8 shows the output voltages of upper and lower tap arms. It can be seen that there is a DC bias in the AC step wave. In

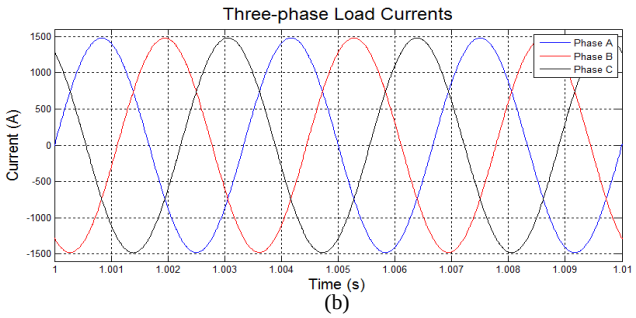
addition, the DC bias in Fig 8.(a) is negative, and positive in Fig 8.(b).

Fig 9 shows the mean voltages of all sub-module capacitors in phase A, B, C, respectively. It can be found that the capacitor voltages are balanced and follow the reference. The total power flowing into the loads is 20MW, shown in Fig 10.

Fig 11 shows the power losses of all the switches in the three-phase MMST, which are calculated based on the MITSUBISHI CM1200HG-66H HVIGBT modules in PLECS software. The conduction and switching losses are 257kW, 100kW, respectively. The efficiency of the three-phase MMST is 98.2%.

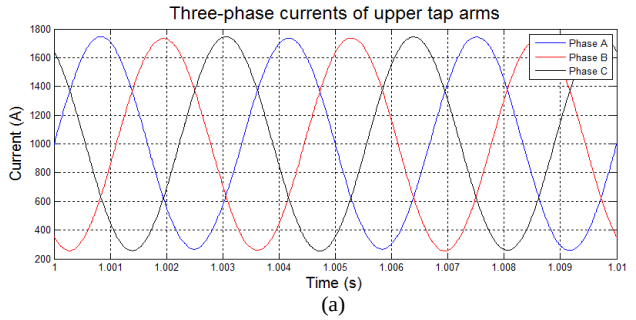


(a)

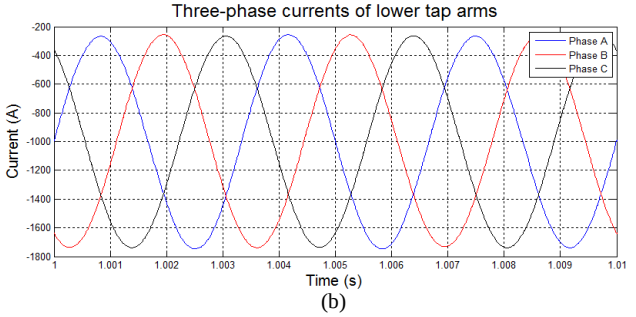


(b)

Fig 6: Three-phase load voltages and currents. (a) v_{la} , v_{lb} , v_{lc} (b) i_{la} , i_{lb} , i_{lc}

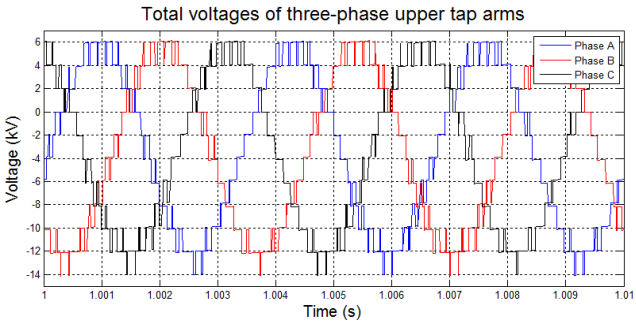


(a)

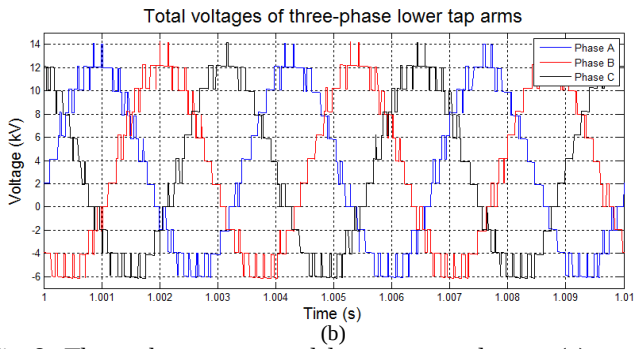


(b)

Fig 7: Real-time three-phase arm currents. (a) i_{sau} , i_{sbu} , i_{scu} (b) i_{sal} , i_{sbl} , i_{scl}



(a)



(b)

Fig 8: Three-phase upper and lower arm voltages. (a) v_{sau} , v_{sbu} , v_{scu} (b) v_{sal} , v_{sbl} , v_{scl}

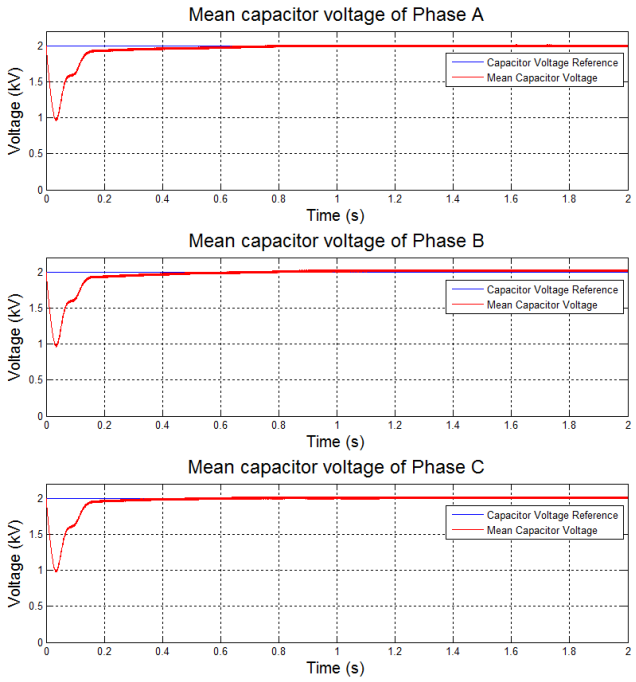


Fig 9: Mean sub-module capacitor voltages of the tap arms

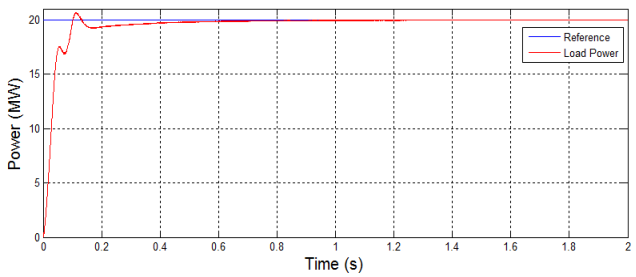


Fig 10: Total load power

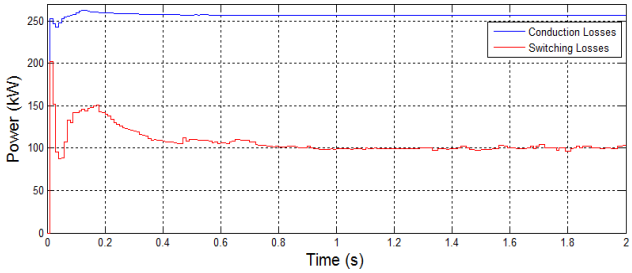


Fig 11: Conduction and switching losses

5 Conclusion

A novel n-phase modular multilevel series HVDC tap method has been proposed. Full-bridge sub-module arms are connected in series with HVDC line to exchange power between the HVDC line and MVAC load. A resonant LC branch is connected between HV and MV sides to decouple the HVDC voltage, and filter harmonics. The detailed analysis of the topology design and operating method are provided. The design of the control method, especially the current control loop is demonstrated. The feasibility of n-phase MMST and performance of control loops have also been verified based on a 20MW, three-phase model by simulation in PLECS software. The waveforms indicating three-phase MMST's steady-state operating conditions verifies the feasibility of the n-phase MMST.

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