Influence of gate bias on the avalanche ruggedness of SiC power MOSFETs

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***Abstract*—This paper investigates the effect of negative gate bias voltage (V_{GS}) on the avalanche breakdown robustness of commercial state-of-the-art silicon carbide (SiC) power MOSFETs. The device's ability to withstand energy dissipation during avalanche regime is a connoting figure of merit for all applications requiring load dumping and/or benefiting from snubber-less converter design. The superior material properties of SiC material means that SiC MOSFETs even at 1200V exhibit significant intrinsic avalanche robustness.**

Keywords—avalanche ruggeddness; silicon carbide; unclamped inductive swithching; power MOSFET; robustness

I. INTRODUCTION

A device's ability to withstand energy dissipation in avalanche breakdown regime (E_{AV}) is a connoting figure of merit for all applications requiring load dumping and/or benefiting from snubber-less converter design even in the presence of non-zero parasitic inductance values [1]. The avalanche ruggedness is typically achieved in silicon (Si) MOSFETs and IGBTs as a result of progressive device design and engineering optimisation by delaying parasitic BJT activation [2]. On the other hand, the specific material properties of silicon carbide (SiC) (e.g., the higher energy band gap) means that SiC MOSFETs even at 1200 V exhibit significant built-in robustness, which deserves dedicated study. However, the higher band gap in SiC makes is highly unlikely for the activation of parasitic npn BJT. Various studies have already shown that SiC power MOSFETs can dissipate E_{AV} up to approximately 1J depending on test conditions [3-5]. This paper aims to investigate the dependence of avalanche ruggedness of SiC power MOSFETs on gate bias voltage (V_{GS}). Experimental results at different V_{GS} along with simulation results are included in this paper.

II. EXPERIMENTAL RESULTS

Avalanche ruggedness is characterized experimentally by way of unclamped inductive switching (UIS) tests [4, 6]. The schematic of a UIS test setup is shown in Fig. 1. An auxiliary IGBT with a 3kV breakdown voltage was used in parallel to ramp up the inductor current (I_L) to the required value, avoiding the self-heating prior to avalanche phase. A schematic presentation of the inductor current (I_L) and drain voltage (V_{DS}) waveforms for a safe UIS transient are also presented in Fig. 2. The experimental results presented here are on 1.2kV 36A rated SiC power MOSFET (C2M0080120D) in a TO-247 package from CREE [7]. Different tests were carried out on device under test (DUT), referring to circuit in Fig. 1, in the first case V_{GS} = 0V was used, and in second case V_{GS} = -5V while keeping all the other test conditions unaltered. The aim of this analysis was to observe the effect of different V_{GS} on the avalanche capability of SiC power MOSFETs. All the tests presented here were carried out at input voltage (V_{DD}) = 400V, load inductor (L_{LOAD}) = 500µH and case temperature (T_{CASE}) = 25°C while changing V_{GS}.

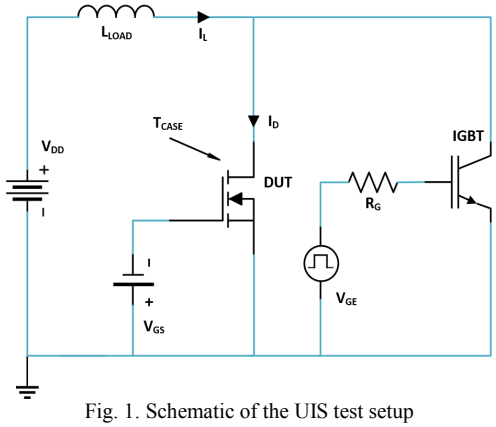

Fig. 1. Schematic of the UIS test setup

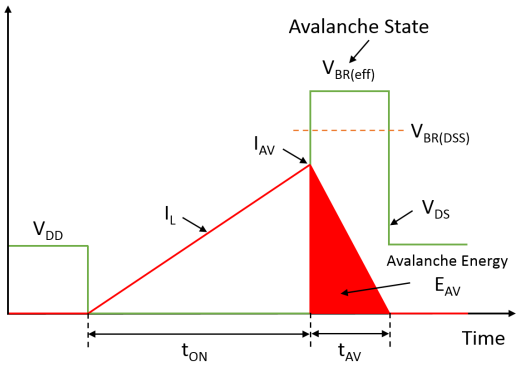

Fig. 2. Representative I_L and V_{DS} waveforms for safe UIS test

Starting with V_{GS} = 0V, Fig. 3 shows typical I_L and V_{DS} waveforms (I_{AV} ~ 43A) for a safe UIS event. A safe UIS test is characterized by the return of I_L and V_{DS} to zero and input voltage (V_{DD}) respectively. The on time (t_{ON}) of the IGBT was gradually increased to increase the peak avalanche current (I_{AV} ~ 47A) until failure was observed. Moreover, under the same test conditions, the gate bias was changed to V_{GS} = -5V. In this case, even though I_{AV} is the same, the device safely completes the avalanche phase and returns to blocking afterwards. A low output impedance power supply was used to supply V_{GS}. For comparison, Fig. 4 plots V_{DS} and I_L for both V_{GS} = 0V and -5V for the same I_{AV}. Here, it can be seen that the DUT failed for I_{AV} ~ 47A for V_{GS} = 0V. On the other hand, the DUT tested for V_{GS} = -5V sustained the avalanche breakdown regime and did not fail. Fig. 5 presents the I_L and V_{DS} waveforms (I_{AV} ~ 50A) at failure for V_{GS} = -5V. For DUT tested at V_{GS} = -5V, higher I_{AV} i.e. higher E_{AV} was needed before failure was observed. The failure is characterized by the collapse in V_{DS} and hence, the DUT losses its ability to block voltage. At failure, I_L starts to increase again (as dictated by V_{DD} and L_{LOAD}) since the device experiences an internal short between all the DUT terminals followed by a catastrophic failure of the device. Several papers have demonstrated characterization of SiC power MOSFETs during avalanche breakdown also showing failure [3-6, 8, 9].

The avalanche energy (E_{AV}) can be defined using equation 1. E_{AV} was calculated for all test conditions and included in the table presented here (bold text for failure E_{AV}). Finally, all the test conditions for the results presented here are also summarized in Table I.

$$E_{AV} = \frac{1}{2} I_0 V_{BR(eff)} t_{AV} \quad (1)$$

Table I. Summary of Experimental result

V_{DD} (V)	L_{LOAD} (µH)	V_{GS} (V)	I_{AV} (A)	E_{AV} (J)
400	500	0	43	0.75
			47	**0.84**
		-5	47	0.88
			50	**0.96**

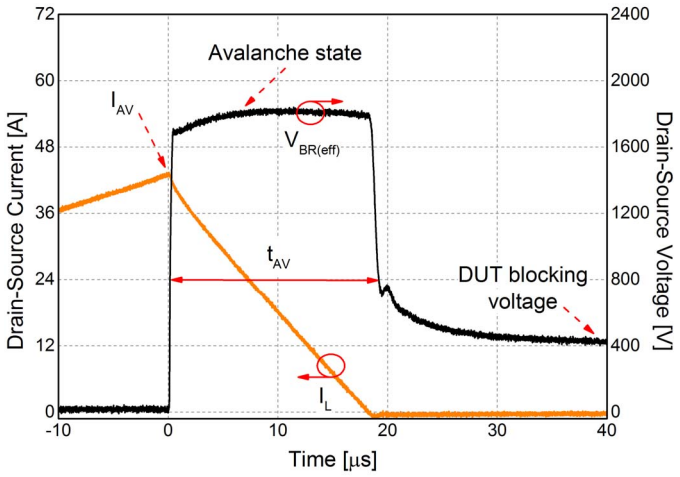

Fig. 3. Experimental I_L and V_{DS} waveforms for safe UIS test; V_{GS} = 0V

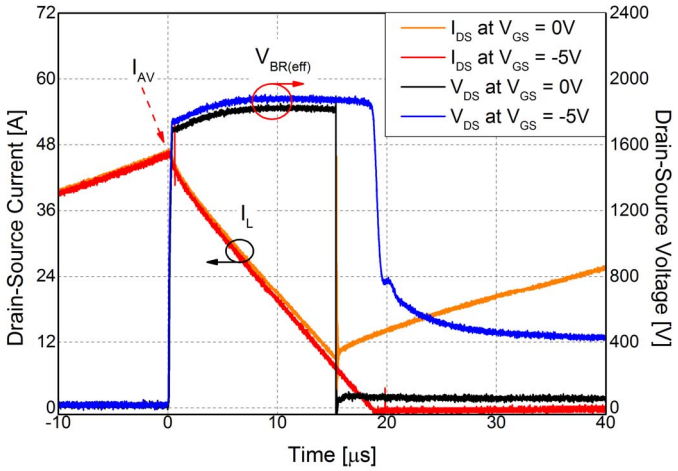

Fig. 4. Experimental I_L and V_{DS} waveforms for safe and failure UIS test for V_{GS} = 0V and V_{GS} = -5V respectively; Comparison

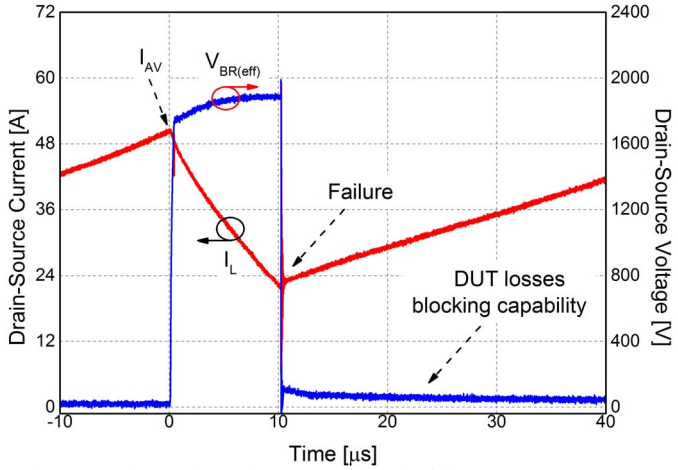

Fig. 5. Experimental I_L and V_{DS} waveforms for failure UIS test; V_{GS} = -5V

III. TCAD Simulation Results

TCAD electro-thermal simulation results reporting the failure mechanism of SiC power MOSFETs during avalanche breakdown operation complement the study of the device behaviour under different gate source bias voltages (V_{GS}). This work advances a previous study on the UIS failure mechanism of SiC power MOSFETs [8], providing new important insight into the dependence of avalanche robustness on gate bias voltage. Electro-thermal mixed-mode 2D simulations were used to reconstruct the observed failure and interpret the experimental results. Fig. 6 shows the simulated planar cell structure with important dimension parameters and doping concentrations.

In these simulations, two physically separated electrodes were used for the P-body and N+ implant regions of the cell structure but connected to the same electrical node. The simulations were carried out at V_{DD} = 400V and L_{LOAD} = 500µH while changing V_{GS}. Fig. 7 present the failure UIS simulation for V_{GS} = 0V. The current components flowing out of both P-body and N+ source contacts are also shown in Fig. 8, together with the overall device current. As can be seen in Fig.8, the electron current starts to flow into the N+ source

region as the time in avalanche (t_{AV}) lapsed until failure occurred.

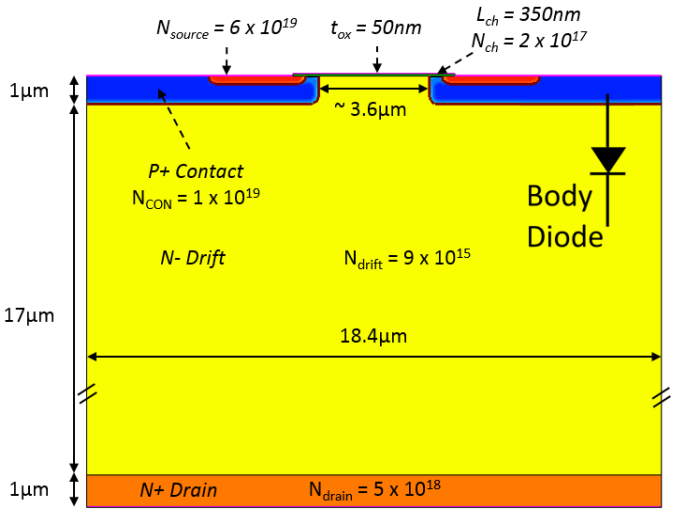

Fig. 6. Simulated planar structure (Not to scale)

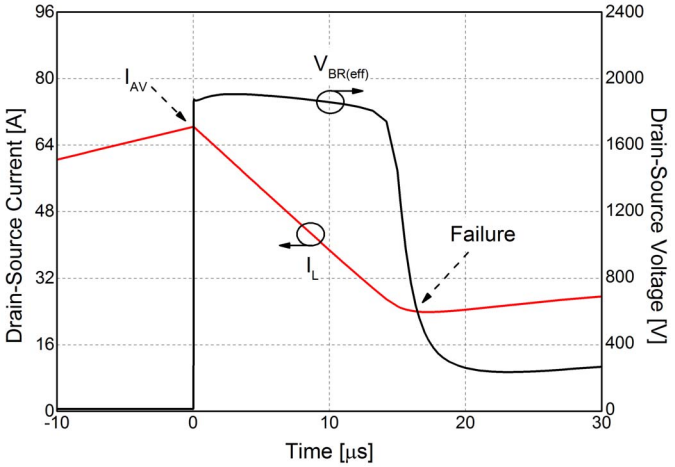

Fig. 7. Simulated I_L and V_{DS} waveforms for failure UIS event; V_{GS} = 0V

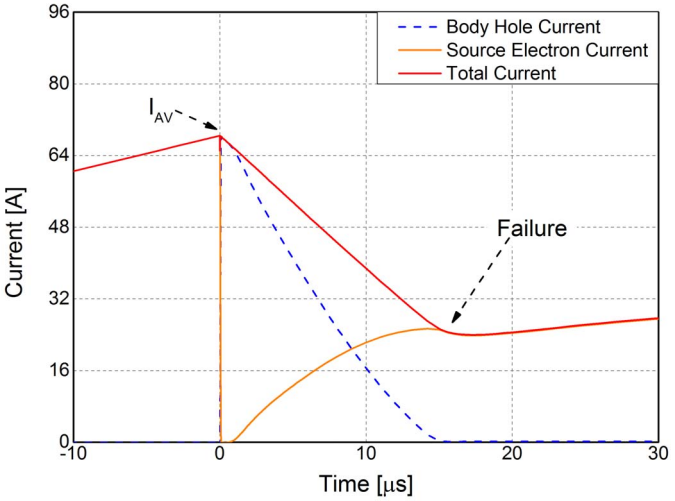

Fig. 8. Source electron and body hole current components for I_L in Fig. 7

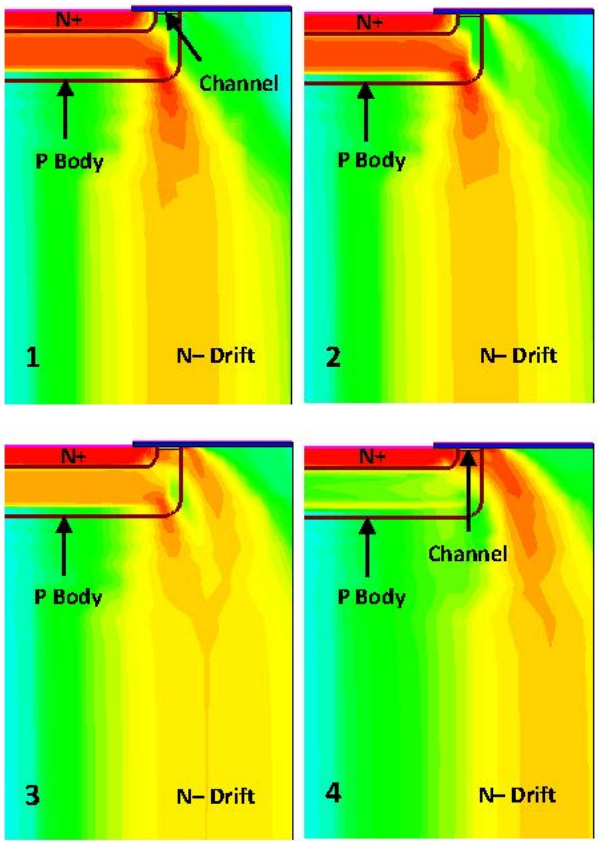

Fig. 9. Total Current Density; Zoomed in near p-body/n-drift region (1-4 with increasing t_{AV})

During avalanche breakdown, the highest electric field occurs at the curvature of the body/drift pn junction and hence, the maximum impact ionization also happens at the same place. While the device is in avalanche, the current density usually flows over the body diode of the MOSFET going through the pn junction curvature as also presented in Fig. 9 (1). The junction temperature (T_J) due to really high power density in such a small device (die size: 3.10 x 3.36 mm) during such short UIS transients could easily rise significantly to really high values well above 1000K. Fig. 9 presents current density at different time instances starting from time instance immediately after entering avalanche breakdown (1) until after failure (4). As a result of such high temperature increase (cell temperature simulated well above 1000K at failure), the current also starts to flow in and below the channel area aided by the reduction of threshold voltage (V_{th}) due to consistent temperature increase near p-body as shown in Figure 9 (2 and 3). After failure, only electron current flows in and below the channel as shown in Figure 9 (4). Mixed-mode simulations results for V_{GS} = -5V are also included in Fig. 10. Here, slightly higher I_{AV} was required before failure was obtained. Simulations have shown that by using a negative V_{GS} to keep the device turned off helps to better close the channel. Therefore, it takes longer (i.e. higher temperature) before the onset of source electron current flowing in and underneath the channel. Hence, channel activation is slightly delayed with negative V_{GS} allowing the device to sustain a slightly higher I_{AV} and E_{AV} before encountering failure.

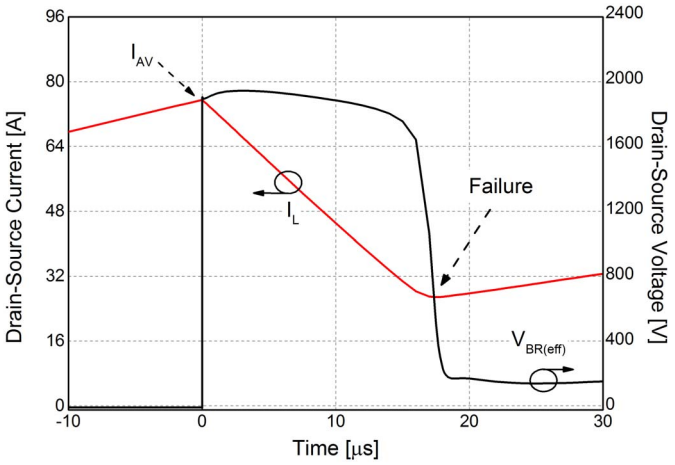

Fig. 10. Simulated I_L and V_{DS} waveforms for failure UIS event; V_{GS} = -5V

Effect of temperature on V_{th} has also been investigated experimentally in [10] which also partially supports the presented interpretation of V_{th} lowering which results in current flow in and underneath channel at failure as the DUT T_J increases.

IV. THERMAL MAPPING

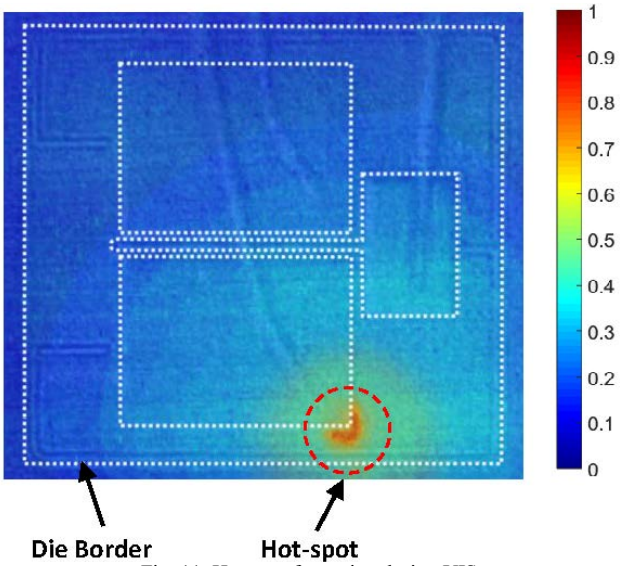

Fig. 11. Hot-spot formation during UIS

The thermal mapping on bare-die devices was also performed using infrared (IR) thermography (explained in [11]). The IR map showed the formation of a localised hot-spot due to current crowding mechanism in a small group of cells close to the source metal contact as can be seen in Fig. 11. The hot-spot formation occurs due to a positive feedback mechanism involving bipolar current flow. The formation of a hotspot usually indicates that bipolar currents flows at failure. It is either possible that the actual device failure occurs at an earlier t_{AV} time instant when the hole current is still flowing which also explains the hot-spot formation since the simulated cell structure is not the true representation of a real device and its associated packaging features. Moreover, the simulations involve just a single cell so the interactions from the surrounding cells is not taken into account thus making it difficult to obtain hot-spot formation with a single cell.

V. CONCLUSION

This paper investigated the influence of gate source bias (V_{GS}) on the avalanche breakdown robustness of SiC power MOSFETs. Experiments showed that negative turn-off V_{GS} = -5V slightly enhances the avalanche withstand capability of the devices. Si power devices can be turned-off with V_{GS} bias up to −15 V whereas SiC is limited in negative bias. The experimental results were also complemented using TCAD simulations which showed progressive shift of current from the body diode towards the channel during avalanche phase. After failure, the current flow was entirely in and underneath the channel. Lastly, thermal mapping on bare die devices are also presented. Unlike in Si, the activation of npn BJT within SiC devices seems highly unlikely due to higher band gap and weak gain of the parasitic bipolar transistor.

REFERENCES

[1] Pala, Vipindas, Edward V. Brunt, Lin Cheng, Michael O'Loughlin, Jim Richmond, Albert Burk, Scott T. Allen, David Grider, John W. Palmour, and Charles J. Scozzie. "10 kV and 15 kV silicon carbide power MOSFETs for next-generation energy conversion and transmission systems." In *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, pp. 449-454. IEEE, 2014.

[2] Fischer, Kevin, and Krishna Shenai. "Dynamics of power MOSFET switching under unclamped inductive loading conditions." *IEEE Transactions on electron devices* 43, no. 6 (1996): 1007-1015.

[3] DiMarino, Christina, and Brett Hull. "Characterization and prediction of the avalanche performance of 1.2 kV SiC MOSFETs." In *Wide Bandgap Power Devices and Applications (WiPDA), 2015 IEEE 3rd Workshop on*, pp. 263-267. IEEE, 2015.

[4] Fayyaz, Asad, Gianpaolo Romano, Alberto Castellazzi, and Andrea Irace. "Robustness investigation of SiC power MOSFETs under negative temperature." In *Power Electronics and Applications (EPE'16 ECCE Europe), 2016 18th European Conference on*, pp. 1-8. IEEE, 2016.

[5] Kelley, Mitchell, Bejoy Pushpakaran, and Stephen Bayne. "Single Pulse Avalanche Mode Robustness of Commercial 1200 V/80 mΩ SiC MOSFETs." *IEEE Transactions on Power Electronics* (2016).

[6] Liu, Siyang, Weifeng Sun, Qinsong Qian, Chunde Gu, Yu Huang, Song Bai, Gang Chen, Runhua Huang, Yonghong Tao, and Ao Liu. "Investigations on degradation and optimization of 1.2 kV 4H-SiC MOSFET under repetitive unclamped inductive switching stress." In *Power Semiconductor Devices & IC's (ISPSD), 2015 IEEE 27th International Symposium on*, pp. 205-208. IEEE, 2015.

[7] *C2M0080120D Datasheet*; Wolfspeed: Durham, NC, USA, 2015.

[8] Fayyaz, Asad, Alberto Castellazzi, Gianpaolo Romano, Michele Riccio, Andrea Irace, Jesus Urresti, and Nick Wright. "UIS failure mechanism of SiC power MOSFETs." In *Wide Bandgap Power Devices and Applications (WiPDA), 2016 IEEE 4th Workshop on*, pp. 118-122. IEEE, 2016.

[9] Fayyaz, Asad, Li Yang, and Alberto Castellazzi. "Transient robustness testing of silicon carbide (SiC) power MOSFETs." In *Power Electronics and Applications (EPE), 2013 15th european conference on*, pp. 1-10. IEEE, 2013.

[10] Unger, Christian, and Martin Pfost. "Energy capability of SiC MOSFETs." In *Power Semiconductor Devices and ICs (ISPSD), 2016 28th International Symposium on*, pp. 275-278. IEEE, 2016.

[11] Romano, G., M. Riccio, G. De Falco, L. Maresca, A. Irace, and G. Breglio. "An ultrafast IR thermography system for transient temperature detection on electronic devices." In *Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), 2014 30th Annual*, pp. 80-84. IEEE, 2014.