Differential Buck Single Phase Grid Connected AC-DC Converter with Active Power Decoupling using a Flipping Capacitor

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***Abstract*—This paper introduces a new single-phase AC-DC converter capable of achieving independent voltage control across a dedicated power decoupling capacitor, by exploiting the same full bridge that controls the grid current in combination with two bidirectional switches, soft commutated at the line frequency (ZVS). A suitable control of the capacitor voltage is used to completely decouple pulsating grid power from the DC-link, enabling the use of smaller film capacitors instead of electrolytic capacitors for power decoupling, improving reliability and increasing power density. This is achieved without additional high switching frequency devices. Furthermore, the interference occurring between rectified grid current and power decoupling capacitor current is exploited in order to reduce the RMS current in the full bridge, thus improving conversion efficiency.**

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I. Introduction

In order to guarantee adequate decoupling of the pulsating component of grid power from the DC-link without using electrolytic capacitors, various topologies have been proposed in literature [1][2][3][4][5][6][7]. A comprehensive review of those and other solutions is found in [8].

Some of those solutions make use of at least one additional high switching frequency half bridge implementing the concept of Ripple Port, connected in parallel with the DC-link and independent from the grid interface section of the converter. This approach is effective but has the drawbacks of additional switching losses and higher part count.

Other solutions, such as the one considered in [6], [7], and [9] achieve power decoupling without any additional active components. However, in this case, the control of the power decoupling capacitors voltages is not completely independent from the grid voltage. As a consequence, the topology requires larger total capacitance, and causes the circulation of additional currents that increase the RMS current flowing in the full bridge.

The topology introduced in [10] uses a single power decoupling capacitor, however it poses tight constraints on its maximum and minimum voltage, and includes a DC link capacitor of considerable size. Moreover, the RMS current stress in the half-bridge that drives the power decoupling capacitor is much higher than RMS of grid current.

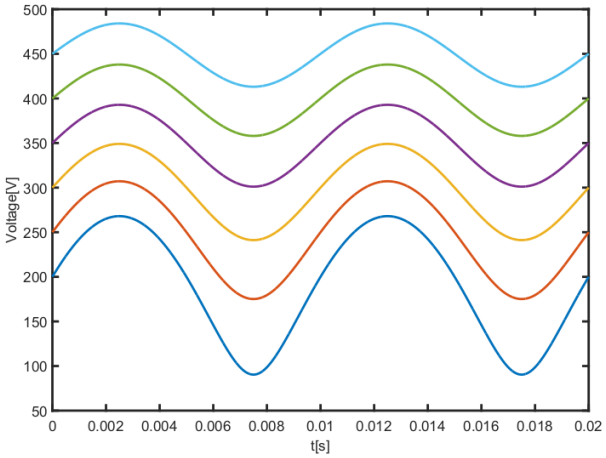

Fig. 1. Power decoupling capacitor voltage waveform, $P = 1kW$, $C = 100\mu F$, $\omega = 2\pi 50 \frac{rad}{s}$, various value of V_0

The topology proposed in this paper achieves a completely independent control of the voltage applied to the power decoupling capacitor, which is connected to the AC side of the converter through a couple of bidirectional switches, soft commutated at line frequency.

The new solution provides active power decoupling using a small required size of the power decoupling capacitor, and at the same time reducing the RMS current stress in the main full bridge, without adding high switching frequency devices.

II. Power Decoupling

The energy balance of a converter can be expressed as in eq.1, where $E(t)$ it the function of energy stored in the converter over time, t_0 is an arbitrary instant of time, and P_{in}, P_{out} are the power flowing in and out of the converter.

$$E(t) - E(t_0) = \int_{t_0}^{t} P_{in}(t^*) - P_{out}(t^*) dt^* \qquad (1)$$

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Assuming the power transferred from the DC source to the grid to be constant and equal to P, i.e. ideal power decoupling is in place, the inverter to operate at an arbitrary power factor and neglecting losses, the difference between the instantaneous powers flowing in and out the inverter is calculated as follows:

$$V_g(t) = \sqrt{2} V_g \sin(\omega t) \tag{2}$$

$$I_g(t) = \frac{\sqrt{2}}{V_g}\Big[P\sin(\omega t) - Q\cos(\omega t)\Big] \tag{3}$$

$$P_{out} = V_g(t)\, I_g(t) = P\left[1 - \cos(2\omega t)\right] - Q\sin(2\omega t) \tag{4}$$

$$P_{in}(t) - P_{out}(t) = P\cos(2\omega t) + Q\sin(2\omega t) \tag{5}$$

Where V_g is the RMS line voltage, P and Q are the active and reactive power injected from the converter to the grid, and ω is line pulsation.

Substituting that in 1, the result is:

$$E(t) - E(t_0) = \int_{t_0}^{t} P\ \cos(2\omega t^*) + Q\ \sin(2\omega t^*) dt^* \tag{6}$$

Energy stored in the reactive elements in a power converter is a function of the voltages in capacitors and current in inductors. Energy stored in small size filter inductors and capacitors can usually be neglected, so that only a few capacitors are to be taken into account, generally the DC link capacitor and, if present, the capacitor of the ripple port.

$$E(t) = \frac{1}{2}\sum_i C_i V_i^2(t) \tag{7}$$

Substituting 7 in 6 the result is a relation between voltages in power decoupling capacitors over time.

$$\begin{aligned} &\frac{1}{2}\sum_i C_i\left[V_i^2(t) - V_{i0}^2\right] = \\ &= \frac{1}{2\omega}\left\{P\sin(2\omega t) + Q\Big[1 - \cos(2\omega t)\Big]\right\} \end{aligned} \tag{8}$$

If only one power decoupling capacitor is used, as in the case of [1] and [10] , and the proposed topology, eq.9 directly yields its voltage waveform over time:

$$V(t) = \pm\sqrt{\frac{1}{\omega C}\left\{P\sin(2\omega t) + Q\Big[1 - \cos(2\omega t)\Big]\right\} + V_0^2} \tag{9}$$

As pointed out in [1], the sign of the voltage is unimportant.

A family of voltage waveforms that, if applied to the same capacitor, yield the same ripple power, for different values of V_0, is shown in figure 1.

III. Proposed topology

A. Description

The proposed topology, shown in figure 2, is made up by a full bridge grid interface, with the addition of a power decoupling capacitor which is alternatively connected to each grid terminal through the switches S_1 and S_2.

The switches S_1 and S_2 have to be capable of reverse voltage blocking. This can be achieved, for example, using two mosfet or IGBT connected in antiparallel or a combination of a diode bridge and a mosfet or IGBT. Another possibility, since capacitor current is equal to zero during the commutation, is the use of two TRIACs.

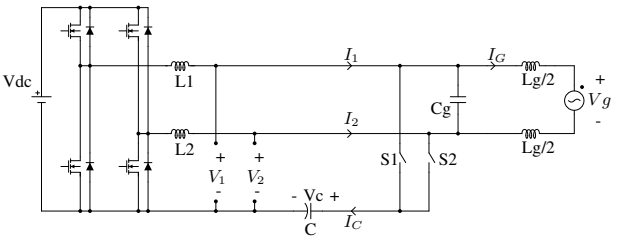

Fig. 2. Proposed topology

This topology is able to provide power decoupling without a large DC link capacitor, while having significant advantages:

- Low total capacitance needed;
- High efficiency of the PWM H-bridge.

B. Steady-state analysis

The switches are operated at each zero crossing of grid voltage, in order to connect the power decoupling capacitor to the positive terminal of the grid. When S1 is closed and S2 is opened, the steady state voltage modulated by the half-bridge connected to L_1 is equal to the power decoupling capacitor voltage V_C, while the steady state voltage modulated by the other half bridge is equal to $V_C - V_G'$.

Voltages V_1 and V_2 have to be controlled as follows:

$$V_1(t) = \begin{cases} V_C(t) & \text{if } V_g(t) \geq 0 \\ V_C(t) - |V_g(t)| & \text{if } V_g(t) < 0 \end{cases} \tag{10}$$

$$V_2(t) = \begin{cases} V_C(t) - |V_g(t)| & \text{if } V_g(t) \geq 0 \\ V_C(t) & \text{if } V_g(t) < 0 \end{cases} \tag{11}$$

Thus, the steady state currents I_1 and I_2 flowing in the half bridges bridge arms:

$$I_1(t) = \begin{cases} I_g(t) + I_C(t) & \text{if } V_g(t) \geq 0 \\ I_g(t) & \text{if } V_g(t) < 0 \end{cases} \tag{12}$$

$$I_2(t) = \begin{cases} I_g(t) & \text{if } I_g(t) \geq 0 \\ -I_g(t) + I_C(t) & \text{if } I_g(t) < 0 \end{cases} \tag{13}$$

Since the capacitor is always connected to the positive terminal of the grid, the steady state voltage modulated by the half bridge that is not directly connected to the capacitor is always lower than the capacitor voltage, and equal to $V_C(t) - |V_g(t)|$. This allows the maximum capacitor voltage to be equal to $V_D C$, while the minimum capacitor voltage has to be higher than $|Vg(t)| \forall t$, so that $V_C(t) - |V_g(t)|$ is always higher than zero.

The steady state voltage waveform $V_C(t)$ can be derived directly from eq.9:

$$V(t) = \sqrt{\frac{1}{\omega C}\left\{P\sin(2\omega t) + Q\Big[1 - \cos(2\omega t)\Big]\right\} + V_0^2} \tag{14}$$

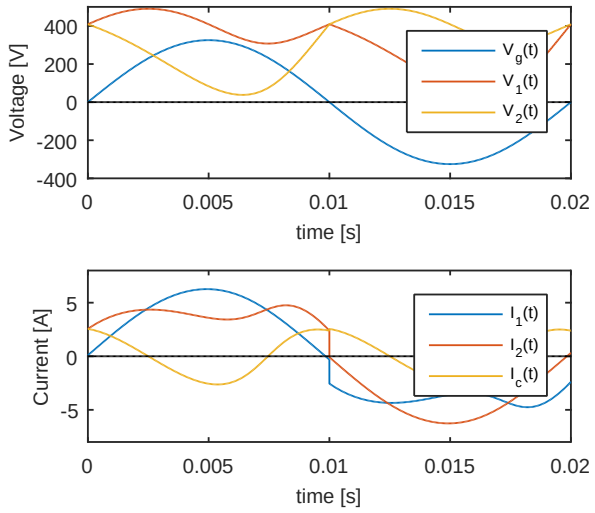

Fig. 3. Voltage and current waveforms

$V_{DC} = 500V, P = 1kW, f = 50Hz, C = 38\mu F$

Capacitor current is obtained deriving its voltage over time (or simply dividing the ripple power by the voltage):

$$I_C(t) = \frac{P\cos 2\omega t + Q\sin 2\omega t}{\sqrt{\frac{1}{\omega C}\left[P\sin 2\omega t + Q\left(1-\cos 2\omega t\right)\right] + V_0^2}} \tag{15}$$

Knowing power decoupling capacitor voltage and current, grid voltage and current and eq.10-13, the steady state voltage and currents V_1, V_2, I_1, and I_2 can be calculated. The resulting waveforms are plotted in figure 3.

C. Destructive interference

Since, as shown in eq.12 and 13, I_1 is equal to $I_g(t) + I_C(t)$ when $V_g(t) \geq 0$, and I_2 is equal to $-I_g(t) + I_C(t)$ when $V_g(t) < 0$, it follows that the current flowing in the half bridge directly connected to the power decoupling capacitor is equal to $|I_g(t)| + I_C(t)$.

This destructive interference occurs both in case of active power in injected in or absorbed by the grid: in case of negative power, the current flowing in the half bridge directly connected to the power decoupling capacitor becomes $-|I_g(t)| + I_C(t)$, but the capacitor current I_C also changes sign.

As can be seen in figure 3, the first harmonic component of the capacitor current is almost opposite in phase with respect to the first harmonic of rectified grid current. Because of this, the RMS value of the current flowing in the half-bridge that drives both capacitor current and grid current is lower than the RMS current of the grid alone. For example, using the parameters indicated in figure 3, the RMS value of grid current Ig_{RMS} is 4.35 A, while the RMS value of $|I_g(t)|+I_C(t)$ is 3.95 A. The RMS value of the current flowing in both half bridges over a grid period is thus lower than grid current, in this example 4.15 A.

The injection in the grid of reactive power involves a change of phase on the first harmonic of capacitor voltage, as can be seen in figure 4. In case of a purely reactive power injected in the grid, the first harmonic of capacitor voltage is in phase with the first harmonic of rectified grid voltage if the reactive power is positive (capacitive behaviour), out of phase if it is negative.

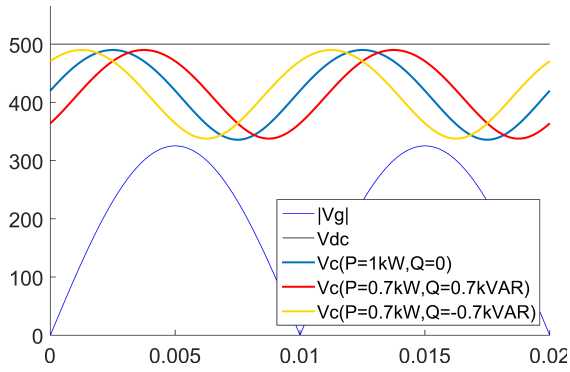

Fig. 4. $V_C(t)$ at various value of the displacement angle φ

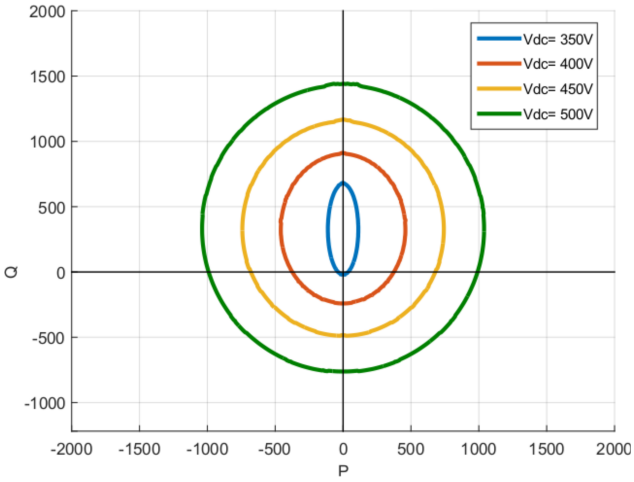

Fig. 5. Capability on the P-Q plane, $C = 40\mu F$

The destructive interference previously described occurs if only active power in injected in or absorbed by the grid, while, in case of purely reactive power transfer, the fundamental components of capacitor and rectified grid current are out of phase by $\frac{\pi}{2}$, so the RMS of the sum is bigger.

D. Capability

The voltages modulated by the two half-bridges V_1 and V_2 are constrained between zero and V_{DC}. Since, as previously described, one is equal to V_C and the other is equal to $V_C - |V_G|$, it follows that the voltage applied to the power decoupling capacitor has to be lower than the DC link voltage and higher than the rectified grid voltage:

$$|V_G| \leq V_C \leq V_{DC} \tag{16}$$

An increase in the active and/or reactive power injected or absorbed by the grid, translates in additional ripple power, and thus in bigger ripple voltage applied on the capacitor, as visible in eq.9. Since the ripple voltage has to respect the constraints defined in eq.16, given a fixed capacitor size there is a maximum power that can be exchanged with the grid while still having a complete power decoupling.

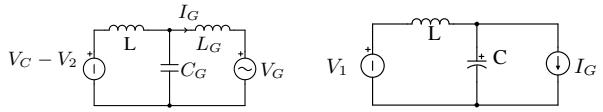

Fig. 6. Equivalent circuits, S1 on

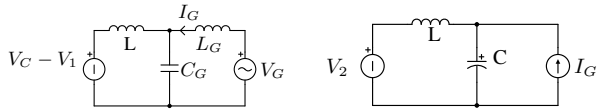

Fig. 7. Equivalent circuits, S2 on

TABLE I
CONFIGURATION CONTROL

Status	S_1	S_2	DCY_1	DCY_2
$V_g > 0$	ON	OFF	DCY_{Vc}	DCY_{Ig}
$V_g < 0$	OFF	ON	$1 - DCY_{Ig}$	DCY_{Vc}
$V_g \simeq 0$	-	-	0	0

Figure 5 shows the limits of the capability of the converter, for a fixed value of power decoupling capacitance (in this case $40\mu F$) and various value of V_{DC}, in the P-Q plane.

Each point in figure 5 is calculated by fixing the displacement angle φ and finding the value of apparent power that corresponds to the maximum capacitor voltage ripple:

$$\begin{cases} \max V_C = V_{DC} \\ \min(V_C - V_G) = 0 \end{cases} \tag{17}$$

The same method can be used to calculate the minimum capacitance needed, given a required P and Q.

For a DC link voltage of $500V$, a line RMS voltage and frequency of $230V$ and $50Hz$, and a required active power P of $1kW$, the minimum capacitance needed is $\simeq 38\mu F$.

IV. CONTROL CONCEPT

A. Description of the system

Since the converter works in two different configuration, depending on which one of the power decoupling capacitor switches is closed, the control system has to be able to function in both configurations, and to withstand the configuration change.

The converter has to be able to regulate grid current, and to remove the DC current ripple regulating the power decoupling capacitor voltage by controlling the duty-cycles of the two half bridges. The system is thus a MIMO, with two inputs and two outputs.

The voltages modulated by both half bridges have an influence on both grid current and power decoupling capacitor voltage; however the size of the power decoupling capacitor is such that its voltage is slowly changing, so that the action of the half bridge directly connected with the capacitor on grid current is slow. The system can thus be modelled by two SISO.

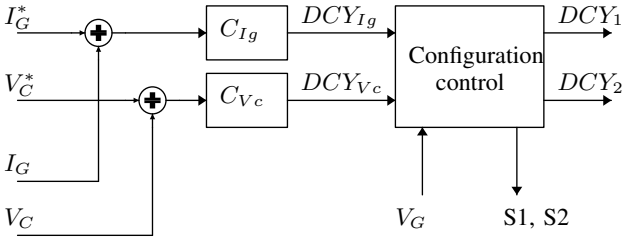

Fig. 8. Control structure

B. Equivalent circuits and control

The system can be represented by the equivalent circuits shown in figure 6 and 7.

The equivalent circuit for grid current is an LCL filter. The design and control strategies for this kind of circuits are well-known [11][12]. In this case, a simple PI controller was used.

The equivalent circuit for power decoupling capacitor voltage control is a simple LC circuit, with the addition of a disturbance constituted by the grid current. Since grid current is low frequency, its action is negligible at control frequencies. Moreover, because of the size of C, the resonant frequency is low as well, and the controller can be as simple as a P. Since the scope is to prove the ripple cancellation equations introduced in section II, in this case the ideal capacitor voltage waveform is used as reference for the controller.

C. Configuration change

Since the two inductors L_1 and L_2 have the same inductance, the system is symmetric, with the exception of the sign of grid current, as can be seen in figures 6 and 7.

Because of this, the same capacitor voltage controller can be used in both configurations, by alternately tying its output to the modulator of the half bridge that is directly connected to the capacitor (that is, the capacitor voltage controller controls V_1 when $V_G > 0$ and V_2 when $V_G < 0$). The same thing can also be done with the grid current controller, changing the sign of the controller gain after each configuration change.

In order for the controller to operate smoothly, not only the structure but also the state of the equivalent system seen by the controller has to be the same before and after the configuration change. In particular, the currents flowing in the inductors L_1 and L_2 have to be equal, since failure to do so results in unacceptable spikes in the grid current following the configuration change.

To easily achieve this, the active switches of both half bridges are quickly turned off prior to the configuration change, so that the converter is forced in DCM and both current are equal to zero when the change occurs. This also helps the commutation of S_1 and S_2, since the capacitor current, being equal to the sum of I_1 and I_2, also is zero during switching.

In the period of time that goes from the turn off of the active components of the bridges to the closing of the next capacitor switch, the control action on grid current is suspended. For this reason, it is important that this operation is executed at the zero-crossing of grid voltage.

TABLE II
SIMULATION PARAMETERS

V_g	230	V_{RMS}	V_0	408	V
P	1	kW	f_s	20	kHz
V_{DC}	500	V	Cg	1	μF
C	38	μF	L_1, L_2, Lg	1	mH

The filtering action of capacitor C_g helps to measure grid voltage, in order to correctly identify the moment of zero-crossing even in presence of noise on the grid side.

V. Simulation

A time domain simulation of the proposed topology was implemented using Simulink and PLECS toolbox. Simulation parameters are shown in table II. The resulting waveforms of current and voltage in the PWM bridge arms and DC and AC currents are shown in figure 9. The DC source was modelled as an ideal voltage source with no series impedance. The DC current waveform shown in red is filtered via a moving average that removes only the switching frequency ripple.

VI. Conclusion

This paper introduces a new single phase AC/DC converter, suitable for low voltage grid connection of DC systems, that is capable of active and reactive power injection and provides active power decoupling without a dedicated Ripple-Port and without a big DC link capacitor. Ripple power cancellation is achieved using a single decoupling capacitor alternatively connected to each terminal of the grid via two switches operated at grid frequency.

A mathematical model used to achieve the power decoupling capacitor voltage waveform is described, and a control scheme is proposed and validated in simulation.

The results show that this topology offers active power decoupling, with a small capacitor and low RMS current flowing in the bridge arms, making it a promising solution for developing high power density single-phase AC/DC converters suitable for grid-connected distributed generation and energy storage systems, capable of bidirectional power flow.

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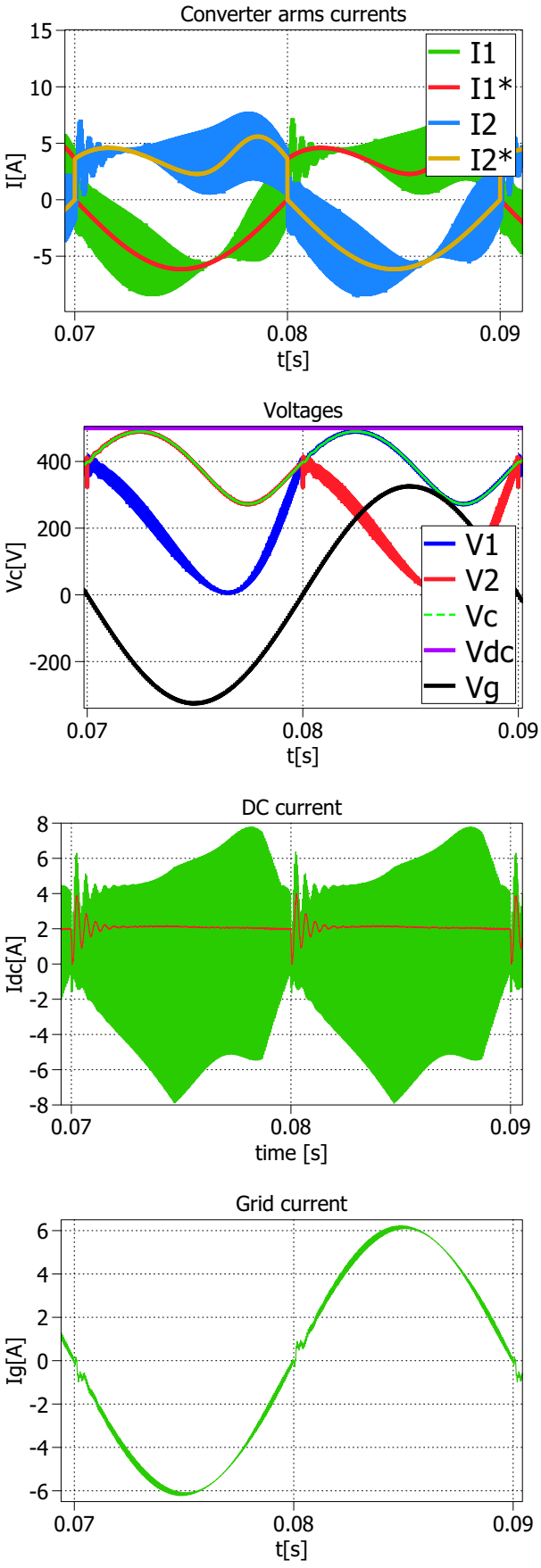

Fig. 9. Simulation results

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