Design and Construction of a Co-Planar Power Bus Interconnect for Low Inductance Switching

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***Abstract*—A co-planar tab-slot type of interconnect demonstrator for connecting power switching devices and DC bus capacitors has been designed and constructed, aimed at low inductance switching. The demonstrator is composed of a double-sided tab connector and a dual polarity slot. This type of interconnect eliminates the use of screw terminal connection between a power module and the DC bus as well as between the DC bus and power capacitors, thus serves to maintain a co-planar current profile throughout the power distribution path. Parasitic analysis both in impedance testing and in Finite Element simulation suggests that the inductance in the bus loop of the demonstrator is approximately half of that achieved in an equally dimensioned busbar with conventional screw terminals.**

Keywords—planar interconnect; low inductance; tab-slot

I. INTRODUCTION

Low inductance power circuit is critical for safe and efficient operation of high current, high frequency power electronics systems. Over years of efforts to lower parasitic inductance in switching loop, one successful development is the planar busbar which provides the greatest surface area for mutual flux cancellation [1]. However, the benefit of this low inductance design is easily compromised at both ends of the busbar where screw connections are employed to distribute power. Inevitably this causes disturbance of current path in the bus layers and effectively disables the mutual flux cancellation. A previous attempt to overcome such compromise has seen the elimination of screw connections in the power module terminal end [2], whereas in the bus capacitor end, screw terminal connections still prevailed. In this work, an interconnection concept of an alternative design has been proposed and a preliminary demonstrator built, which aims to maintain the co-planar current profile throughout the power distribution path. Based on the proposed concept, a complete half bridge inverter switching cell will be delivered in the near future in which screw terminal connections are to be entirely eliminated.

II. DESIGN CONSIDERATIONS

Fig. 1 illustrates a schematic of a switching cell where low inductance is achieved by employing the proposed co-planar interconnect. The interconnect which establishes DC-link between the switching devices and bus capacitors features a double-sided tab connector (essentially the power terminals of a planar switching module [3], see Fig. 2 left), and a receiving slot for mating the tab connector by a spring contact mechanism constructed at one end of the busbar pair (Fig. 2 right).

A. Power Module Design

Fig. 3 shows in two orientations the cross sectional views of an illustrative power switching module assembly which features a planar interconnect substrate with double sided co-planar power terminals for external connection. The interconnect substrate also houses the gate terminals of the switching devices.

B. Design of DC-Link Receiving Unit

Fig. 4 shows schematically a pair of sheet conductors with a 'comb' shaped spring contact area at one end for secure mating with a co-planar tab connector and an opening at the other end for connecting a bus capacitor (metallized film type) in a co-axial configuration. The plastic case for accommodating the sheet conductors is not shown in the schematic.

III. MANUFACTURE OF DC-LINK UNIT

As illustrated in Fig. 1, the core of this proposed concept is the realization of the DC-link which bridges the power switching module and the bus capacitor in a co-planar / co-axial format. Therefore the manufacture of the DC-link unit naturally becomes the focus of this work to demonstrate the co-planar / co-axial interconnection. The following will detail the manufacturing process for the sheet conductors (as shown in Fig. 4) and the plastic case housing the conductors.

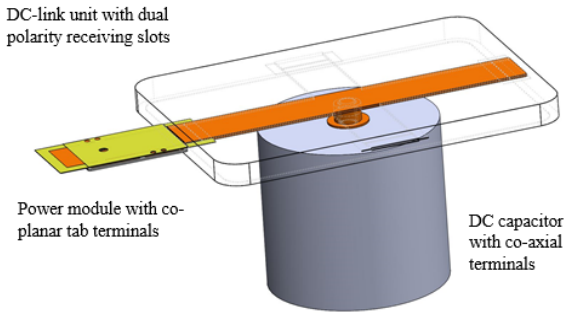

Fig. 1. Schematic of the co-planar interconnection concept

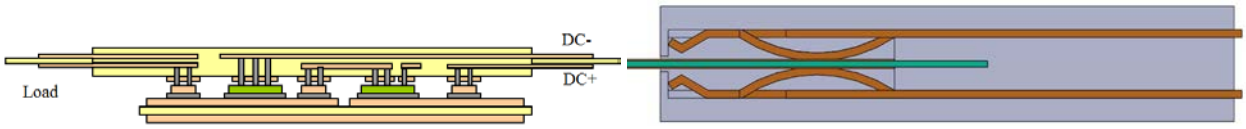

Fig. 2. Schematic of a power module (left) and (right) with its tab terminal mated with the designed slot

A. Manufacture of Conductors

The material used for making the conductors is a copper-beryllium alloy CuNi2Be due to requirements for enhanced mechanical strength and surface hardness compared with copper [4]. A pair of copper alloy sheets were first formed by laser cutting; then the curved strips of the conductor for spring contact were formed by a press punching process using a custom designed press tool and die set; finally any excess material of the formed conductor was removed by using a ceramic disc cutter.

B. Manufacture of Plastic Case

By design, the plastic case is detachable for easily accommodating the formed conductors. Each detached part was additively manufactured with a thermoplastic aliphatic polyester (polylactic acid or PLA) by an Ultimaker 2+ 3D printer (Ultimaker B.V. The Netherlands) using a fused filament fabrication process. The 3D printed parts were then assembled by nylon bolt-nut fixing at sides.

C. Manufacture of a planar tab connector

For demonstration purpose, a double-sided co-planar tab connector was manufactured by laminating two copper foils with a polyimide sheet. In the lamination process, the foils were first attached to both surfaces of the polyimide sheet by using a DuPont™ Pyralux LF sheet adhesive; then the whole assembly was subjected to the laminating conditions specified in the adhesive technical data sheet, i.e. pressurized to 300 psi at 190 °C for 90 minutes.

Fig. 5 shows photos of a planar tab connector, a film capacitor with co-axial terminals, the manufactured DC-link unit for mating the connector and the capacitor, and the assembled demonstrator of the proposed co-planar interconnect.

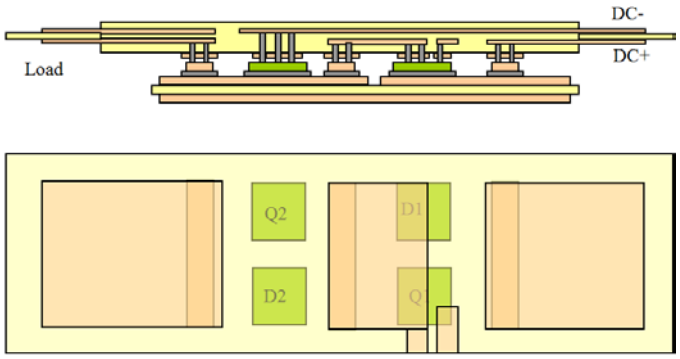

Fig. 3. Schematic of an illustrative planar power module assembly

IV. Evaluation of Bus Loop Inductance

A. Methods of Evaluation

A Keysight E4990A impedance analyzer (Keysight Technologies UK Ltd) was used to measure the parasitic inductance within the bus loop. The bus loop was created by short-circuiting the two co-planar terminals of the tab connector using a thin silver foil attached to both terminals. The attachment was consolidated by the use of a Pb-Sn-Ag solder paste and a reflow process at 220 °C for 5 minutes. Two small copper strips were also soldered to the other end of the sheet conductors (opposite the spring contact end), so as to facilitate the connection of the DC-link unit to the terminal fixture of the impedance analyzer.

A simplified co-planar busbar interconnect demonstrator, with dimensions equal to those of the sheet conductors (excluding the 'comb' portion) inside the DC receiving slot and with screw connection terminals, was also built as a comparison to the proposed tab-slot interconnect with regards to the parasitic inductance in the bus loop. The screw-terminal busbar was manufactured by attaching two copper sheets onto both surfaces of a polyimide sheet with epoxy resin used as the joining media; while the loop was formed by short-circuiting the two terminals with a third copper conductor via screw connection. Connection to the impedance analyzer was made in a similar way as for the DC-link unit described above.

Finite Element Analysis (FEA) was also performed with simulations run in Ansys Maxwell on two models, each in exact representation of one of the physically built demonstrators. The simulation results were compared with those obtained from impedance testing so as to validate the simulations performed in the design stage.

B. Results

Fig. 6 shows the parasitic inductance within the bus loop obtained from impedance testing and FEA simulation (both at frequencies sweeping from 10 kHz to 10 MHz) of the two demonstrators. The results show that the testing values are generally 4% - 10% higher than those from simulation across the entire frequency sweep for the tab-slot demonstrator and 2% - 13 % higher in the case of the screw terminal demonstrator respectively. The difference might largely be attributed to the geometric deviation of the manufactured parts from original design.

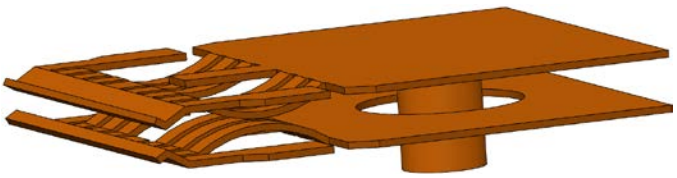

Fig. 4. Schematic of the sheet conductors inside the DC-link unit

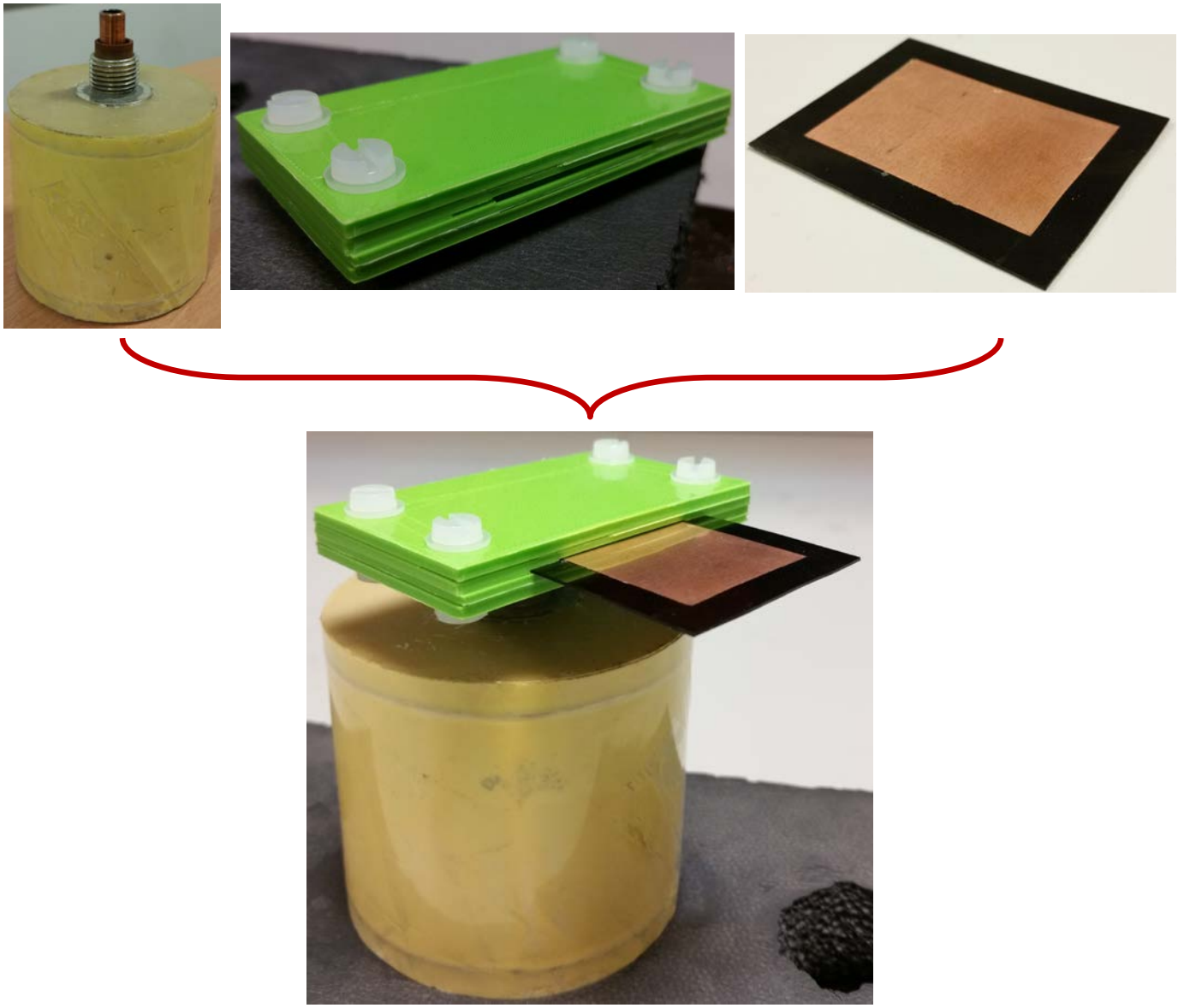

Fig. 5. Photos of a planar tab connector, a film capacitor with co-axial terminals, the manufactured DC-link unit, and the assembled demonstrator

Comparing the two graphs in Fig. 6, measurements from the screw-terminal demonstrator show values at least 90% larger than those of the tab-slot demonstrator, which is well below 10 nH, across the whole frequency range. Finite element simulations performed on models representing the two builds shows similar relationships. In other words, the implementation of the proposed tab-slot interconnect reduces the parasitic inductance in the bus loop to almost half of that achieved in an equally dimensioned busbar with conventional screw interconnection. Table 1 shows the inductance values at 100 kHz obtained from impedance testing and FEA simulation for both demonstrators.

C. *Discussion*

The parasitic inductance of the screw terminal busbar can roughly be considered as the combined contributions from two parts. The first part is a planar busbar while the second being the screw terminals. For the planar busbar part, its contribution to the overall inductance can be calculated using the following formula [5]:

$$L_{bus} = \frac{\mu l}{\pi}\left(ln\frac{d}{t+w} + \frac{3}{2} + \Delta_k + \Delta_e\right) \quad (1)$$

Where μ is the magnetic permeability of the separation material, l the conductor length, d the separation distance, t the conductor thickness, and w the conductor width; while Δ_k and Δ_e are coefficients depending on the geometric parameters of the busbar.

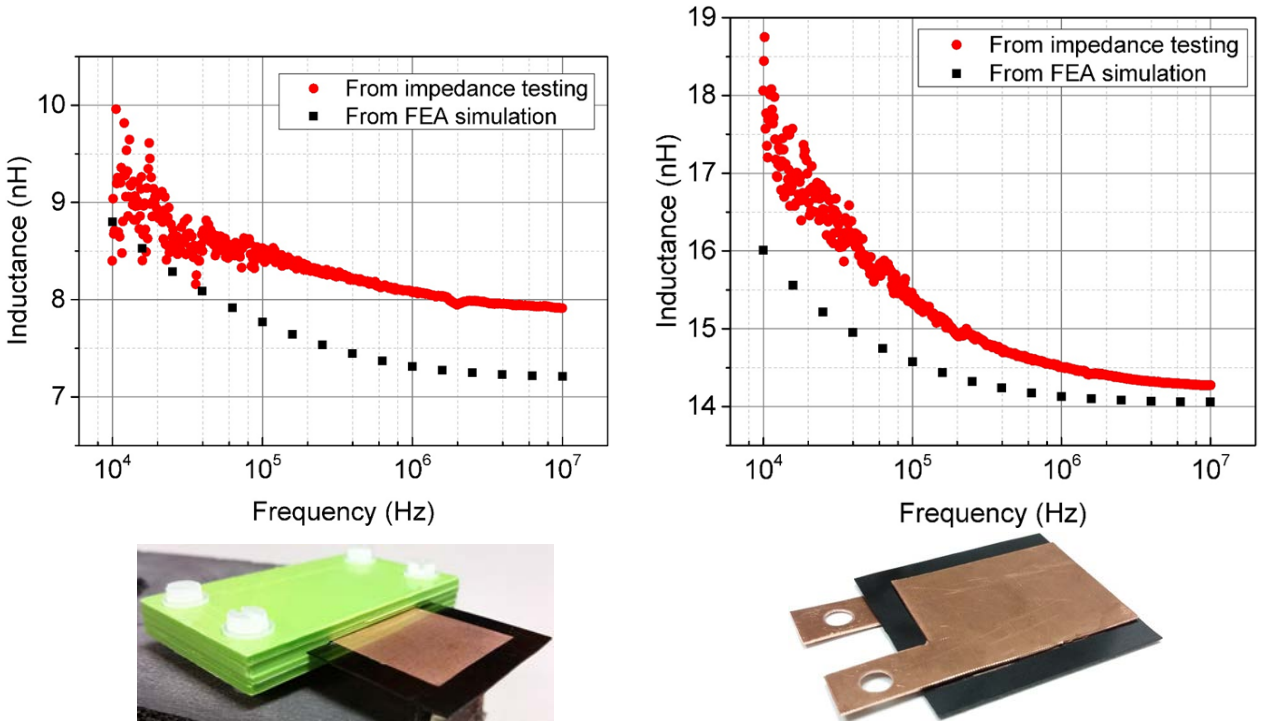

Fig. 6. Parasitic inductance generated in the bus loop of the tab-slot demonstrator (left) and a screw terminal demonstrator (right)

By inputting all parameters representing the planar busbar into (1), the result is 3.3 nH. Thus the contribution of the screw terminals to the overall parasitic inductance at 100 kHz is (15.3 minus 3.3) 12 nH. This generally agrees well with a large number of literatures where screw-terminal incurred inductance alone could easily exceed 20 nH [6]. Combined with contributions from other components in a commutation loop, the overall loop inductance with screw terminal interconnection could consequently increase to tens of nano-henries. Therefore, it is of great benefit to seek alternative approaches, such as the one proposed in this work, to replace screw terminals in the bus interconnection, so that the co-planar current profile can be maintained throughout the power distribution path, thus delivering a low inductance switching loop.

V. Conclusion

A co-planar tab-slot type of interconnect demonstrator for connecting power switching devices and DC bus capacitors with minimum loop inductance has been designed and manufactured. The demonstrator is composed of a double-sided tab connector and a dual polarity receiving slot which houses a pair of sheet conductors with spring contact zone for secure mating the tab connector. Parasitic analysis both in impedance testing and in FEA simulation suggests that the inductance generated in the bus loop of the tab-slot demonstrator is approximately half of that achieved in an equally dimensioned busbar with conventional screw terminals. The demonstrator will thus serve as the base for building a complete half bridge inverter switching cell in the near future.

TABLE I. Inductance Values at 100 kHz

Subject for Evaluation	Impedance Testing (nH)	FEA Simulation (nH)
Tab-slot demonstrator	8.53	7.77
Screw demonstrator	15.34	14.58

Acknowledgment

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