Capacitive effects and memristive switching in three terminal multilayered MoS_2 devices

M.Gater[1], A.M. Adawi[1,*] and N.T. Kemp[2,*]

[1]*Department of Physics and Mathematics, University of Hull, Hull, HU6 7RX, U.K.*

[2]*School of Physics and Astronomy, University of Nottingham, Nottingham, NG7 2RD, U.K.*

* Corresponding authors: A.Adawi@hull.ac.uk, Neil.Kemp@nottingham.ac.uk

***Abstract*—We report on the electrical properties of gated two-terminal multilayered molybdenum disulfide (MoS_2) memristor devices having a planar architecture. The approach based on highly dispersed MoS_2 flakes drop cast onto a bottom gated Si/SiO_2 (100nm) wafer containing metal Pd contact electrodes yields devices that exhibit a number of complex properties including memristive and capacitive effects as well as multiple non-zero-crossing current-voltage hysteresis effects. The devices also show a reaction to a varying gate bias. An increasingly positive gate led to the devices displaying a linear ohmic I-V response while an increasingly negative gate bias drove the system to behave more memristive with a widening hysteresis loop.**

Keywords—memristor, capacitance, memtransistor, three-terminal, transition metal dichalcogenides, MoS_2

I. Introduction

Since the discovery of the TiO_2 memristor [1] by HP labs in 2008 there has been an enormous resurgence in two-terminal resistive switching devices for next generation non-volatile memory and neuromorphic computing applications [2]. Whilst two terminal architectures have enormous scalability advantages for making ultra-high-density memory arrays utilizing the crossbar approach, there are many applications that would benefit from having devices that can be switched or tuned by a third terminal. "Optical gating" is one approach and the development of optical memristors [3-6] as both a light receptor and a computing element has many advantages in neuromorphic computer vision applications where the memristor can act as both a light receptor and a computing element [7]. Another approach, utilizing "electric field gating" and a three-terminal gated architecture, has also recently been developed and these so-called "memtransistors" are expected to be important for imparting complex functions, such as heterosynaptic plasticity, in future neuromorphic systems [8].

Transition metal dichalcogenides (TMD) have been studied as active materials in three-terminal electric field gated approaches, with studies focusing on monolayer materials, such as molybdenum disulfide (MoS_2) [8][9]. Pinched hysteresis loop with zero-point intersection and gating effects have been reported. In contrast, multilayered devices, whilst simpler to fabricate are arguable more difficult to understand and exhibit a range of complex behaviours. Work done previously on monolayer MoS_2 has either used vary large channel widths [8], up to 150 µm, or more recently, has measured through the plane of the MoS_2 using an STM [10]. In both cases, gold was utilized as contact electrodes. In contrast, this study focuses on devices fabricated using active layers of multilayer MoS_2 flakes deposited onto palladium (Pd) electrodes with channel width of 5-10 microns. The device fabrication of this system is much simpler than other systems previously fabricated as there is no need for complex bilayer photolithography techniques or the requirement of achieving monolayer MoS_2 active layers. Additionally, whilst non-zero hysteresis curves have been observed in monolayer MoS_2 [8], double-crossing hysteresis effects, similar to those reported in bulk materials [11] have not yet been reported in MoS_2.

II. Methodology

Silicon wafers containing a 100 nm thermally oxidized surface (Si/SiO2(100nm)) were cut using a diamond scribe into approximately 25 mm x 25 mm squares and chemically cleaned via sonication (Ultrawave u50) in de-ionised water, acetone and isopropanol for 5 minutes each, followed by drying via nitrogen gas. To ensure ultra-clean surfaces, a final cleaning step of 16 minutes in a plasma cleaner (Diener electronic Zepto model 2, power 200 W) was also utilized. The clean silicon substrates then underwent negative image

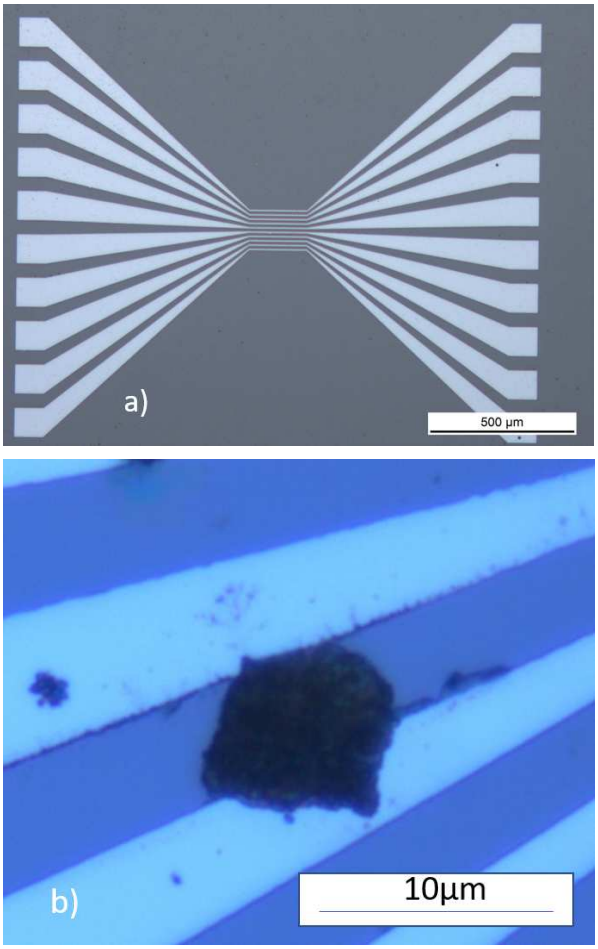

Fig.1. a) A bottom gated Si/SiO_2 silicon chip with Pd source-drain electrodes. b) A MoS_2 flake resting on top of two Pd electrodes (10µm spacing) creating a device.

reversal photolithography using an AZ5214E photoresist (Microchemicals) in order to pattern the device with electrodes having gap separations of 5, 10 and 20 µm.

The metal electrodes consisted of 15 nm of titanium (Ti), as an adhesion layer to the SiO2 surface, and an overlying 30 nm palladium (Pd) layer for making contact to the MoS_2. A typical electrode layout that was used is shown in Fig. 1a). The metal deposition was carried out by an electron beam evaporator (HHV Auto500) with a base pressure of 10^{-7} mbar. Following metal deposition, the silicon chips underwent a lift off process by placing the chips in a beaker containing 100 ml of technistrip solution (P1316 Microchemicals) for 24 hours to remove the photoresist and metal excess layers.

To complete the devices, 10 µL of a highly dilute solution of MoS_2 suspended in isopropanol (2D Semiconductors) were drop cast onto the silicon chips and the alcohol was allowed to evaporate. The devices now patterned with electrodes and containing dispersed MoS_2 flakes (Fig. 1b) were placed on a hot plate to anneal for 30 minutes at 120°C to remove any excess solvents or waters. The backside of the device was scratched using a diamond scribe and a layer of silver conductive paint was brushed into the groove to make the gate electrode connection. The back side of the chip was then attached to a 30 mm x 30 mm copper plate using silver paint, which acted as the electrical connection for the gate electrode. A HP4140B measurement system was used to carry out the current-voltage sweeps and the gate voltage was applied using an Aim-TTi CPX400D power supply.

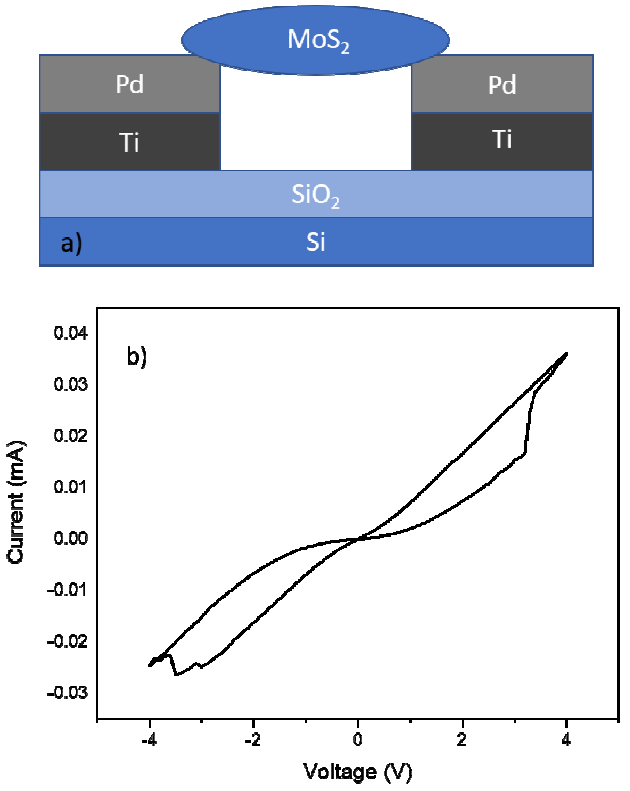

Fig. 2. a) Basic schematic of the MoS_2 memristor device. b) Typical I-V response of a test device with 5 µm electrode spacing and showing a pinched hysteresis loop, which is the signature of memristor behaviour.

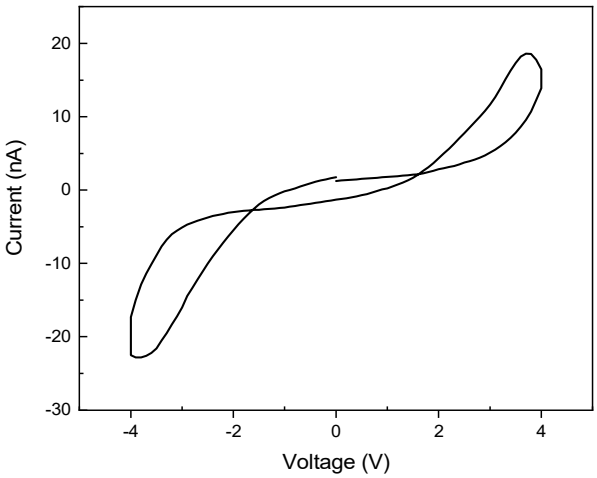

Fig. 3. An I-V response from an MoS_2 device exhibiting non-zero double-crosspoint hysteresis curve.

III. Results and Discussion

In this section we present the results for a typical device architecture that is shown in Fig. 2a. The presence of the flake bridging between the source and drain electrodes was confirmed in all cases by optical microscopy in conjunction with the detection of reasonable large values (>1 nA) for the current. Fig. 2b shows a typical I-V sweep on an area of the device that contains an overlapping MoS_2 flake between two of the electrodes. The I-V sweep ranged from -4 V to +4 V and shows a clear pinched hysteresis loop, which is a signature of memristor behavior. There was no gate potential applied to the gate electrode in this case.

Similar memristor hysteresis loops were observed in multiple measurements across different devices on the same chip and also different chips. It was noted that in all cases, no forming step was required to initiate any switching behaviours. This has also been commonly observed among other reports in the literature for TMD based memristive systems [8].

An interesting effect exhibited in about 25% of the devices is shown in Fig.3. The I-V curve in this case shows a non-zero double-crosspoint hysteresis. Similar effects have been observed in other bulk memristor materials [11] and whilst non-zero crossing has been in observed in monolayer MoS_2 in the low voltage range, where it was speculated to be caused by a memcapacitive effect caused by the electrode [8], the combination of both non-zero and double-crosspoint hysteresis was not observed. The true nature of this capacitance is not particularly well understood, but it has been proposed to be due to the device architecture of memristors, which is structurally similar to that of a capacitor and typically consisting of a vertical layered "sandwich-like" structure of two parallel plates separated by a functional dielectric layer. The capacitance effect can occur when there is a large accumulation of positive and negative ions at the interfaces between the electrodes and the functional layer. A model proposed within the literature to replicate the I-V response is that of an ideal memristor and capacitor in parallel, as demonstrated previously in the case for the presence of a parasitic capacitance [15]. However, the planar architecture

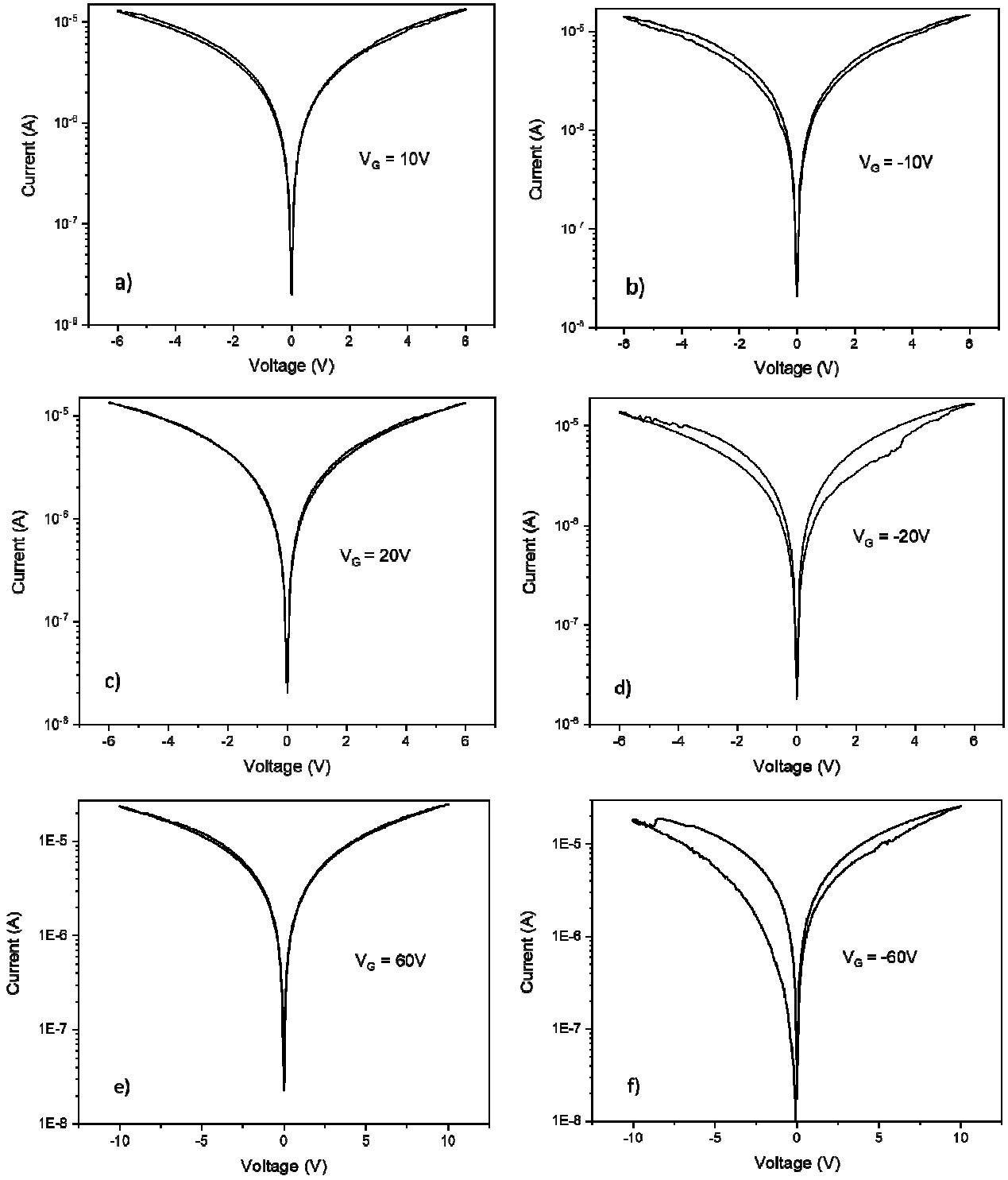

Fig. 4. a-f) Plots of the log source-drain I-V response of a device with a varying back-gate voltage. The plots show a clear separation between a negative and positive gate bias. Positive gate bias causes disappearance of the memristor hysteresis behaviour whilst an increasing negative gate bias causes enhancement of the memristance effect with an increased resistance Off/On ratio

used in our study would have a significantly different capacitance effect compared to that of a vertical "sandwich-like" architecture, especially when also considering the geometric differences consisting of large distance between the source and drain electrode (~5 μm), large length along the electrode (~5 μm) and a very thin flake thickness (≈ 54 nm for the flake shown in Fig. 1b.), which would mean the capacitance should be vanishingly small (~0.5×10^{-18} F). Overall, these issues warrant the need of a much larger investigation aimed at determining how the memristor and capacitance couple in this scenario. This will be done in further studies.

In the following, the effect of an applied gate bias is reported. These results were obtained for a device in which a MoS_2 flake bridged the electrodes across a source-drain gap size of 10 μm. With zero potential applied on the gate (not shown) the device exhibited a clear pinched hysteresis

loop and again no forming step was required to initiate the memristance effect. Firstly, positive potentials were applied to the gate electrode of the device. Fig. 3 a), c) and e) show the I-V sweeps for when the potential was successively increased to +10 V, +20 V and +60 V, respectively. No significant effect was observed in the shape of the I-V curves or magnitude of the source-drain current.

In contrast, negative applied gate potentials produced significant differences in the I-V properties of the device, as shown in Fig. 3 b), d) and f), where the potential was successively decreased to -10 V, -20 V and -60 V, respectively. For successively larger negative potentials on the gate electrode the memristor effect is enhanced. The hysteresis curve opens more and there is there a larger difference between then resistance on (R_{ON}) ad resistance off (R_{OFF}) states. The R_{ON} and R_{OFF} values for a -20 V gate bias are approximately 145 kΩ and 400 kΩ respectively.

The high gate voltages used in this study are in line with what other groups have seen for MoS_2 field effect transistors. However, it is an area of concern since it would negate their potential use in real-world applications. There are several possible ways to resolve this issue. The thickness of the dielectric layer used in this work was relatively thick, 100 nm, and this can be significantly reduced by a factor of 8-10 without much complication. Further reductions in the gate voltage can also be achieved by using high-κ dielectrics instead of silicon dioxide [16]. This allows an increased gating effect (increased gate capacitance) whilst also keeping the dielectric thick enough to be robust and avoid current leakage. Other groups have also reported that the choice of metal electrodes is important [17] since this modifies the contact resistance to the MoS_2 at the source and drain electrodes. Future studies will explore these effects in more detail for the device architecture used in this work.

One mechanism thought to play a role in the gating effect is the migration of substitute metal atoms from the source-drain electrodes into sulfur vacancies within the crystal structure of MoS_2 when the device is under an external bias [10]. The binding energy of sulfur [12] in monolayer MoS_2 is similar to that for the formation of substitutional gold defects (~3 eV) and it has been shown that enhanced electric fields near an STM tip facilitates the migration of gold atoms to defects sites [10]. The reversible nature of this process supports a gate-like mechanism, whereby positive and negative potentials on the gate electrode modulates the formation and migration process, which in turn modifies the conductance and memristor switching properties of the MoS_2 conduction channel between the source and drain electrodes. The presence of grain boundaries in the MoS_2 can enhance this mechanism and modulation of the interface Schottky barrier heights also plays an important role [8].

However, there are still many factors about the switching mechanism that remain unclear. Recently, the presence of adsorbed water molecules and the formation of hydroxyl ions (OH^-) that undergo field driven migration has been shown to play a role in the resistive switching properties of MoS_2 [14]. In this mechanism, MoS_2 acts also as a catalyst causing the splitting of adsorbed water molecules to form OH^-, which then migrate to the metal interface and influence the energy barrier at the source and drain electrodes.

The role of the electrode material is also important and needs to be clarified since memristor switching in MoS_2 has been observed in devices that have electrodes made from metals other than gold, in particular hard metals such as chromium [14] and silicon [8]. Intriguingly, a recent theoretical study proposes that "sulfur popping" and the formation of a virtual filament causes switching in MoS_2 and that the process is independent of the electrode material [13]. To help clarify these effects this current work has used palladium electrodes. Palladium is substantially harder and more robust than gold, yet memristor switching was still observed. Whether Pd atoms migrate or not remains to be determined and further studies will be aimed at determining this effect.

IV. Conclusions

This work has shown the effect of electrical back gating on multilayer MoS_2 lateral devices. The gating effect observed is that with increasing positive gate bias the separation between the resistance R_{OFF} and R_{ON} states disappears, and hysteresis effects are no longer observed. This means the device no longer acts as a memristor but instead becomes purely resistive in nature. In contrast, increasing the negative bias drives the system to act more like a memristor with enhanced separation between the R_{OFF} and R_{ON} states and increased hysteresis. This could have potential applications in the next generation of neuromorphic computing and non-volatile memory with the ability to control the devices synaptic learning properties via electrical back gating.

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