3.3 kV SiC JBS Diode Configurable Rectifier Module

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Keywords

« Wide bandgap devices », « Silicon Carbide (SiC) », « Packaging »,« Diode », « high voltage power converters », « Wind energy »

Abstract

This paper presents the use of innovative high-voltage SiC diode technology in the development of a user configurable full-wave or half-wave rectifier bridge. The devices are of merged Junction-Barrier-Schottky (JBS) type to enable for optimum performance even in the presence of current surges, as demanded by the application. To contain the cost of the proposed solution, their packaging relies on Insulated Metal Substrates (IMS), as opposed to conventional ceramic type substrates. The layout and module pin terminations are chosen to yield optimum electro-thermal and electro-magnetic performance in compatibility with a standard solder and wire-bond assembly process. Preliminary functional static characterization tests at different temperatures are also presented.

Introduction

Over the past few years Silicon Carbide (SiC) has gain more widespread credibility as an interesting substitute of Silicon (Si), especially for high voltage devices and applications, due to its ability to enable high blocking voltages without compromise on on-state and switching performance, in virtue of its higher critical electric field and extremely low intrinsic carrier density [1-7]. In particular, SiC enables the transfer of Schottky-type rectifiers to voltage ranges of several kV's, with lower on-state voltage drops and charge storage/extraction phenomena than the *p-i-n* structure at moderate current values. However, as higher current levels are needed, a bipolar type of diode proves more efficient. This work looks at the development of an uncontrolled diode based rectifier, of common use, for instance, in wind power conversion systems, with the ability to handle repetitive current surges of up to some times the nominal on-state current level [8]. So, to make the most of Schottky and *p-i-n* junction diode features, high voltage 4H-SiC Junction Barrier Schottky (JBS) diodes were designed and fabricated, with a nominal breakdown voltage in excess of 3.3 kV [9]. The devices were packaged in a multi-chip rectifier module configurable as both full-bridge and half-bridge rectifier topology (single phase). In the following, the module design and development are presented, including structural

analysis and the assembly process; finally, results of preliminary static and dynamic electrical characterisation are presented.

Diodes

JBS diodes perform like Schottky diodes at moderate values of conducted current and as bipolar type diodes when the current density increases. A key challenge in developing this technology on SiC is the well-known difficulty of forming ohmic contacts: here, the front-side metallization (anode side) is even more of a challenge since it has to simultaneously provide a Schottky contact to the low doped n-epi and an ohmic contact to the p+ implanted junction barrier (i.e. the PiN part). Promising results, both in terms of on-state performance and ensuring repetitive characteristics among different manufacturing lots, were obtained with the deposition of 100 nm $TiAl_3$ on the front-side and rapid thermal annealing the wafers for 2 min at 980°C [9-11].

Module design

A specific application requirement for the module to be developed, as schematically summarized in Fig. 1, is the possibility for it to be used in both full-wave (Fig. 1 (a)) and center-tapped secondary half-wave (Fig. 1 (b)) transformer isolated rectification schemes. Indeed, both solutions are of common use and offer the possibility to trade-off between transformer design simplicity and efficiency of the rectification process (the full H-bridge being the simpler in terms of magnetics design, but having two diodes conducting in series during rectification and the center-tapped being more demanding from a magnetics design point of view, but offering the possibility to connect the rectifying diodes in parallel pairs, virtually reducing by 4 the conduction losses). So, in the design of the module, special attention was given to developing a package that would ensure the freedom for the final user to implement either configuration, for instance by means of a custom designed external printed circuit board (PCB).

A housing was designed to accommodate a total of four equivalent SiC diodes. Because of the current rating of each individual chip, 6 diode chips in parallel were used for each of the 4 diode switches to ensure a module level nominal rating of 100 A. Fig. 2 shows an illustration of the module layout: diodes B and C have a common cathode, as in both of the two required config-

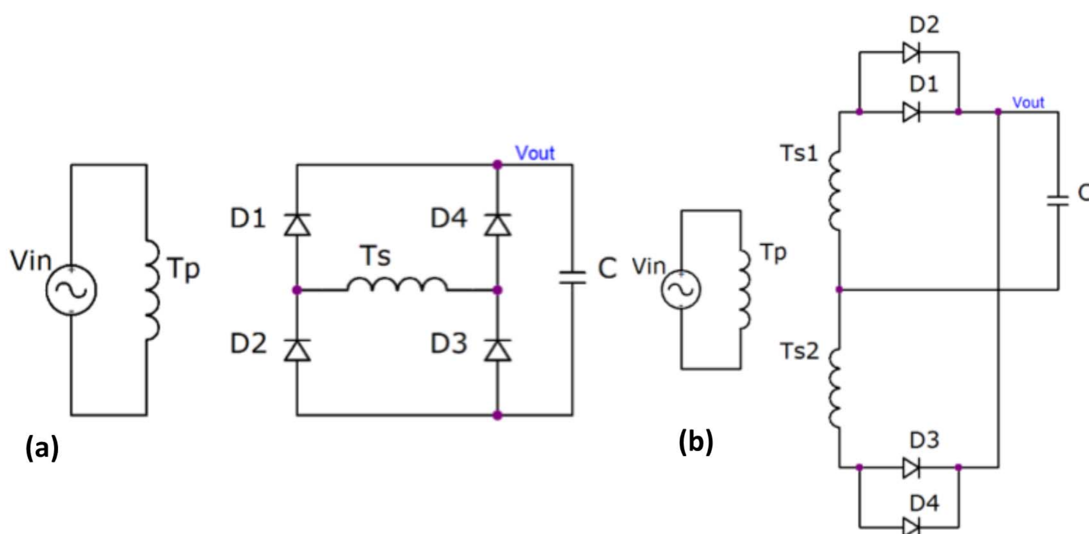

Fig. 1 Intended application of the diode module: (a) full-bridge rectification; (b) half-bridge rectification scheme with centre-tapped transformer. Tp and Ts indicate the transformer primary and secondary windings, respectively.

urations, two diodes always share a common cathode terminal; diodes A and D have fully independent terminals to enable interconnection of the terminals as needed. Each of the 7 independent power terminals is implemented by means of 3 parallel pins, so as to reduce parasitic inductance. As can be seen in Fig 2 (a) (and better still in Fig. 5), these pins are designed with an S-shaped base with the two-fold purpose of enabling ease of mounting (soldering or sintering) and ability to tolerate some degree of mechanical solicitation and stress before compromising or impairing the structural integrity and electrical functionality of the module. Also, the layout takes care of symmetry from both an electrical and a thermal perspective, both at the level of single equivalent diode implementation and at overall module level.

As for the practical implementation of the module, next to the use of HV SiC JBS devices and

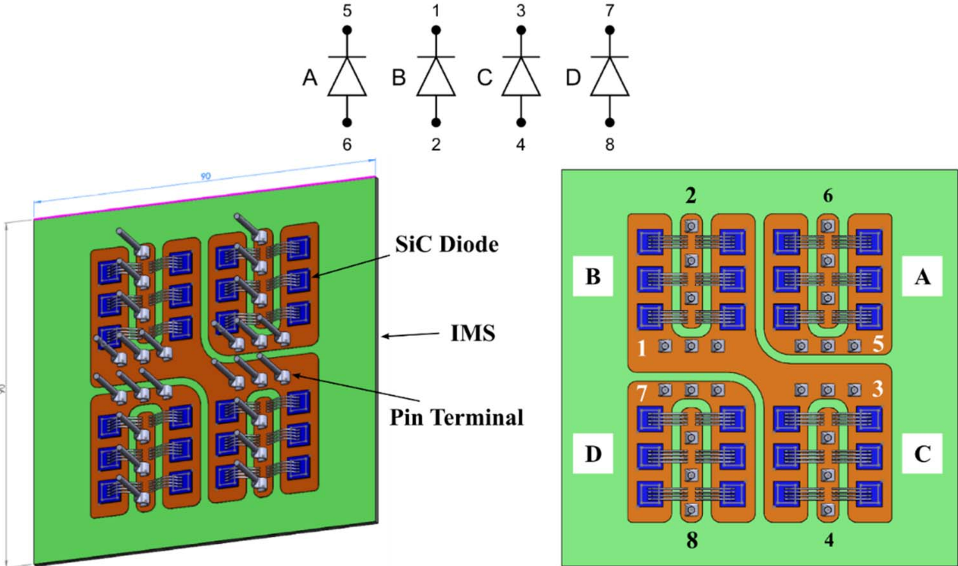

Fig. 2 SiC diode module design, with 6 chips in parallel per diode.

the electrical configurability of the module, a third element of novelty is introduced by using IMS technology for the module main substrate. With some compromise on the thermal performance, which can be entered here in view of the relatively large size of the diodes (5.8 x 5.8 $mm^{2;}$ 400 µm thick), electrically insulated metal substrates offer a low cost alternative to ceramic substrates. Metal substrate circuitry, as illustrated in Fig. 3, consists of a metal base plate onto which a copper conductor layer is attached with a thermally conductive epoxy dielectric. In addition to aluminium (Al), metal substrates such as copper (Cu) and copper-clad molybdenum are suitable as substrates. Alloys are typically chosen for the base metal to yield optimum heat dissipation ability, mechanical integrity, low cost and lightweight construction. Here,

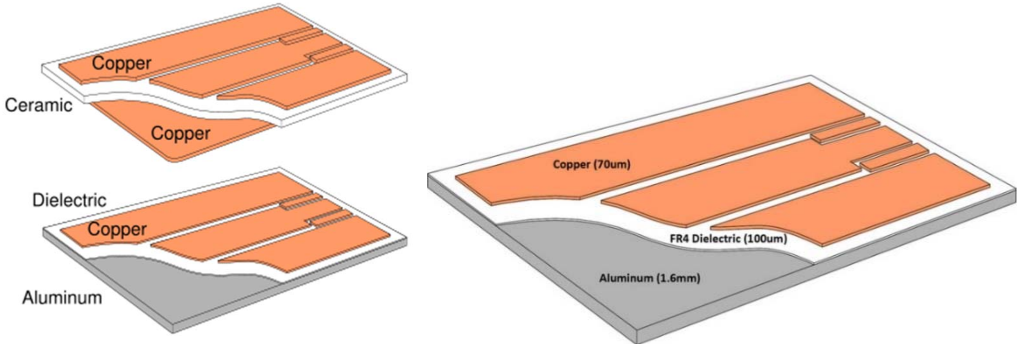

Fig. 3 Illustration of the construction principle of Insulated Metal Substrates (IMSs).

it was decided to use Al to start with. The power tracks are 210 µm thick and the insulating material (FR4) is 100 µm thin to ensure good heat transfer from the devices to the Al baseplate. The power terminal pins are Cu, with Nickel finish, same as the power Cu tracks on the IMS. It should be noted that the 100µm-thick dielectric material were suitable for blocking up to 5kVDC, as specified by the manufacturer [12].

Thermal Simulation

With the structural data above, steady state simulation was carried-out to investigate the thermal behavior of the package, using the commercial software ABAQUS. Fig. 4 shows the resulting temperature field estimation for different heat transfer coefficient applied as a boundary condition on the bottom layer and a power loss of 23W per chip. As can be seen, the maximum estimated temperature is well below the device limits, even in the case of rather poor cooling boundary conditions (147ºC with h=1000 W/m^2.K), confirming the validity of the design in terms of layout and sizing.

Assembly and preliminary characterization

The constituent parts used to build the diode module are shown in Fig. 5. They include:

- Insulated Metallic Substrate (IMS)
- 3.3kV SiC diodes
- Copper power terminal pins

The IMS consists of 100µm-thick insulating materials with a thermal conductivity of 1.6 W/m.K and a dielectric withstand capability of 5kV$_{DC}$. 210 µm thick Cu tracks were used on top of the insulation layer for conducting the rectified load current. All the SiC diodes were

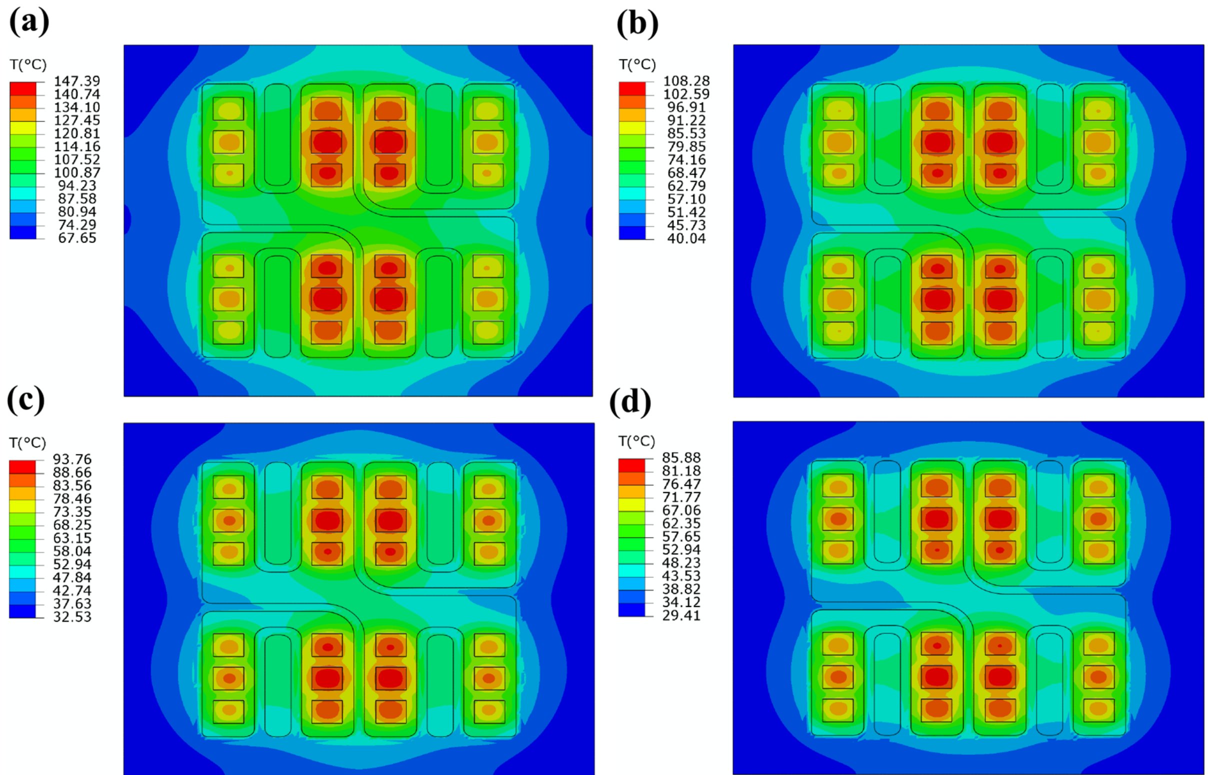

Fig. 4 Steady-state thermal simulations at different heat transfer coefficient (a) 1000 W/m^2.K, (b) 2000 W/m^2.K, (c) 3000W/m^2.K and (d) 4000W/m^2.K. The power loss was set to 23W per chip

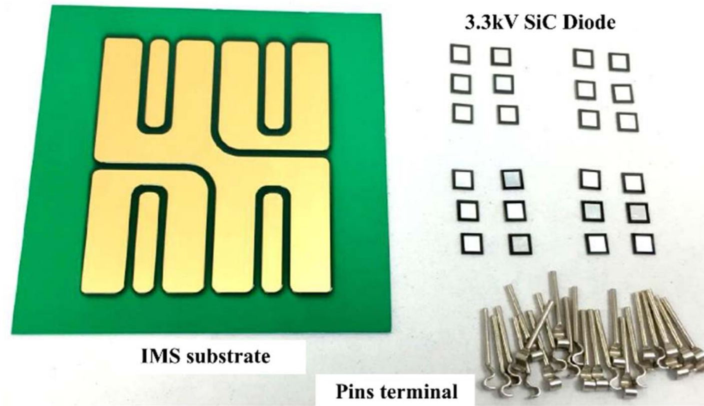

Fig. 5 Parts used for the assembling process: IMS, SiC Diode and Pins Terminal

finished with standard Al top metallization. The power terminal pins are nickel clad copper: they are shaped at the base so as to enable ease of soldering and absorbing some amount of mechanical deformation/stress without compromising the structural integrity of the module.

Fig. 6 illustrates the assembling process of the module. Plasma etching of all parts was used to remove any residual organic contamination, prior to the assembly process. The sequence of steps was:

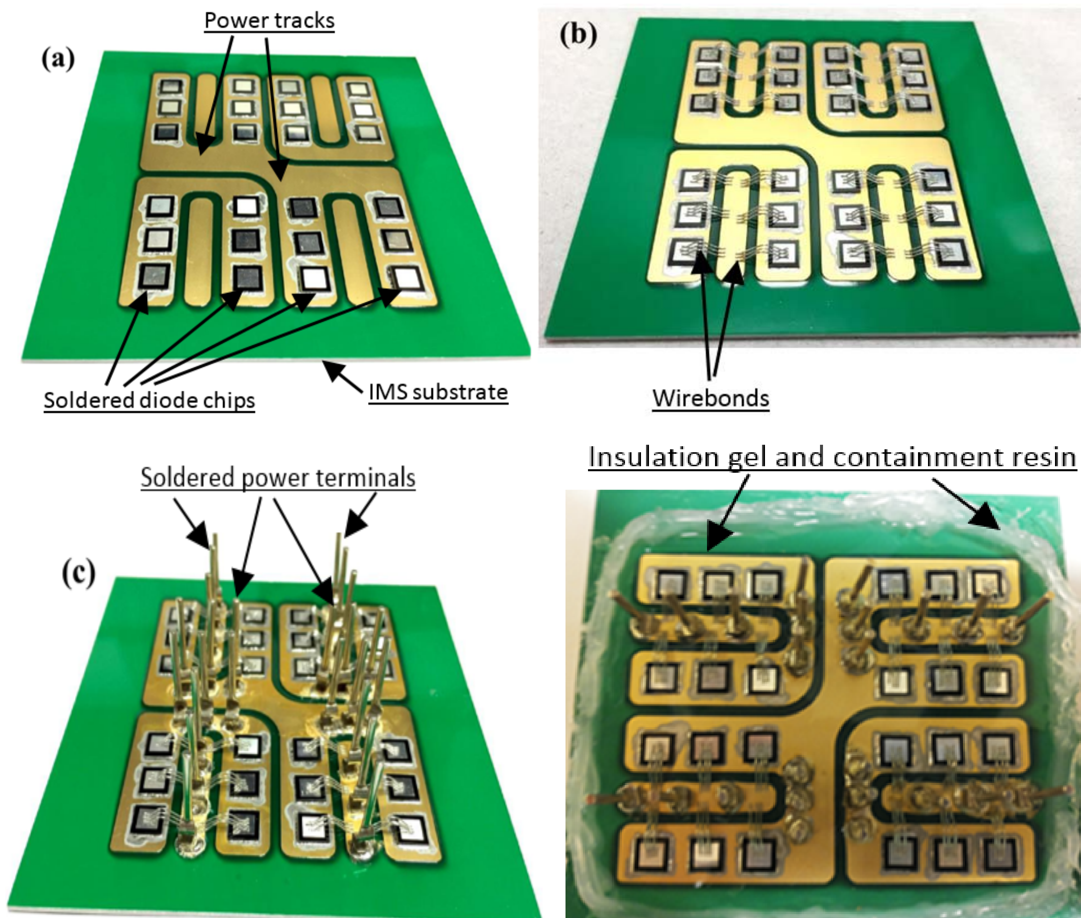

Fig. 6 Photos of the module at different assembling step: (a) Solder reflow of SiC Diode on the IMS; (b) wire-bonding; (c) soldering of the power terminal; (d) insulation and dielectric isolation.

- The SiC Diodes were bonded on the IMS using tin-silver (SnAg) preforms. The solder reflow process was performed under vacuum (Fig. 6 (a)).
- Al wire-bond technology was used to connect the Anode to the Cu tracks (6 (b))
- The pin terminals were bonded using soldering technology (Fig. 6 (c))
- For insulation, the assembly is then covered with Silicone Gel under vacuum and cured at 125°C (Fig. 6 (d)).

Electrical test

Static test

A static current-voltage characteristics test was carried out to test the forward characteristics of the SiC JBS Diode. Fig. 7 shows the forward on-state characteristics of each of the 4 diodes, measured at different values of the baseplate temperature, ranging between 25 and 75ºC. As can be seen, the thermal stability of the diodes performance is very good, especially if compared with Si devices in similar voltage classes.

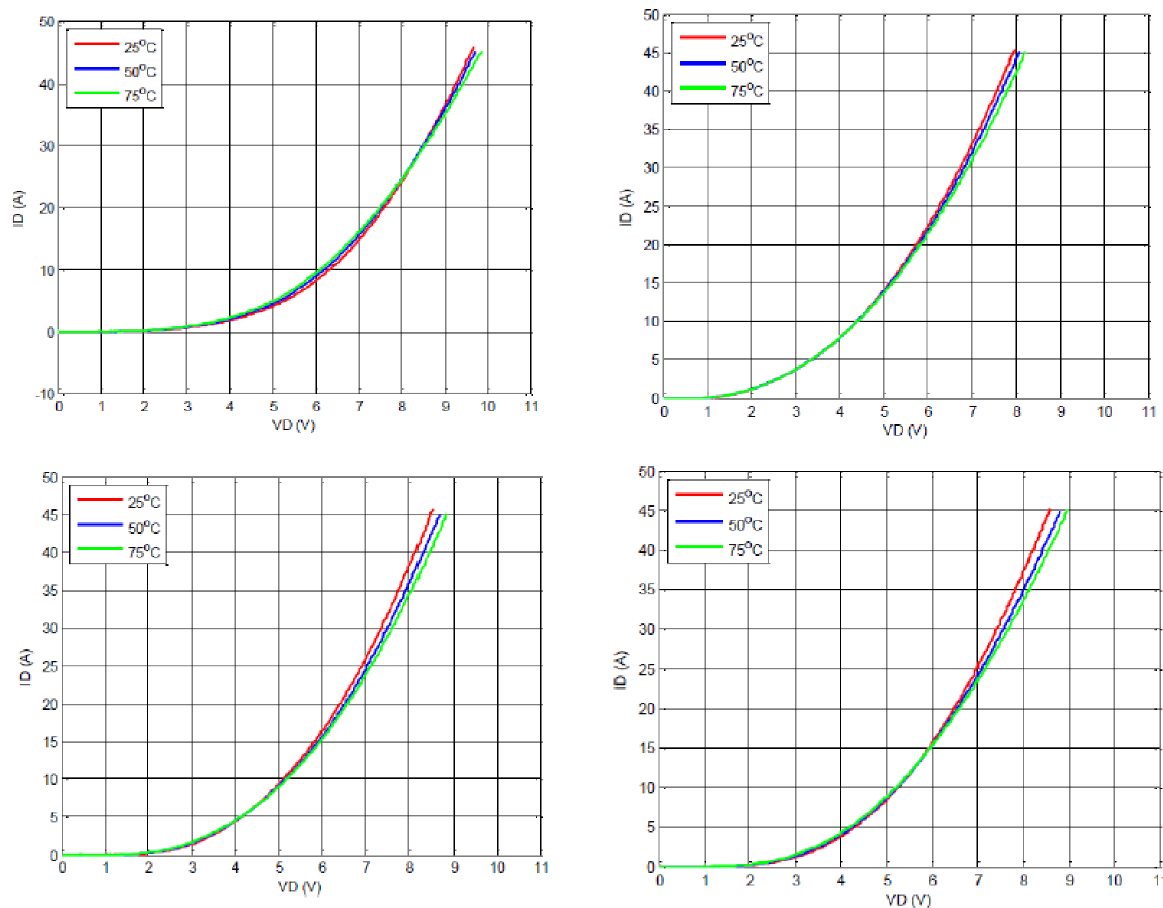

Fig. 7 Measured forward characteristics of the 4 diodes (each diode consists of 6 parallel chips) at different substrate temperatures.

Dynamic test

Double-pulse test is a widely used approach to characterize the switching performance of novel devices and test the packaging parasitic elements. As illustrated in Fig. 8, it is performed by applying a gate signal with two pulses to a switching device: the first pulse is used to charge the load inductor to the desired current level and study the turn-off performance of the transistor (switching MOSFET in Fig. 8) and the turn-on behavior of the free-wheeling diode (the DUT

here); the second pulse, vice-versa, is used to investigate the turn-off transient of the diode and turn-on of the transistor. A SiC MOSFET is used for the active switch; the load inductor is connected in parallel with the SiC JBS Diode module (single diode operation). The experimental test conditions are listed in Table I: in these preliminary tests, the load current was conservatively set at 20-25 A and the case was kept at ambient temperature. Fig.9 shows the experimental current waveforms of 4 SiC JBS Diode during the switching off and on of the SiC MOSFET. The parasitic inductance involved in these tests is external to the module, due to the difficulty of optimizing the interconnection to the test setup.

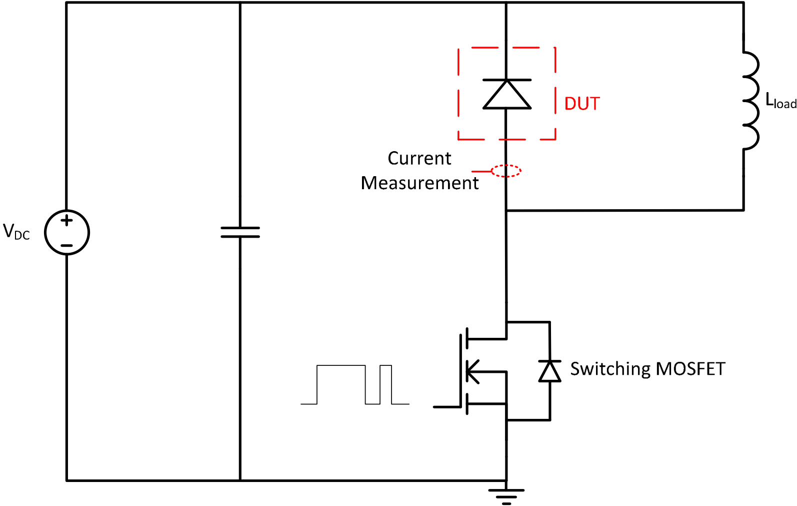

Fig 8. Double-pulse test circuit schematic.

Table I: Experimental parameters for Double Pulse test

Part	**Type**
Diode current (I_{diode})	25A
Gate voltage (V_{GS})	20V/-6V
Load inductance (L_{load})	1mH
Case temperature (T_j)	25°C (Room temperature)
Oscilloscope	Tektronix DPO 7104 (BW=500MHz)
Voltage probe	Differential probe (BW=50MHz)
Current sensor	Rogowski coil PEM CWT1 (BW=20MHz)

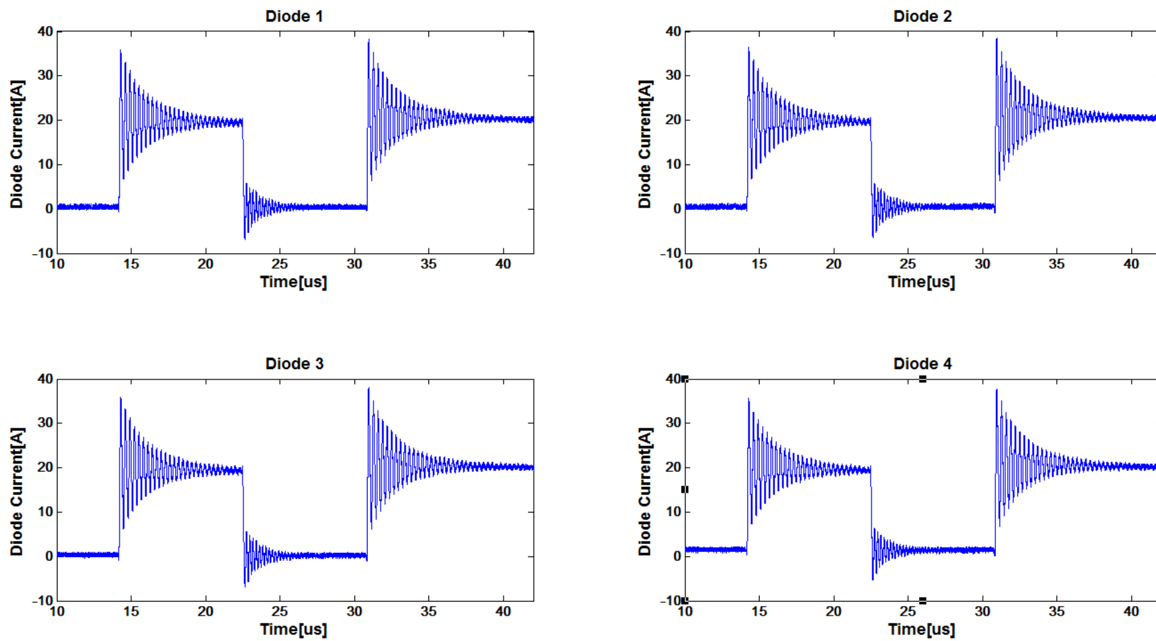

Fig.9 Pulsed current waveforms of the four SiC Diodes in the module.

Conclusion

An innovative high-voltage SiC diode technology in the development of a user configurable full-wave or half-wave rectifier bridge has been presented in this paper. The devices are of merged Junction-Barrier-Schottky (JBS) type to enable for optimum performance even in the presence of current surges, as demanded by the application. An Insulated Metal substrates (IMS) were proposed as a mean for packaging in order to keep a lower cost of the proposed solution, as opposed to conventional ceramic type substrates. The layout and module pin terminations are chosen to yield optimum electro-thermal and electro-magnetic performance in compatibility with a standard solder and wire-bond assembly process. The SiC JBS diodes were electrically tested at different temperatures. Finally, these SiC diodes were tested in a double-pulse test showing their functionality during the switching transient.

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