Towards Distributed Cell-less MIMO Testbed: An RFNoC Implementation

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Abstract—In this extended abstract, we will present a novel cell-less multiple-input multiple-output (MIMO) testbed design and an initial implementation based on the design. The key objective is to design a flexible and scalable architecture to facilitate the Artificial Intelligence (AI)-based beamforming solution, and offload computing extensive algorithms, especially the Channel State Information (CSI) estimation algorithms, to the Field Programmable Gate Arrays (FPGAs), which is to address the challenge for the local signal processing at the distributed Base Stations (BSs). An initial testbed implementation is presented, which has been evaluated in the lab environment with 2 single-antenna BSs and 2 single-antenna users.

Index Terms—Cell-free networks, Software defined radio (SDR), massive multiple-input multiple-output (MIMO), testbed.

I. INTRODUCTION

The novel cell-less network architecture, especially the usercentric method, is one of the promising solutions to address the inter-cell interference in current "cell" based architectures. In the user-centric method, each user can be served via the cooperation of multiple BSs, which helps provide better performance to the original cell-edge users [1]. However, the real-time signal processing (e.g. channel state information (CSI) estimations) with local resources is a very challenging task, especially for the multiple-input multiple-output (MIMO) scenario where distributed BSs are with constraint resources.

There are very few cell-less testbed designs focusing on distributing the signal processing with local BSs, where existing attempts are small-scale and using powerful computing resources to emulate the distributed BSs. This is because the signal processing (especially baseband modules) is mainly using C/C++ based framework (e.g. OpenAirInterface [2]), which are mainly designed for powerful computers and can hardly ensure their real-time performance with embedded devices (e.g. the distributed BSs). The open-source openOFDM and its further developed scheme openWiFi [3] are FPGA based frameworks with a focus on IEEE 802.11 protocols. But it involves non-trivial efforts to integrate high-level signal processing algorithms (e.g. multi-user CSI estimation and beamforming algorithms) and the implementation thereafter.

As part of the AI-enabled Massive MIMO (AIMM) project [4], we will investigate a novel distributed cell-less MIMO testbed design and implementation solution, which focuses on

a flexible and scalable architecture to facilitate the AI-based beamforming solution.

II. TESTBED DESIGN AND IMPLEMENTATION

Here we consider that the distributed BSs are equipped with both central processing unit (CPU) and FPGA resources. The FPGA resources will be exploited to commit real-time and computing extensive algorithms, including multi-user CSI estimation and the baseband signal processing modules (e.g. timing recovery). The embedded CPU resources have computing constraints, e.g. frequency, memory and power, which will only be used for high level algorithms (such as beamforming algorithms). The proposed solution exploits the open source FPGA development framework called RFNoC 4 [5], where the customized modules can be integrated with the existing Universal Software Radio Peripheral (USRP) FPGA modules (e.g. Digital Up Converter (DUC) modules). To facilitate the CPU and FPGA based modules to work in a streamline manner, the drive is also developed using the RFNoC 4 framework for the CPU modules to control and interface with the FPGA modules. The aforementioned components and their mapping to the RFNoC 4 framework is illustrated in Fig. 1.

GNU Radio (CPU)		
GRC Bindings (YAML)	Block Code (Python/C++)	
GNURadio Inferface User module parameters	 Signal Processing Modules (CPU) Graphical User Interface 	
USRP Hardware Driver (CPU)		
Block Description (YAML)	Block Controller (C++)	
Routing: Radio->DDC->User module FPGA Resource Configuration	 x86_64 arch (for PC host) Arm cortext-a9 (for N321 embed) 	
FPGA (USRP N321)		
Block Test Bench (SystemVerilog)	Block HDL(Verilog+VHDL+IP)	
 Simulation with measurements/Matlab Bit-waveform verification 	 Matched Filter (for timing & CSI) SRRC Filter (for pulse shaping) 	

Fig. 1. An illustration of the cell-less MIMO testbed development following the RFNoC 4 framework.

In the design of this cell-less testbed, each BS is fulfilled by USRP N321. Since there are two independent receive/transmit channels, one USRP N321 can be implemented as two independent BSs by a parallel implementation of the same FPGA module with different BS parameters. The antennas for the different BSs on the same USRP N321 can be physically separated by extending cables for lab-scale experiments. The CSI is the key information required for the multiuser MIMO scenarios to optimize the beamforming designs, so that the spatial diversity can be exploited to improve the system throughput when multiple users are served at the same time and spectral bands. Although transmitting all baseband signals from remote antennas to the CPU could exploit the global information for better CSI estimation and demodulation performance, it will also be a challenge to the fronthaul links with raw real-time baseband signals. Therefore in this design for the distributed testbed, the CSI will be estimated locally with the embedded FPGA computing resources at each BS.

Preamble Pilot 1 •••• Pilot K	Payloads
Timing CSI Estimation Synchronization	

Fig. 2. The data frame structure for the multi-user CSI estimation.

The pilot design is following the structure as shown in Fig. 2, whose structure can be further adapted to popular frame designs including IEEE 802.11. For a system with K users, each user is assigned with a specific time slot so that a pilot is transmitted in that time slot for the CSI estimation purpose. For a precise estimation of the CSI, the pilot is using the discrete Fourier transform (DFT) sequence with a length of 64. The CSI estimation is fulfilled by the matched filter (MF), whole filter taps are the DFT sequences. In this way, the estimated CSI can be obtained via the outputs of the MF when the inputs of the MF are the whole DFT sequences, while different users CSI can be distinguished by the time slot this DFT sequence is located to. To reduce the hardware resource complexity, all users are reusing the same pilot sequence.

III. INITIAL RESULTS AND DISCUSSIONS

An initial testbed has been prototyped with the designed baseband modules in Fig. 3, where 2 independent singleantenna BSs and 2 single-antenna users are implemented. For evaluation purpose, the testbed contains only essential modules including timing recovery, CSI estimation and PSK demodulation modules. These modules provides the minimum setup for a complete link layer communication system, where key metrics can be evaluated including bit error rate (BER), data rate and spectrum efficiency.



Fig. 3. An initial testbed implementation with 2 single-antenna BSs and 2 single-antenna users.

The initial testbed has been evaluated in the lab environment, whose results are demonstrated in Fig. 4. Note that in the experiment, only the uplink from the user to the BS has been evaluated. By separating the antennas largely enough without using beamforming algorithms, the BSs can successfully estimate the corresponding CSIs between the antennas. This is illustrated in Fig. 4, where the estimated CSI between BS1 and user 1 is represented by the real and image parts as h_{11} _real and h_{11} _imag, and the other parameters are following the same notation method. During the experiment, both users can achieve a spectrum efficiency above 0.629 bps/Hz, which is expected for the minimal system implementation with a low bandwidth of 200 kHz and BPSK modulation schemes.



Fig. 4. The results for the initial testbed implementation (A scaled view of the screen in Fig. 3).

IV. CONCLUSIONS AND FUTURE WORKS

In this extended abstract, we have presented our latest progress on the FPGA-based cell-less testbed development. Initial results have demonstrated that the designed baseband modules can be implemented using FPGA resource onboard a BS (e.g. USRP N321). In the implemented testbed, the baseband modules contain the essential modules for a minimum link layer communication system, which provides the key framework for further improvement, including the integration of advanced signal processing algorithms such as beamforming algorithms. In future steps, both traditional beamforming algorithms (e.g. zero-forcing) and AI-based beamforming algorithms will be integrated with the implemented baseband modules. A lab-scale testbed will be implemented for proof-ofconcept studies, e.g. to evaluate the end-user performance gain (e.g. throughput) of AI-based beamforming algorithm over its traditional counterparts.

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