Integrated Bi-Directional SiC MOSFET Power Switches for Efficient, Power Dense and Reliable Matrix Converter Assembly

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***Abstract*— This paper presents an innovative device packaging and system integration approach aimed at optimizing the electro-thermal, electro-magnetic and thermo-mechanical performance of the switches in a power converter. In particular, the focus is on state-of-the-art commercially available silicon-carbide (SiC) power MOSFETs used within a matrix converter topology. The improvements at switch level over conventional packaging and integration solutions translate into higher efficiency, power density (in terms of volume and weight) and reliability at system level. In view of typical application domains (e.g., renewable energies, solid-state transformation, smart grids, electric transport), requiring harsh environment withstand capability with high reliability and availability levels, an AC-to-AC matrix converter is chosen as a particularly relevant case study. The paper also addresses two aspects of growing relevance: reliable manufacturability and preventive maintenance compatible modular system assembly for reduced impact of single component failure on system availability.**

Keywords—Wide Band-Gap power Devices, SiC Power MOSFETs, matrix converters, integration.

I. INTRODUCTION

Efficiency, power density and reliability are main drivers of power electronics technology evolution. The conjunct improvement of these figures-of-merit is a challenging undertaking, due to the conflicting technological requirements underlying the optimization of each of them. The advent of wide-band-gap (WBG) semiconductors (e.g., silicon carbide SiC; gallium nitride, GaN) is enabling significant steps towards that aim. Nevertheless, bespoke packaging and integration solutions are crucial to ensure that the superior features of the device technology can be taken full advantage of.

Building upon previous work done on silicon transistors (IGBTs) and diodes [1], this contribution delivers an innovative solution tailored to the characteristics of SiC MOSFETs: in view of substantially different functional and structural features between the two device types, an original design is presented to maximize the benefit that can be drawn from the integration exercise. The design is validated and optimized in terms of materials selection, geometry, sizes and cooling solutions by means of computer aided analysis. A prototype of the integrated bi-directional switch is presented, along with a 3-to-1 phase matrix converter assembly and preliminary results of technology validation and lifetime assessment.

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II. INTEGRATED BI-DIRECTIONAL SIC MOSFET SWITCHES

AC-to-AC power conversion requires switches that enable bi-directional (BD) current flow between the power source and the load, while blocking voltage of either polarity. If MOSFETs are used, then a typical BD switch (BDS) is as shown in Fig. 1: the drain terminal of each transistor (D1 and D2) is the only power terminal to the outside world, with current flowing in and out of it during operation, whereas the gates (G1 and G2) and common source (S) terminals are to be made externally accessible for driving purposes only. The common source connection simplifies gate-driver design and operation. If required by the switching scheme, current flow can also rely on the MOSFET intrinsic body-diode during some operational instants.

In view of its intended operation, an optimum integration solution for this architecture is illustrated with the help of Fig. 2: the two transistor chips are mounted backside down (drain terminal) onto two separate, but identical direct bonded copper

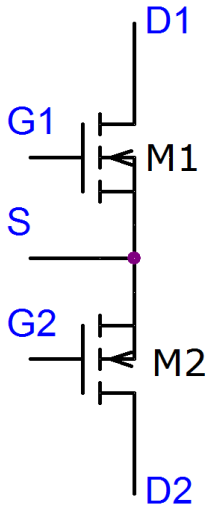


Fig. 1. Schematic of a bi-directional power switch using MOSFETs in common *source* connection. D_1 and D_2 are power terminals; $G_{1,2}$ and S are only used for driving purposes.

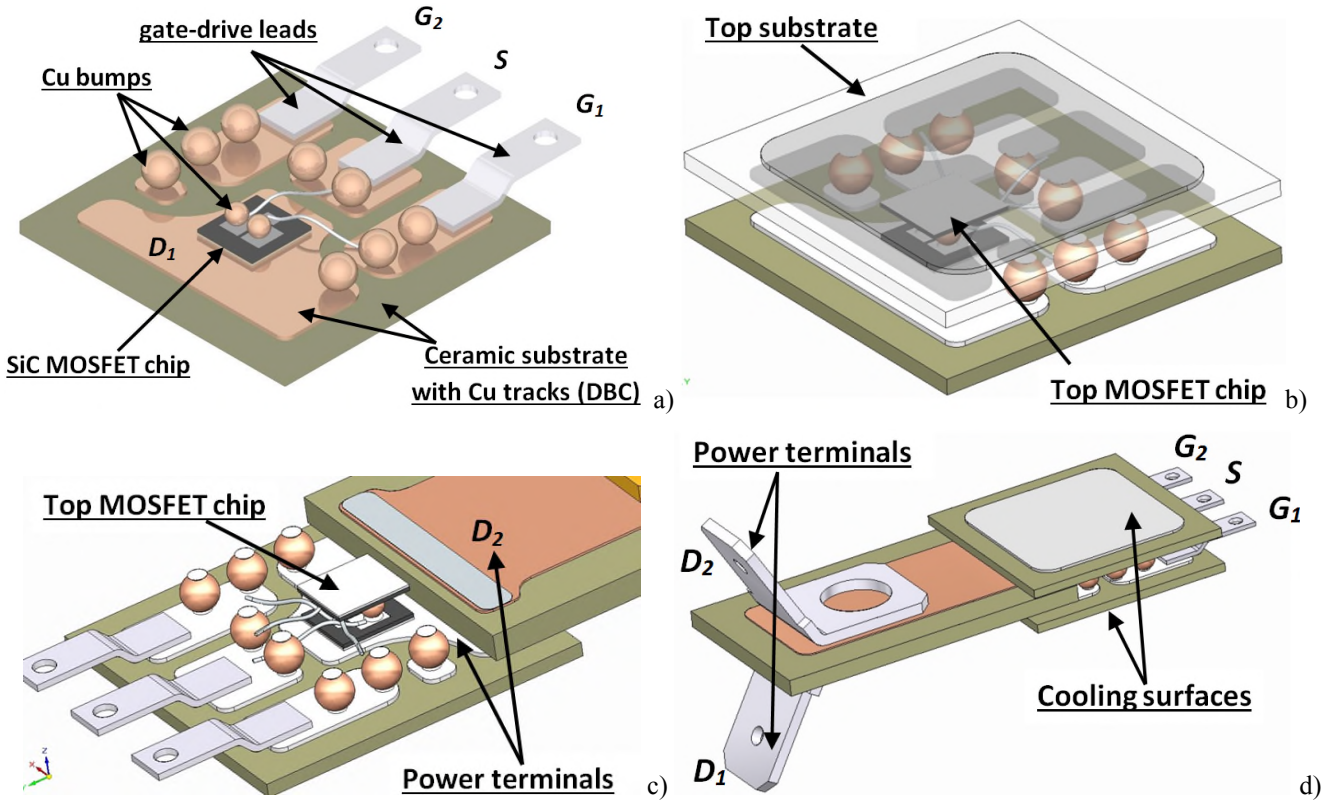


Fig. 2. In a), SiC MOSFET chip M_1 mounted on ceramic substrate. The chip side dimensions are 3.10 x 3.36 mm; the substrate is 15 x 15 mm; in b), mounting of top-side substrate and SiC MOSFET chip M*2*; in c), interconnection of third intermediate substrate for power terminals; in d), fully assembled power switch design.

(DBC) substrates (Fig. 2 a)); one substrate is flip-mounted on top of the other by means of soldered copper (Cu) bumps (Fig. 2 b)); smaller bumps are used on the SiC chips top-side to implement the current conducting interconnection of the source terminals for between the two transistors (Fig. 2 b) and c)); a dedicated additional DBC substrate partly sandwiched between the other two substrates is used to implement the power terminals D1 and D2, whereas, for simplicity, bond-wires and external leads are still used for the gate-drive interconnection here (Fig. 2 c) and d). Fig. 3 shows a cross-sectional view of the integrated BDS with details of the power and drive interconnects. For reference, the devices used in this study are

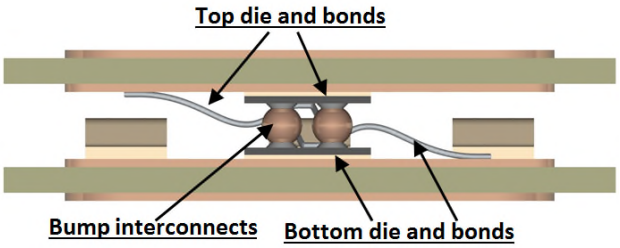


Fig. 3. Cross-sectional view of the BDS assembly with details of the internal interconnections.

1200 V – 80 mΩ MOSFETs, with dimensions of 3.1 x 3.6 mm^2 and about 200 µm thickness [2].

It is worth pointing out that the devised assembly solution is compatible with an automated process, which could run, for instance, according to the sequence:

1) dies soldered on substrates (use of solder foil and masks);

2) wirebonding;

3) all bumps and gate-source drive terminals soldered on one substrate (use of solder paste);

4) die carrying substrates and intermediate power terminals substrate soldered;

5) insulation (gel filling) and terminals interconnections.

Also, the center power terminal carrier does not need to be a ceramic substrate and could instead be some kind of printed circuit board (PCB) of suitable thickness and material, able to withstand the temperature values involved in the assembly process.

III. Thermal Analaysis for Design Optimisation

The two SiC MOSFETs are the heat generating elements during operation. Heat can be evacuated from the devices via

the backside connection to the DBC Cu track and by means of the Cu bumps on their top surface. The DBCs consist of two

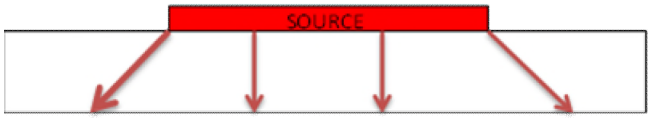


Fig. 4. Illustration of heat-spread assumption for analytical calculations.

Cu layers and one ceramic layer (typically, aluminum nitride, AlN, or silicon nitride, SiN). Although not shown here explicitly, the rest of the space between the two DBCs has to be filled with a gel (e.g., Silgel 616), to ensure both dielectric insulation and voltage withstand capability and protection from environmental pollution and corrosion: the insulating gel is typically a very poor thermal conductor.

Each component in the assembly is characterized by a given value of thermal conductivity, size and geometry, making the accurate characterization of the switch thermal performance non-trivial. In view of the aspect ratios and relative sizes of the devices and the substrates and the solder layer in between them, since both devices are heat generating elements and the assembly is symmetrical relative to a plane cutting the middle of the bumps (see Fig. 3), as a first order approximation for the stationary time domain it can be assumed that heat spread through the DBCs is as illustrated in Fig. 4, where the heat-spread angle is approximately 40°. With this configuration, the thermal resistance of the switch can be calculated as

$$R_{th} = \frac{1}{2.\lambda.(b-a)}.\ln\left[\frac{b}{a}.\left(\frac{a+2.e.\tan(\alpha)}{b+2.e.\tan(\alpha)}\right)\right] \quad (1)$$

with λ the thermal conductivity (W/m.°C), b and a are the lateral dimensions of the heat source ($b>a$), e the thickness of the object (m). The thermal resistances of all intervening layers are calculated with Eq. (1) for each material in the heat-flow path: the surface of the thermal source is calculated at each interface, as indeed it's not the same because of the propagation cone. Forced convection (liquid cooling) heat-transfer boundary conditions are assumed. At first, water is used as cooling fluid with a speed of 5 m/s and so we obtain a Reynolds number less than 500000, indicative of laminar flow. Thus, the relation can be used for the Nusselt number, where Re and Pr are the Reynolds and Prandtl numbers, respectively:

$$Nu = \frac{2}{3}Re^{0.5}.Pr^{0.33} \quad (2)$$

$$Re = \frac{\rho.v.l}{\mu} \quad (3)$$

$$Pr = \frac{\mu.C_p}{\lambda} \quad (4)$$

with μ the dynamic viscosity of the fluid (Pa.s), C_p the specific heat of the fluid (J/kg.°C), λ the thermal conductivity of the fluid (W/m.°C), ρ the density of the fluid (kg/m^3), v the speed of the fluid (m/s), l the length of the plate (m) (the last value calculate for the thermal source) and h the convection coefficient (W/m^2.°C). Then, the convection coefficient can be extracted from

$$Nu = \frac{h.l}{\lambda} \quad (5)$$

With this thermal resistance (conduction and convection) the theoretical die temperature is calculated as

$$P = \frac{T_{die} - T_f}{R_{th}} \quad (6)$$

with P the power produced by the die, T_{die} the die temperature (°C), T_f the fluid temperature (°C) and R_{th} the thermal resistance (K/W).

The theoretically estimated die temperature for the switch being too high, the design was further developed to include a small finned heat-sink soldered on top of each DBC. A parametric study was carried out to optimize the design, assuming a fluid temperature of 20°C and a power dissipation of 100W per transistor. Fig. 5 gives some results of the

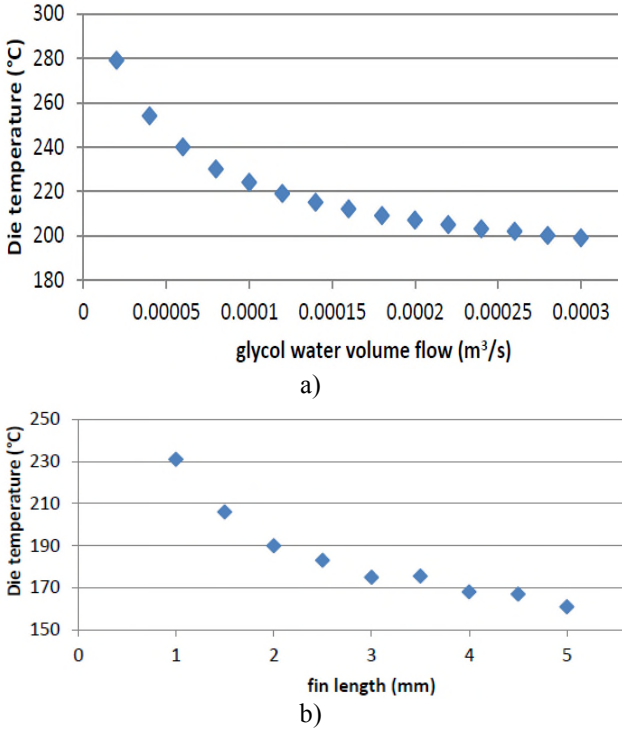


Fig. 5. : Die temperature as a function of the glycol water volume flow, a); and of the heat-sink fin length, b).

estimated max temperature within the assembly (surface of the transistors) as a function of cooling liquid flow-rate and heat-sink fin-length. By intervening on solder layers and ceramic substrate thickness and by defining proper heat-sink characteristics, the maximum temperature was contained well within the device nominal rating (175 ºC), as verified with the help of 3D thermal simulations, illustrated by the results presented in Fig. 6.

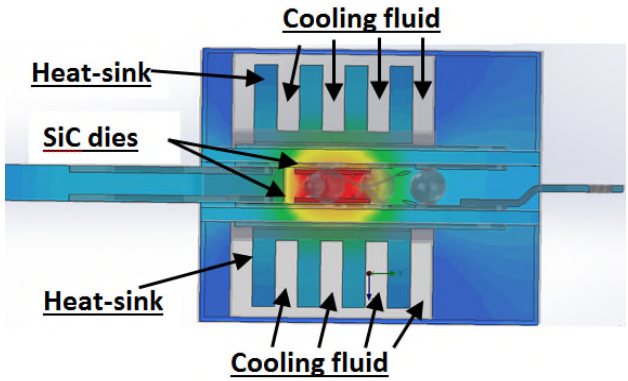


Fig. 6. Simulated temperature distribution within the integrated power switch with the advanced design option incorporating thermal management.

As a result of the simulation study, in the final design the DBCs are 15 x 15 mm^2 and were implemented using 0.6 mm thick AlN ceramic with 0.2 mm thick Cu tracks. The size of the heatsink was chosen as a function of the thermal source surfaces calculated previously and finally set to 5 x 7 mm^2 with a top layer thickness 0.5 mm and with 4 fins spaced 1 mm, 1 mm wide and 2 mm high. The heat-sink is soldered in correspondence of the chip location on the underlying face of the substrate. The mechanical framework is implemented by the liquid cooler, constructed from a polymer in such a way as to enable easy thermal interconnection of multiple switches to form a system. The idea is illustrated in Fig. 7 a) for a single switch. Three such bricks can be easily interconnected by means of gaskets and screws and two additional plastic pieces (detailed in the next section) to build up a liquid cooled 3-to-1 phase matrix converter module. A thermal simulation of the whole system confirmed the ability to operate under safe temperature values, as can be seen in the results of Fig. 8. The estimated temperature gradient of the cooling liquid between inlet and outlet of the cooler was about 3 K when a flow rate of 15.10^{-5} m^3/s.

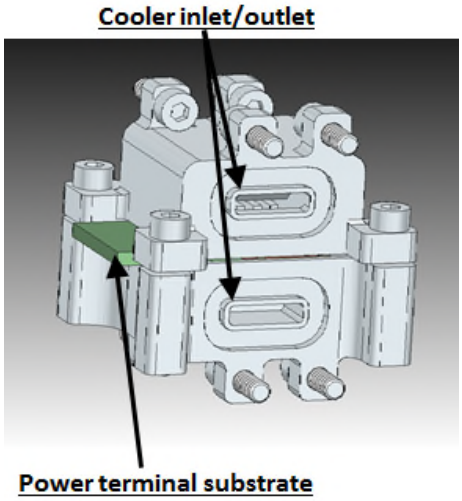


Fig. 7. Cooler design for a single switch.

IV. Hardware Prototype

Fig. 9 shows some parts of the hardware prototype, described in the caption to the figure. The switches are insulated with dielectric gel. A gasket enables modular and re-openable system assembly simply via additional joining elements. The cooler design is also modular, so that assembly of a matrix converter block is achieved by combining a given number of elementary bricks. All elements of the structure are shown in Fig. 10: one joining element enables interconnection of two basic bricks as per Fig. 7; a second joining element, featuring a threaded cavity for mounting of the liquid fluid circulating pipes, enables connection to the temperature regulating unit. The final system level assembly is shown in Fig. 11: The phases are later terminated with soldered pins and interconnected by a dedicated bus-bar PCB, where the input filter passive components can also be mounted. The structure can be easily dismounted to replace a single brick in case of failure.

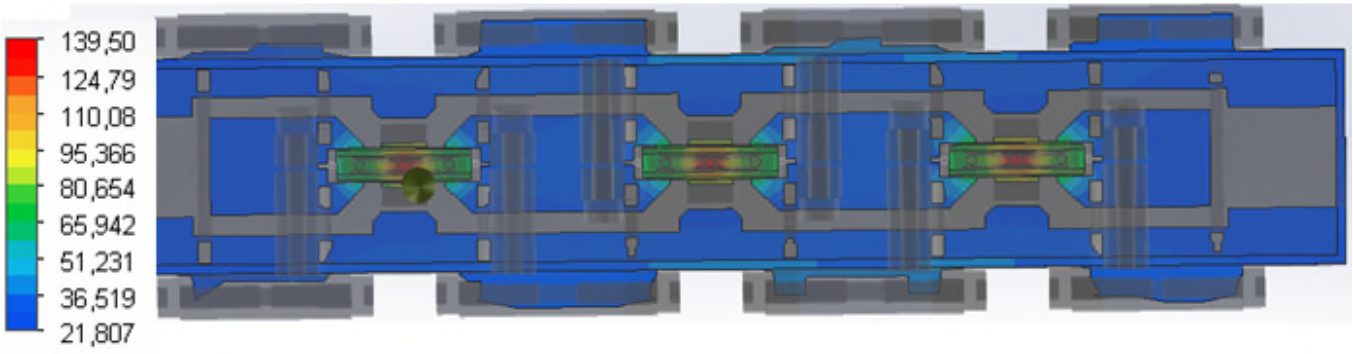
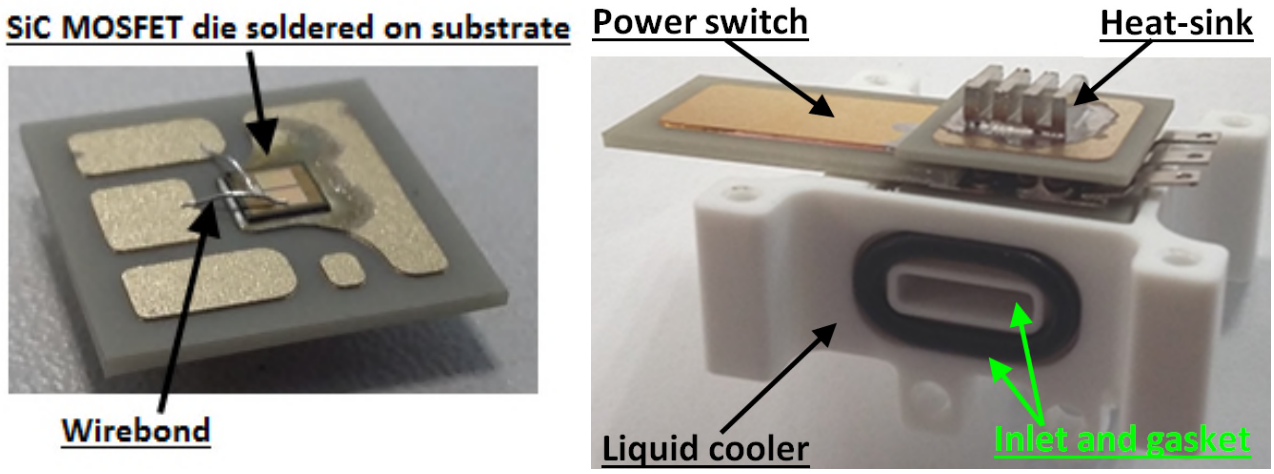


Fig. 8. Thermal simulation of the whole 3-to-1 phase matrix converter module.



a) b)

Fig. 9. In a), SiC MOSFET chip soldered onto ceramic substrate, with gate and source wire-bonded; in b), fully assembled power switch sitting on half of liquid cooler.

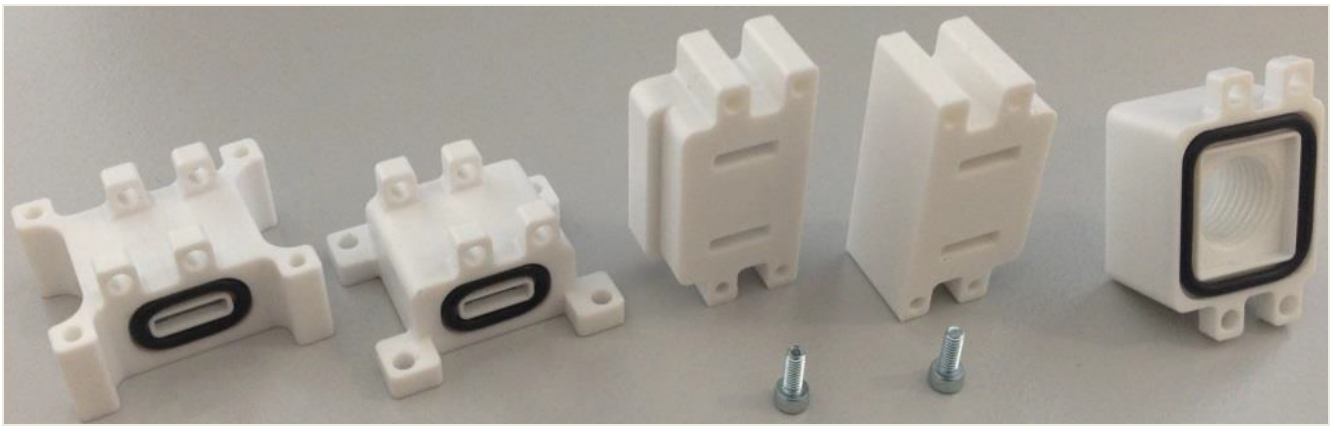


Fig. 10. Components of the liquid cooler unit.

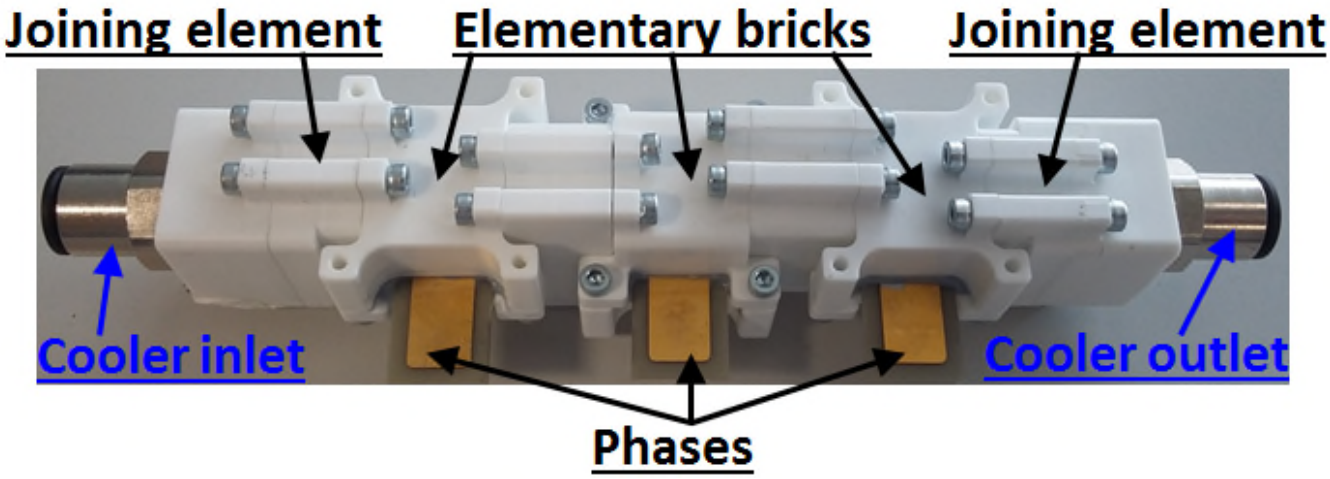


Fig. 11. Modular converter assembly (3-to-1 phases).

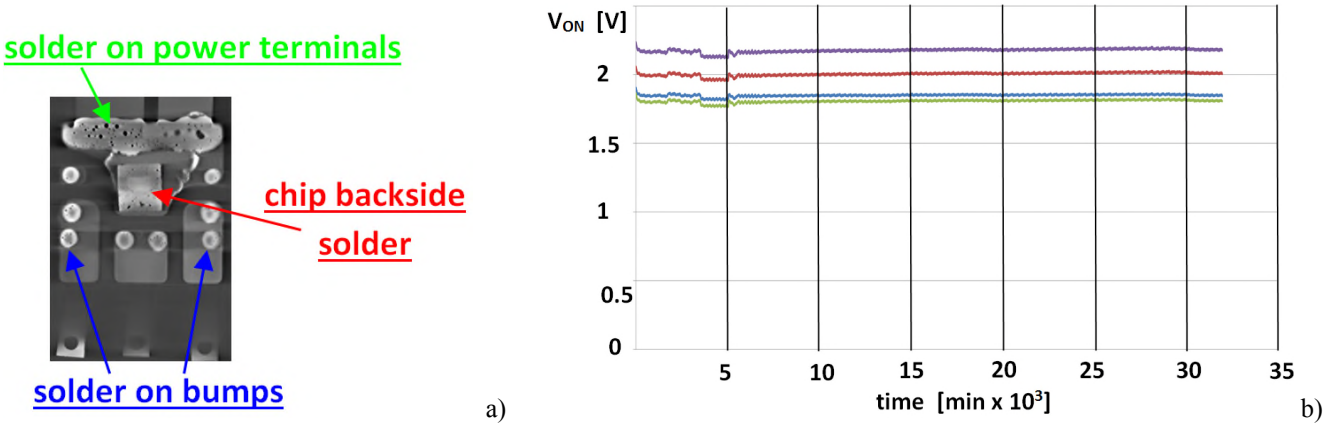


Fig. 12. In a), X-ray tomography of switch after power cycling highlighting solder degradation at critical locations for built-in reliability design optimization; in b), monitoring of V_{ON} as an indicator of degradation against thermal cycling.

Preliminary technology validation tests have been run and confirm the viability of the proposed solution [3]. Active and passive power cycling at single switch level were carried out and non-destructive x-ray tomography, of the kind shown in Fig. 12 a), was used to assess the level of degradation at different times during cycling and achieve an iterative optimization of the assembly process. Latest results of temperature controlled prolonged cycling, reported in Fig. 12 b), indicate no failure after 500 hours: the thermal cycle goes from of -55 to 150 ºC in 15 minutes, both during cooling and heating, and comprises of 30 minutes at temperature at both ends of the scale. The transistor on-state voltage is sued as a monitor of degradation.

V. Conclusion

This paper has presented an innovative integration scheme of SiC power MOSFETs to create highly integrated bi-directional power switches, used to assemble a 3-to-1 phase matrix converter cell. The approach aims to progress beyond state-of-the-art in power converter design and construction, by improving power density (including both volume and weight), performance and reliability, at the same time bringing along modularity for improved system level availability and reduced impact of failure on maintenance and repairing costs. The proposed assembly approach is compatible with automated processes.

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