UIS failure mechanism of SiC power MOSFETs

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***Abstract*—This paper investigates the failure mechanism of SiC power MOSFETs during avalanche breakdown under unclamped inductive switching (UIS) test regime. Switches deployed within motor drive applications could experience undesired avalanche breakdown events. Therefore, avalanche ruggedness is an important feature of power devices enabling snubber-less converter design and is also a desired feature in certain applications such as automotive. It is essential to thoroughly characterize SiC power MOSFETs for better understanding of their robustness and more importantly of their corresponding underling physical mechanisms responsible for failure in order to inform device design and technology evolution. Experimental results during UIS at failure and 2D TCAD simulation results are presented in this study.**

Keywords—Silicon carbide; MOSFET; Avalanche breakdown; Avalanche ruggedness; Unclamped inductive switching

I. INTRODUCTION

Silicon carbide (SiC) power MOEFETs offer impeccable device features for power electronics applications. As compared to Silicon (Si), features such as faster switching speeds, lower on-state losses, lower off-state leakage currents, higher power density per unit area, higher thermal conductivity and smaller die sizes are some of the exciting benefits of SiC which could not be realized using the existing Si device technology [1, 2]. SiC power MOSFETs are relatively newer in device manufacturing technology than its well established Si counterparts. They require extensive characterization comprising of experiments and advanced TCAD simulations assessing their robustness under different unintended test conditions such as UIS (Unclamped inductive switching) and SC (short circuit) for better in-depth understanding into physics of failure mechanism and to facilitate future device technology advancements.

Under UIS, the failure of Si power MOSFETs is linked to the activation of parasitic bipolar junction transistor (BJT) [3]. Fig. 1 illustrates the structure of a power MOSFET. The V_{BE} of parasitic NPN BJT for Si is around 0.6-0.7V which decreases with temperature at a rate of 2mV/K and on the other hand, the base resistance (R_B) of the p-well increases with temperature [4]. For parasitic BJT activation, the voltage across both ends of R_B of the p-well, should be higher than the built-in

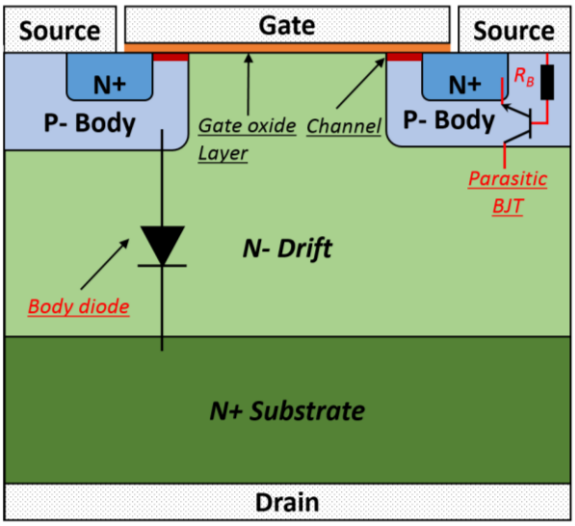


Fig. 1: Power MOSFET structure

voltage of the base-emitter junction. Indeed, evolution of Si MOSFET design has targeted substantially the improvement of the parasitic BJT structure to enhance robustness against activation. However, it is expected that the wide bandgap and low intrinsic carrier concentration of SiC makes it very unlikely for the intrinsic BJT to be activated during typical UIS events (i.e. with typical values of switched currents and ensuing temperature evolution). Not only that, the built-in voltage at the base-emitter junction in SiC is also higher (around ~ 2-3V) than in Si [5].

II. SILICON CARBIDE MOSFET AVALANCHE RUGGEDNESS AND ANALYSIS METHODOLOGY

Avalanche ruggedness is a useful feature of power devices. Ability of power devices to dissipate energy during avalanche breakdown results in convertor designs without snubbers. Also, systems such as engine control units (ECUs) and anti-lock braking systems in automotive applications require power devices to dissipate more consistent overload transient energy release from inductive loads, typically motors and actuator controlled solenoids. Previous publications have shown that commercially available SiC MOSFETs exhibit

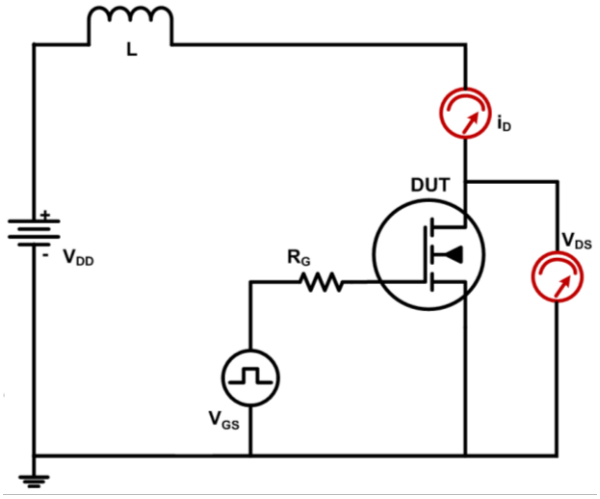


Fig. 2: UIS test circuit schematic

significant intrinsic avalanche ruggedness and could dissipate avalanche energy (E_{AV}) above 1 J, depending on the test conditions [6 – 8].

UIS test circuit, as illustrated in Fig. 2, is widely used for assessment of avalanche ruggedness of power devices. Here, the device under test (DUT) is turned ON using a single gate pulse (t_{ON}) to ramp up the inductor current to the desired value. When the device turns OFF, the device enters avalanche breakdown since current in the inductor cannot immediately go to zero due to the current continuity condition. Parameters such as t_{ON}, L and V_{DD} are normally altered to move outside of the device's safe operating area (SOA) until failure is obtained during avalanche breakdown. The self-heating of the DUT during t_{ON} was simulated and was found to be significantly lower than the temperature levels experienced during avalanche breakdown; therefore, the self-heating of the device is considered here to be negligible.

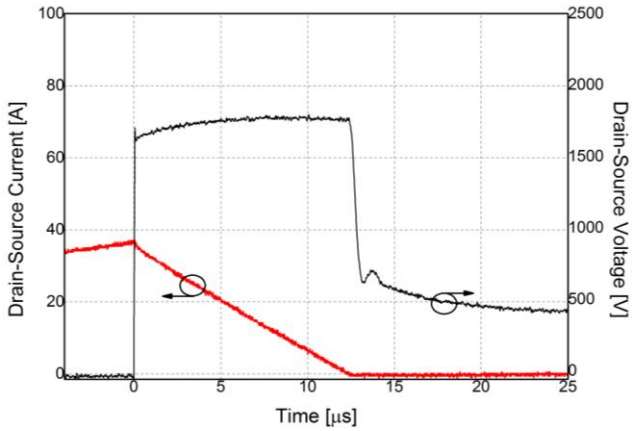
In order to get more insight into device internal phenomena and the actual failure mechanism during avalanche breakdown, here, experimental results showing failure were reproduced with the aid of 2D TCAD physical simulations. UIS measures were also performed on bare dies where thermal imaging using infrared IR camera was performed to obtain the temperature distribution of the DUT's surface.

III. Experimental Results

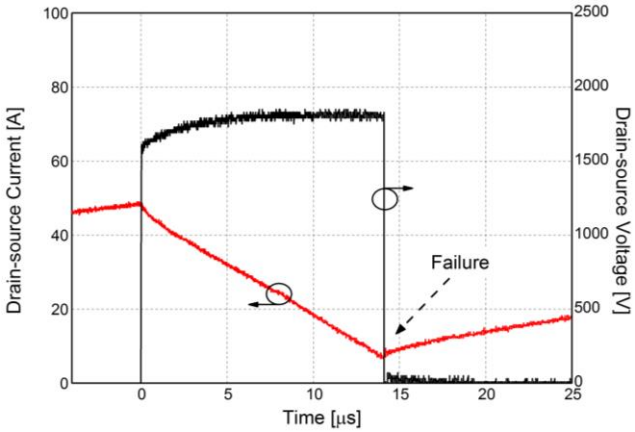
Experimental results showing drain current (I_D) and voltage (V_{DS}) for UIS test for discrete second generation 1.2kV 36A SiC power MOSFET manufactured by CREE [9] are shown in Fig. 3.

For test condition without failure, Fig. 3(a), the inductor current goes to zero as the avalanche time is lapsed and the drain source voltage goes to V_{DD}; therefore, the device still withstands voltage and is hence functional. The peak current (I_0) and time in avalanche (t_{AV}) was increased to dissipate higher

$$E_{AV} = \frac{1}{2} I_0 V_{BD(eff)} t_{AV} \quad (1)$$



(a)



(b)

Fig. 3: Experimental UIS I_D and V_{DS} failure waveforms; (a) – Before failure; (b) – At failure; V_{DD} = 400V; T_{CASE} = 25˚C; L = 500µH;

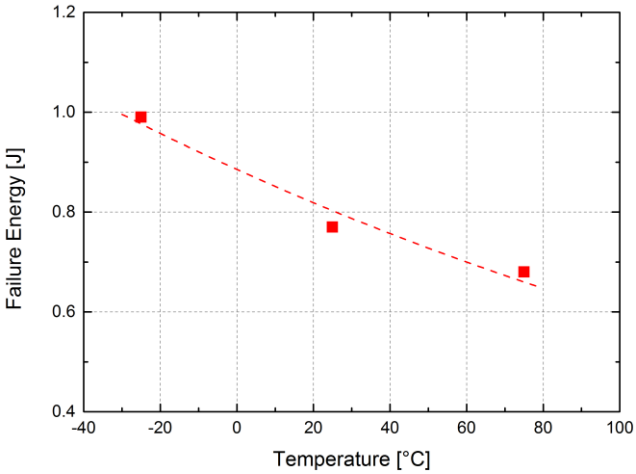


Fig. 4: Critical E_{AV} versus temperature (T_{CASE}) [10]

avalanche energy (E_{AV}) and thus moving out of the safe operating area (SOA) until failure was obtained as reported in Fig. 3(b). At failure, a short was observed between all three terminals of the MOSFET (gate, drain and source) as the voltage comes down sharply and the current starts to increase again linearly as dictated by the inductor alone. Equation (1) dictates the energy dissipated during avalanche breakdown (E_{AV}). The critical avalanche energy ($E_{AV\_CRITICAL}$) versus case temperature (T_{CASE}) has been plotted in Fig. 4 and it clearly indicates that the critical E_{AV} decreases for higher T_{CASE}. Several previous studies have presented the relationship between different I_0 and t_{AV} values for UIS test on SiC power MOSFETs with an aim to determine the critical E_{AV} as well as the SOA boundary conditions [10, 11].

IV. TCAD SIMULATIONS

TCAD Synopsys Suite was used to investigate the insight physics of the device at failure and give interpretation of experimental results. Fig. 5 shows the full planar cell structure which was used to perform 2D electro-thermal device simulations. Cell bulk doping was carefully chosen (N_{DRIFT} = 9 x 10^{15} cm^{-3}) to obtain breakdown voltage (V_{BD}) close to the experimental value (V_{BD} ~ 1900V) as shown in Fig. 3. The P-body and the N+ source terminals of the simulated device structure were separated (both terminals set to same bias voltage of 0V). Relevant physical models representing interface traps and degradation of mobility were also included into the simulation.

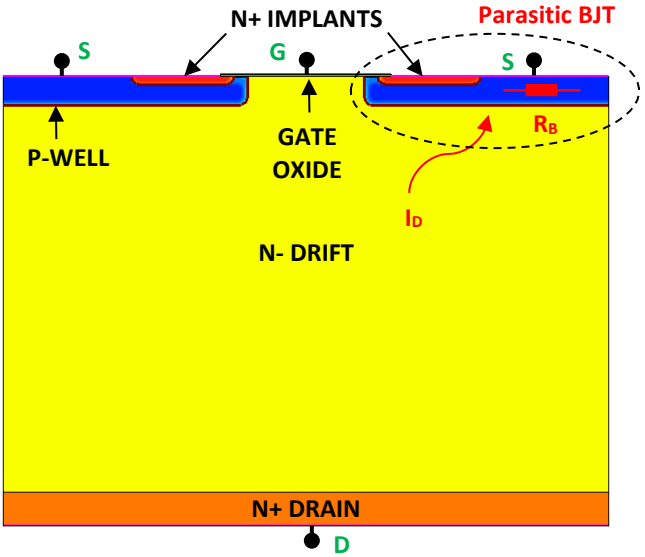


Fig. 5: TCAD MOSFET full cell structure (Not to scale)

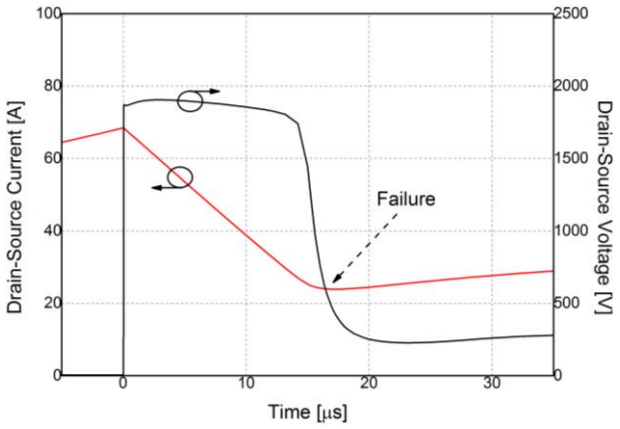


Fig. 6: Simulated UIS I_D and V_{DS} failure waveforms; V_{DD} = 400V; T_{CASE} = 25°C; L = 500µH;

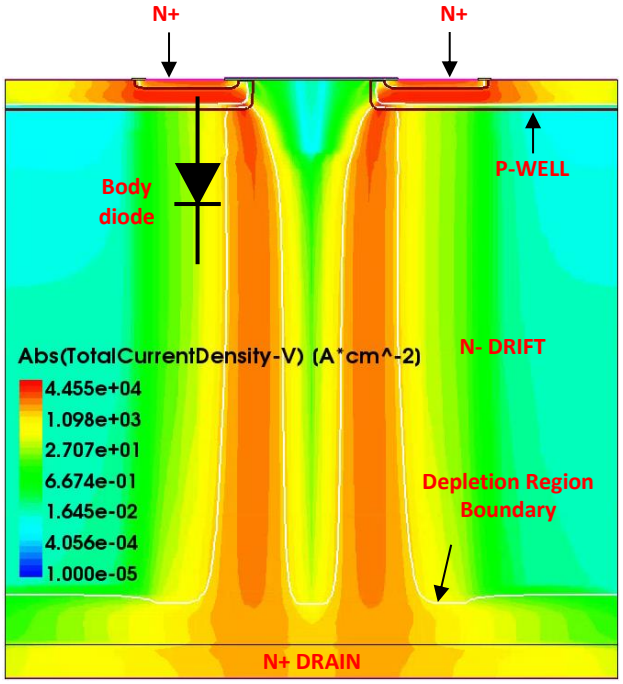


Fig. 7: Total Current Density during avalanche breakdown (Far away from failure)

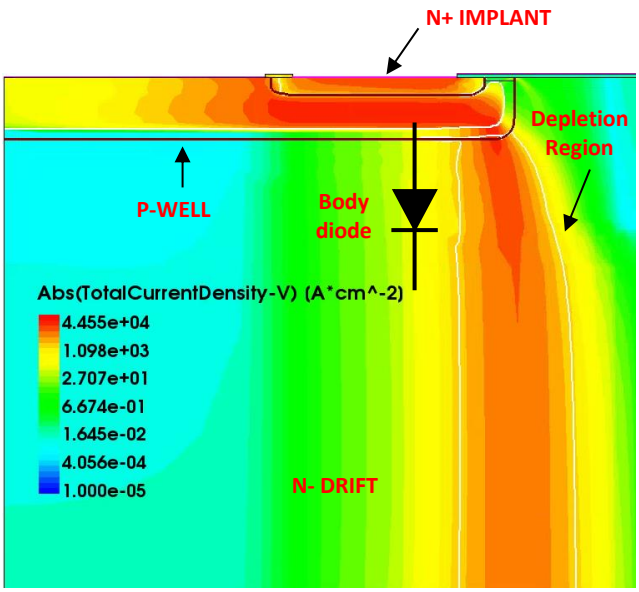


Fig. 8: Total Current Density; (Zoomed in view of Fig. 7)

Fig. 6 shows mixed mode TCAD simulation results showing drain current (I_D) and voltage (V_{DS}) at failure. The total current density distribution within the cell immediately after device enters breakdown is shown in Fig. 7. During avalanche breakdown, the current flows through the intrinsic body diode and the base resistance (R_B). Since the electrical field during avalanche breakdown is maximum at the edge of the p-well / n-drift, the current is therefore saturated close to the edge of the pn junction as could be seen in Fig. 7 and Fig. 8. As a result of that, the lattice temperature of the device close to the edge of the pn junction increases rapidly to really high values, raising well above 1000K, as the failure intervenes.

It was observed that as the device temperature increases, current starts flowing in the channel and in the p-well region immediately underneath the channel (Fig. 9) indicating a concurrent decrease of threshold voltage (V_{TH}) and an increase of the device leakage current due to such elevated temperatures. This results in a thermally unstable operational condition characterized by rapid thermal runaway. Indeed, even if channel is activated, bias conditions correspond to a thermally unstable region of operation, characterized by increasing I_D with temperature [12]. The inability of the device to further withstand voltage after failure is also confirmed as the depletion region shrinks in Fig. 9 suggesting that the device would be no more functional and therefore classed as failed.

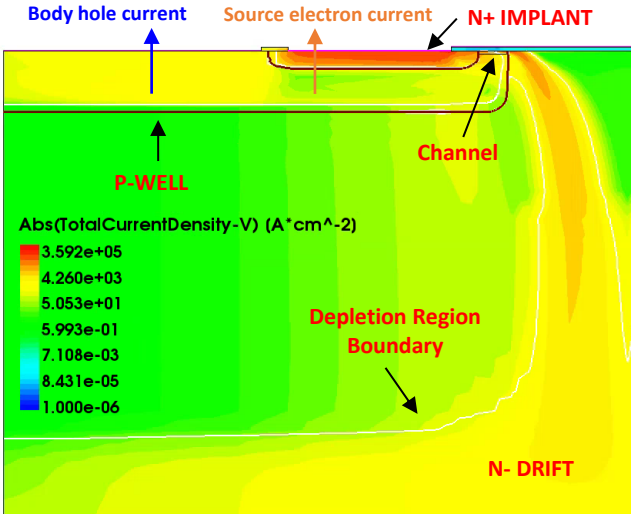


Fig. 9: Total Current Density; (Zoomed in – After failure)

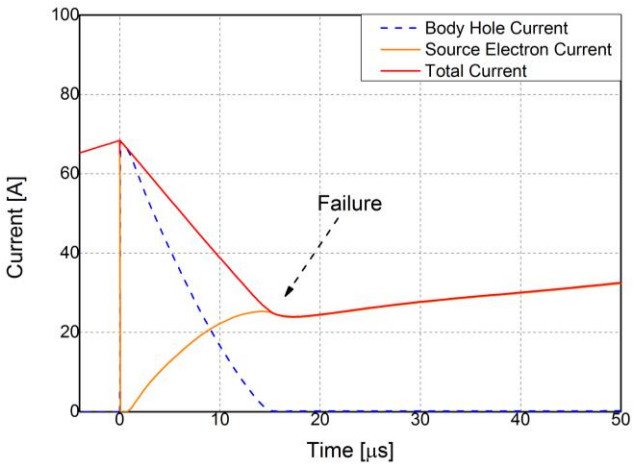


Fig. 10: Different current components

The electron and hole current components of the device's total drain-source current are shown in Fig. 10. The source electron current due to majority carriers (orange solid line) is the main current component when the device is ON (channel is activated) to ramp up the inductor current. The source electron current component ideally should be negligible during avalanche breakdown as the device is no more in the ON-state. During avalanche breakdown, holes (dotted blue line) and electrons (red solid line) flow out of p-body and n+ drain terminals respectively as the body diode of a power MOSFET is eventually a PiN diode. But due to reported elevated device lattice temperature in excess of 1000K during avalanche breakdown, V_{TH} significantly decreases below zero which results in activation of the channel (increase of source electron current) as well as increase of the drain leakage current underneath the channel leading to thermal runaway and eventually causing device failure as can be better understood from Fig. 9 and Fig. 10.

V. THERMAL MAPPING

To complement the experimental results and the TCAD simulation results, infrared thermal mapping system (as described in [13]) was used to acquire temperature distribution of bare die devices during UIS tests. A localized hot-spot formation due to current crowding over a small number of cells within the total active area of the device was observed as shown in Fig. 11. Thermal map reports temperature normalized to the

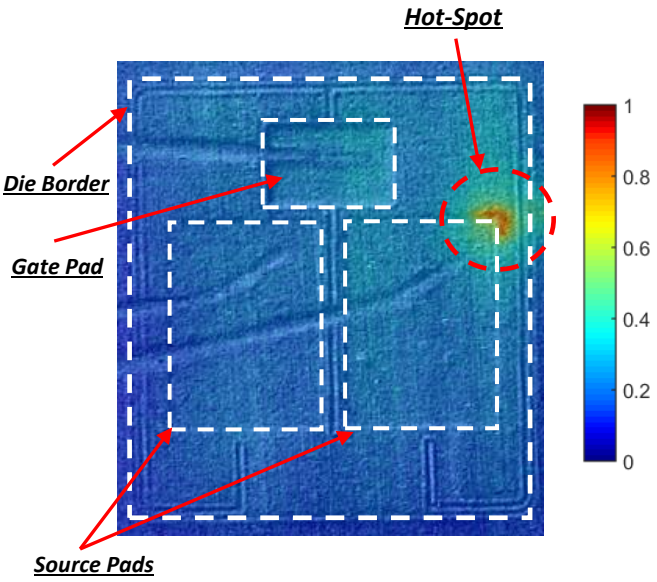


Fig. 11: Hot-spot formation during UIS on bare die device (Normalized); V_{DD} = 400V; T_{CASE} = 75˚C

calibration range of camera. Equation (2) was used for temperature normalization during post processing of the thermal map where T_{max} is the maximum measured temperature of the thermal map and T_{REF} is the DUT's case temperature. During failure, estimated surface temperature during avalanche breakdown were well in excess of 500°C. The topographic image of the bare die was superimposed onto the thermal map to clearly show the bare die device boundary.

$$T_n = \frac{T - T_{REF}}{T_{\max} - T_{REF}} \quad (2)$$

Further TCAD simulations are required with more cells in parallel in order to investigate the role of device design parameter mismatch in enhancing the occurrence of hot-spots and thermal runaway with highly localized current crowding phenomena. It is really important to ensure uniformities among all cells in the device to avoid weak spots inside the device. By doing this, nonlinearities between cells are kept minimal thus ensuring that the failure occurs randomly in the device's active area [14].

VI. CONCLUSION

UIS tests were performed on commercial SiC power MOSFET to assess their avalanche ruggedness. Failure obtained in UIS were reproduced using 2D TCAD electro-thermal simulations showing the physics leading to failure due to a significant decrease in the threshold voltage (V_{TH}) and increase in the drain leakage current leading to flow of electron current into the source terminal during avalanche breakdown. Thermal imaging of bare die devices under UIS conditions were also performed and a localized hot-spot due to focalization of current in a small area was observed on the device during failure. It is also needed that investigations assessing device's avalanche breakdown capability should be coupled with body diode forward voltage stability [15] to give a better understanding and characterization of the body diode feature of SiC power MOSFETs.

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