Developing Power Semiconductor Device Model for Virtual Prototyping of Power Electronics Systems

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***Abstract*—Virtual prototyping (VP) is very important for power electronics systems design. A virtual prototyping design tool based on different modelling technology and model order reduction is proposed in the paper. In order to combine circuit electromagnetic model with power semiconductor device models, a SiC-JFET behavioural model is presented and implemented in the design tool. A half bridge circuit using SiC-JFET devices is thus represented in the VP software. The presented SiC-JFET behavioural model is then validated by comparing with experimental measurements on switching waveforms.**

***Keywords*—Virtual prototyping; Model order reduction; Power semiconductor device modelling; Behavioural model; Switching waveforms**

I. Introduction

Power electronics systems are essential in the drivetrain of hybrid and electrical vehicles. Optimising the design of these systems is important in increasing performance, such as reducing overall drivetrain weight and size, improving efficiency so as to increase range, and ensuring a robust and reliable drivetrain [1].

Optimising system design through the construction and testing of physical prototypes can be time-consuming and expensive. Thus, virtual prototyping (VP) techniques offer one solution to eliminate the requirement for construction and testing of physical prototypes, which could reduce design time and costs so as to realize highly optimised system designs. A key requirement for VP is the ability to predict the performance of a design by using only simulation, which could help designers to obtain reliable results in a quick way.

Thermal design and electromagnetic compatibility design are very important for power electronics systems used in electrical vehicles, in which automotive drivetrain could reach more than 100kW power rating. At one side, even at system efficiencies greater than 95%, the large quantities of waste heat produced require an efficient thermal design. Thus, it is necessary that power devices (passive and active) losses and heat path from each heat source to the cooling equipment could be accurately and fast simulated in order to evaluate system thermal performance. At another side, the switching nature of the power semiconductor devices introduce high dI/dt and dV/dt which necessitates careful consideration in terms of electromagnetic performance. Thus, it is necessary that both electromagnetic interference (EMI) source and its propagation loop could be well represented, so power semiconductor device dI/dt, dV/dt transition and parasitic elements shall be accurately and efficiently simulated. Moreover, the fast time-constants (nanoseconds) associated with the power semiconductor devices, slow time-constants (minutes) associated with thermal effects, and requirement for 3D modelling of the system design, mean that novel, efficient simulation techniques and design tools are required to avoid excessively long simulation times.

Developing a VP design tool which can predict the above performance could help designers to previously validate their prototype prior to experimental measurements. A VP design tool has been proposed by authors in [2], [3], where power electronics system thermal performance has been validated. However, accurate modelling of the power semiconductor device was found to be a limitation in the above papers. Thus, in this work, it will be presented that how efficient behavioural semiconductor models can be when they are combined with model order reduction techniques for 3D system simulation to allow rapid virtual prototyping of power electronic systems.

The paper is structured with following parts. At first, modelling techniques of the proposed VP design tool for power electronics systems will be reviewed. Then, power semiconductor device behavioural model will be presented. Afterwards, a half bridge circuit using SiC-JFET is represented by the VP design tool. Simulation results and experimental measurements of device switching current and voltage are compared, which is followed by the conclusion.

II. Modelling techniques of Virtual prototyping design tool

A. Efficient Device Modelling

Different components within a power electronic system require different modelling techniques. Power semiconductor devices could be either physically modelled or behaviourally modelled. Physical model accounts for the internal structure and physical processes of the device. However, it is notoriously complex and can result in extremely slow simulation times [4]. By contrast, behavioural model represents electrical and thermal behaviour of the device, which is flexible and easy to implement in simulation tool. As power semiconductor device is usually fixed when designers use them in power electronics systems, developing their behavioural models is suitable in a VP design tool. Behavioural models could also be used to represent passive device and active device driver circuit.

Components whose physical location will influence system performance such as bus-bars, PCBs and heatsinks, cannot use simplistic behavioural models. The 3D geometry of these components influences system performance and will be changed during the system optimisation process by designers, so a simulation model capable of capturing the effect of these changes must be used. Accelerating these physical, 3D simulations is essential to allow fast simulation times, which will be presented in the next part.

B. Efficient Modelling of the 3D Design Geometry

To fully evaluate the performance of a design, numerical methods must be used to translate design details such as geometry and construction materials into an equivalent mathematical model. One most used technique is spatial discretisation (meshing) which generates a large system of Ordinary Differential Equations (ODE) by dividing the design geometry into many small sections or elements over which a solution describing the effects of interest can be written. Thus, thousands of elements, resulting in a system of thousands of ODEs, can be necessary to obtain accurate results. In the software developed, the approach based on Finite-Difference Method (FDM) is used for thermal simulation and that based on Partial Element Equivalent Circuit method (PEEC) is used for electromagnetic simulation.

In order to increase simulation speed, Model Order Reduction (MOR) techniques to reduce the number of equations generated by the discretisation is applied in the VP design tool. The principle of MOR techniques is that if a discretisation produces n ODEs, which give rise to n eigenvalues spread over the model frequency response range, the solution can in fact be accurately represented using a much smaller number of m eigenvalues. Krylov subspace project algorithms are used to find a much smaller system of m ODEs which accurately capture the original dominant eigenvalues, where m $\ll$ n. As expressed in eq. (1), the algorithm produces an $m \times n$ matrix H and its transpose H^T with orthonormal rows which can be used to link original state vectors x to its reduced order vector x_r.

$$\begin{aligned} x_\mathrm{r} &= [H]x \\ x &= [H]^T x_\mathrm{r} \end{aligned} \tag{1}$$

Thus, a reduced order system with following new equations linking the input u of size a and output y of size b of the original system could be obtained by applying eq. (1).

$$\begin{aligned} [H]M[H]^T \dot{x_\mathrm{r}} &= [H]A[H]^T x_\mathrm{r} + [H]Bu \\ y &= C[H]^T x_\mathrm{r} \end{aligned} \tag{2}$$

$$\begin{aligned} [M_\mathrm{r}]\dot{x_\mathrm{r}} &= [A_\mathrm{r}]x_\mathrm{r} + [B_\mathrm{r}]u \\ y &= [C_\mathrm{r}]x_\mathrm{r} \end{aligned} \tag{3}$$

The reduced ordered matrices M_r, A_r, B_r and C_r are $m \times m$, $m \times m$, $m \times a$ and $b \times m$ matrices, of which the size is much smaller than their original ones M $(n \times n)$, A $(n \times n)$, B $(n \times a)$ and C $(b \times n)$. Thus, only m equations need to be solved at each time-step. No spatial information is lost, as variables such as the voltage, current, temperature and heat-flux values at any node in the original model can be calculated from the reduced order states using the H^T matrix (eq. (1)). Therefore full 3D graphical analysis, at any time-step, is still possible. The volume of data required to be stored and processed for long simulations is also significantly reduced.

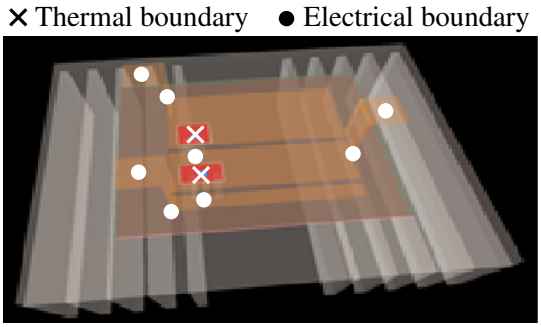


Fig. 1: Defined boundaries in geometrical model

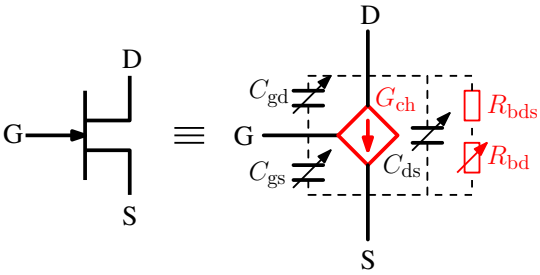


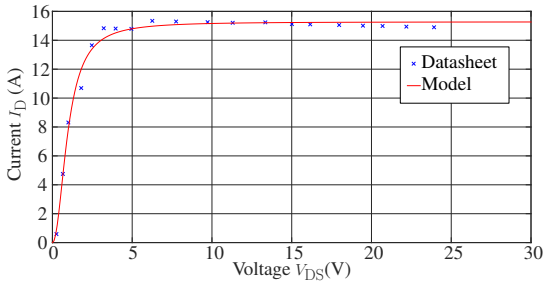
Fig. 2: Equivalent circuit of a transistor

The software applies an Arnoldi MOR algorithm [5] for thermal order reduction, and the related PRIMA [6] algorithm for electromagnetic order reduction. The accuracy of these techniques when applied to a typical power electronic simulation is shown in [3].

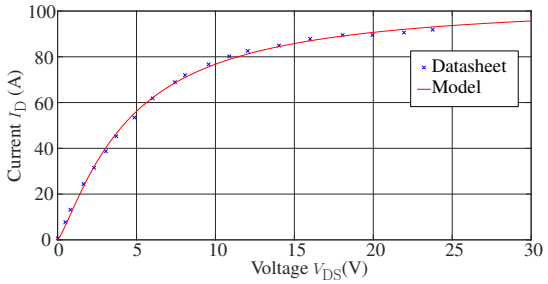
C. Coupled Physical and Behavioural Model Description

The 3D design geometry is defined in terms of building blocks such as 3D solids, along with a set of electrical and thermal boundaries. These basic building blocks can be grouped to form components such as power modules, substrate tiles, heat-sinks or bus-bars. The boundaries serve as points to which the behavioural models of the remainder of the system can be connected for design evaluation, which is shown in Fig. 1. Electrical boundary can be used to connect with other electrical part for electrical simulation while thermal boundary can be used to connect with other thermal part for thermal simulation.

As shown in [3], the proposed VP design tool is capable of both thermal and electromagnetic model generation. Electromagnetic model and its interaction with power semiconductor models will be focused in this paper. Thus, power semiconduc-



(a) $V_{GS} = -9$V



(b) $V_{GS} = -3$V

Fig. 3: SiC-JFET static characteristics comparison of different V_{GS} voltages

tor device behavioural model will be presented in the next section.

III. Power Semiconductor Devices Modelling

A unipolar power transistor can be generally modelled with the equivalent circuit shown in Fig. 2, which is presented by authors in [7]–[9] to model SiC-JFET, SiC-MOSFET and GaN-HEMT. Current source G_{ch} represent power transistor forward static characteristics, which is controlled by both V_{DS} and V_{GS} voltages. Body diode static characteristic is represented by a non-linear resistor R_{bd} and a constant resistor R_{bds}. The dynamic behaviour is modelled by three non-linear capacitors C_{gd}, C_{ds} and C_{gs} and each capacitor is only dependent on the voltage across it. Depending on device structure and packaging type, internal gate resistor and parasitic inductances could be added in this model.

A. Static characteristics modelling

A "Normally-on" SiC-JFET (IJW120R070T1, 1200V/35A, $V_{th} \approx -13.5$V) is modelled in this subsection.

When $V_{GS} > V_{th}$, at one V_{GS} voltage, the following equation can be used to represent the V_{DS}-I_D curve. All the parameters a, b and c in the above equation could be obtained based on datasheet or the measured values through fitting method by using $fmincon$ function in MATLAB.

$$I_D = a - \frac{a}{1 + \left(\frac{V_{DS}}{b}\right)^c} \tag{4}$$

The comparison between the model and the datasheet is shown in Fig. 3 at different V_{GS} voltages. It is shown that the chosen simple function can represent well the device static

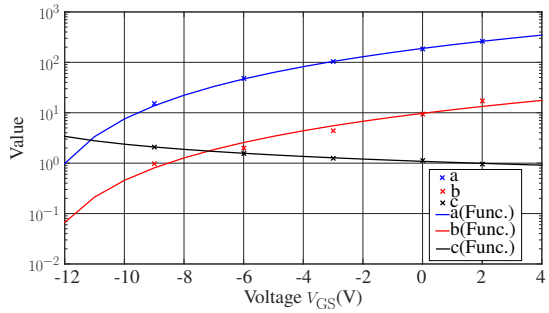


Fig. 4: Comparison between the function and the obtained parameters in eq.(4)

characteristics. The value of the parameters in eq.(4) can then be obtained on different V_{GS} voltage values. Following equation eq.(5) could represent the evolution of each parameter (when $V_{GS} > V_{th}$), where s indicates parameter a, b, c. The values of s_1-s_4 are given in TABLE. I.

$$s = \frac{s_1}{1 + \left(\frac{V_{GS} - V_{th}}{s_2}\right)^{s_3}} + s_4 \tag{5}$$

TABLE I: s_1-s_4 values in eq.(5) for each parameter (various units without physical meaning)

s	s_1	s_2	s_3	s_4
a	-1.05×10^4	71.46	2.4	1.05×10^4
b	-1.3×10^4	321.3	2.27	1.3×10^4
c	6.13	1.98	0.8	0

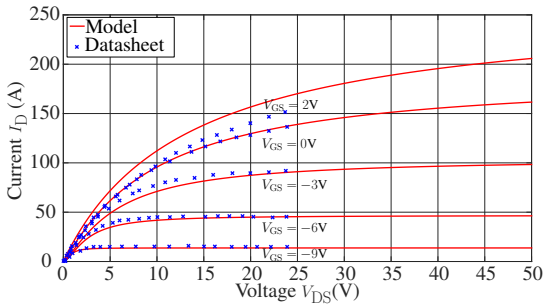
The comparison between eq.(5) and the obtained parameters in eq.(4) is shown in Fig. 4. The value of each parameter out of the datasheet range is obtained by extrapolation of the eq.(5). When device is reverse conducted, conduction current I_{SD} could be represented by the sum of the device channel current I_{ch} and body diode current I_{bd}, where non-linear resistor R_{bd} could be represented by the following equation, in which V_{bd} is the voltage across R_{bd}. Parameters $a_{bd} = 2.66\Omega$, $b_{bd} = 1.38V$, $c_{bd} = 1.244$ and $R_{bds} = 0.001\Omega$ are used to model body diode static characteristic. Thus, the comparison between the datasheet and the model is shown in Fig. 5, where it is shown that the model represents well the device static characteristics. However, the difference between the model and the datasheet relies mainly on the difference between the chosen function and the parameters in Fig. 4.

$$R_{bd} = \frac{a_{bd}}{1 + \left(\frac{V_{bd}}{b_{bd}}\right)^{c_{bd}}} \tag{6}$$

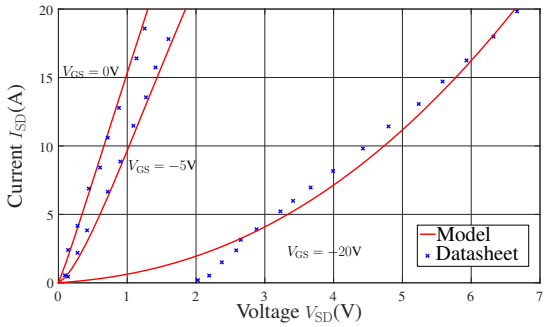
B. Dynamic characteristics modelling

The nonlinearity of both C_{gd} and C_{ds} are expressed by following mathematical function when V_x is inferior to 500V:

$$C_x = \frac{a}{1 + \left(\frac{V_x}{b}\right)^c} + d \times exp\left(-e \times V_x\right) \tag{7}$$



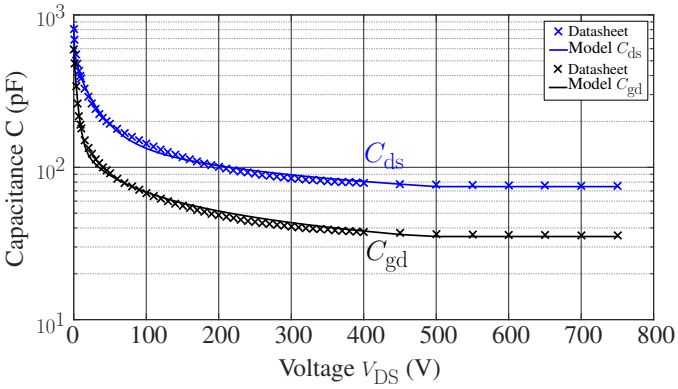
(a) Forward conduction



(b) Reverse conduction

Fig. 5: Comparison between the model and the datasheet on SiC-JFET static characteristics

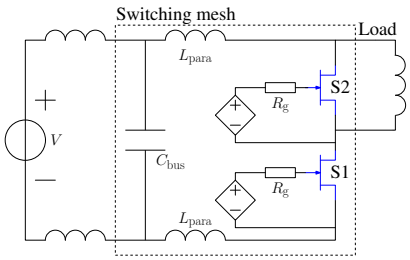
where C_x is the capacitance value and V_x is the voltage across the capacitor. In the range where V_x is superior to 500V, C_x is expressed by a constant capacitance value.



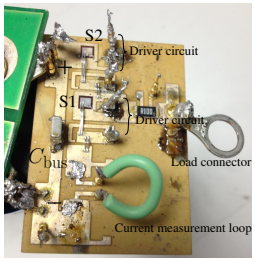
(a) C_{ds} values

Fig. 6: Comparison on inter-electrode capacitance values and their models

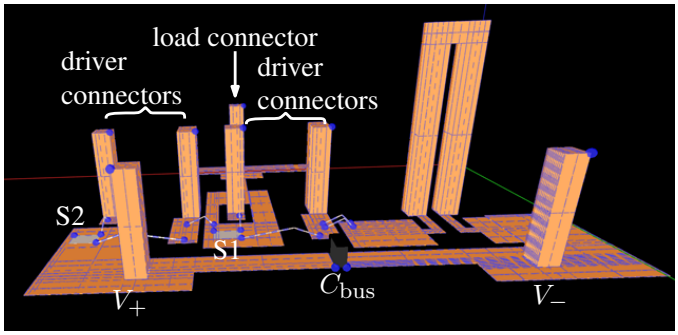
The comparison between inter-electrode capacitances datasheet values and their values are shown in Fig. 6, which shows that both C_{gd} and C_{ds} are expressed well by the chosen functions. For C_{gd} capacitance, the used parameters are $a = 2.5 \times 10^4(pF), b = 3.58 \times 10^{-4}(V), c = 0.464, d = 2 \times 10^4(pF), e = 0.22(V^{-1})$ and for C_{ds} capacitance, the used parameters are $a = 647(pF), b = 3(V), c = 0.398, d = 210.4(pF), e = 0.038(V^{-1})$.



(a) JFET half bridge electrical circuit



(b) JFET half bridge switching circuit



(c) JFET half bridge switching circuit representation

Fig. 7: JFET half bridge circuit and its representation

C_{gs} is assumed to be a constant capacitor and its value is the same as given in datasheet: 1.6nF.

The presented SiC-JFET model will then be implemented in the presented VP design tool. Device switching waveforms of the simulation will be compared with experimental measurements.

IV. Experimental Validation

A. SiC-JFET half bridge circuit representation

The SiC-JFET half bridge electrical circuit is shown in Fig. 7a, which is mainly constructed by a bus capacitor C_{bus}, two SiC-JFETs S1 and S2, driver circuit of each device and an air-core inductor as the load.

The switching mesh of the circuit is shown in Fig. 7b, where parasitic inductances could be found not only in the switching current loop, but also in the driver circuit.

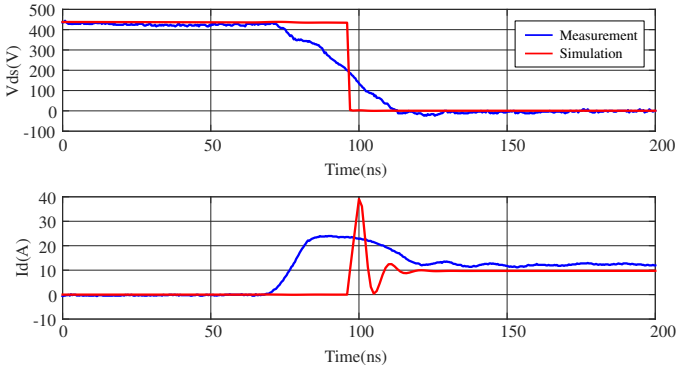
The switching circuit is then represented in the VP design tool, in which the PCB track of the switching mesh is represented with their geometric information. The power supply, C_{bus}, SiC-JFETs S1 and S2, device driver circuits and load are represented by their corresponding behavioural models in the simulation circuit through electrical boundaries, which are shown as blue points in Fig. 7c, where switching loop parasitic inductance L_{para} values are determined by the 3D meshed model.

SiC-JFET S1 switching current I_D and switching voltage V_{DS} are compared between the measurement and simulation, of which the results are presented in the following subsection.

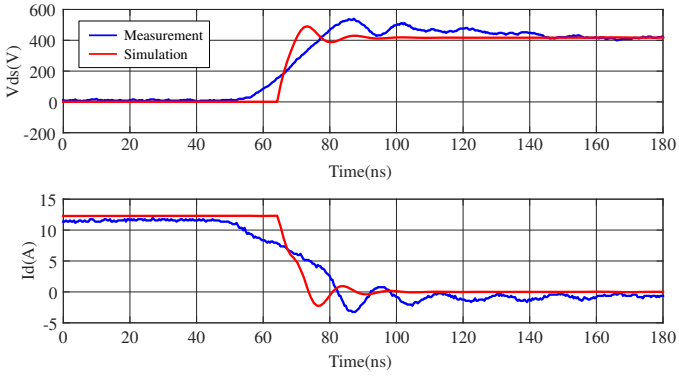
B. Comparison results

Current I_{D} and voltage V_{DS} are compared in the three conditions below. In condition 1, simple SiC-JFET device model (ideal switch with a parallel RC branch) as that presented in [3] is used and parasitic inductance values are extracted by the software. In condition 2, the presented SiC-JFET model is used, however there is no parasitic inductance values extracted. In condition 3, the presented SiC-JFET model is used while parasitic inductance values are extracted and used in the simulation.

1) Condition 1: The comparison between the measurement and the simulation in this condition is shown in Fig. 8. The simple device model could not represent good I_{D} and V_{DS} switching transitions, because the capacitance value in the model is constant and there is no capacitive coupling (Miller effect) between drain and gate of the device. The obtained switching energies of the simulation are: $E_{\mathrm{on}} = 0.5\mu\mathrm{J}$ and $E_{\mathrm{off}} = 11\mu\mathrm{J}$, which is far from those of the measurement: $E_{\mathrm{on}} = 165\mu\mathrm{J}$ and $E_{\mathrm{off}} = 25\mu\mathrm{J}$. Thus, the ideal model yields an inaccurate switching loss as the measurement.



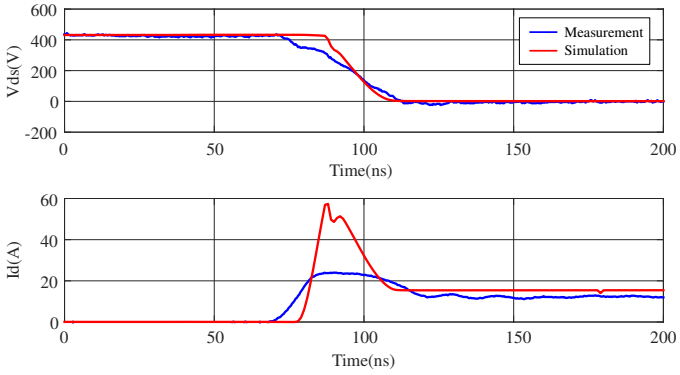
(a) JFET ON



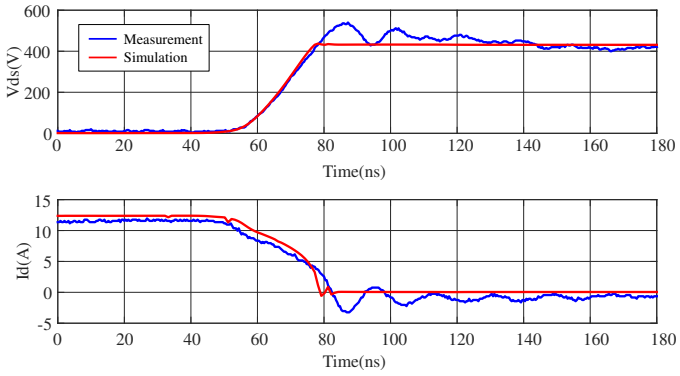
(b) JFET OFF

Fig. 8: JFET switching waveforms comparison of condition 1

2) Condition 2: The comparison between the measurement and the simulation in this condition is shown in Fig. 9. As parasitic inductances in the circuit are not extracted, LC resonance at the end of the turn-ON and turn-OFF switching are not represented in the simulation. Meanwhile, device turn-ON dI/dt transition is much faster than measurement, which yields a bigger turn-ON I_{D} peak current. The obtained switching energies of the simulation are: $E_{\mathrm{on}} = 218\mu\mathrm{J}$ and $E_{\mathrm{off}} = 34\mu\mathrm{J}$, which is close than ideal model but still different from the measurement.



(a) JFET ON



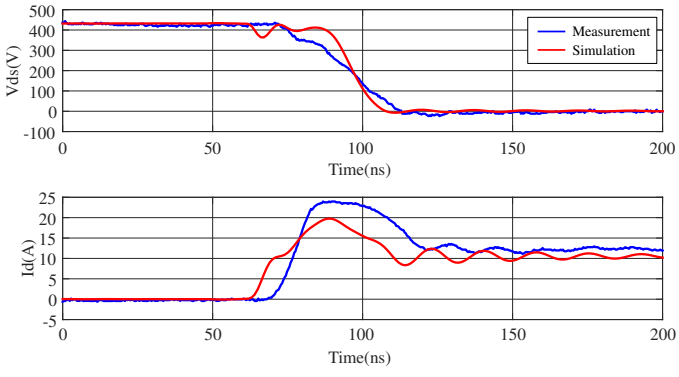
(b) JFET OFF

Fig. 9: JFET switching waveforms comparison of condition 2

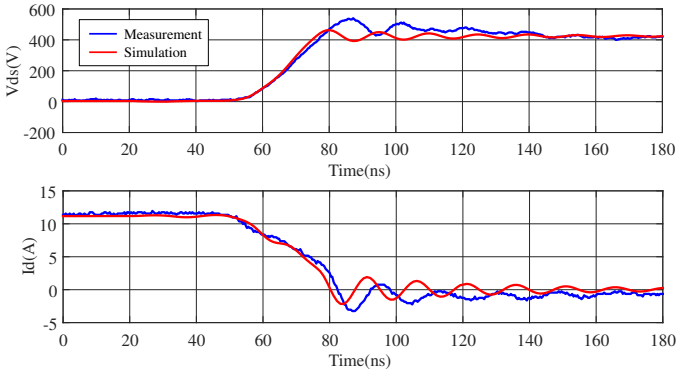
3) Condition 3: The comparison between the measurement and the simulation in this condition is shown in Fig. 10, where it shows that device switching waveforms are closer to the measurement by adding parasitic inductances and the presented device behavioural model. The simulation represents generally well the measurement on both current, voltage transition and LC resonance at the end of the switching. LC resonance frequency is accurately represented, which demonstrates that device output capacitance value C_{oss} and switching loop parasitic inductances are well simulated. Device turn-OFF dI/dt and dV/dt are represented well by the simulation. The main difference between the measurement and the simulation is the turn-ON switching transition, which is mainly due to the inaccurate representation of the stored charge in the simulation when upper device S2 is reverse conducted. Future work will be focused on how to correctly represent this parameter in the model. The obtained switching energies of the simulation are: $E_{\mathrm{on}} = 148\mu\mathrm{J}$ and $E_{\mathrm{off}} = 28\mu\mathrm{J}$, which are closer to the measurement than above two conditions.

Simulation time to obtain the above results is within 1 minute, which includes the generation of inductance equations from 3D model, MOR and simulation time of 71μs with $1n$s time step. The MOR method helps to reduce the original 723

equation model to 23 equation model in order to accelerate simulation speed. The presented device model could be also used in circuit simulation software such as PSPICE. However, as parasitic inductances could influence on device switching waveforms, their values including mutual inductances of the switching mesh are necessary to be extracted and added in simulation circuit, which might consume lots of time.



(a) JFET ON



(b) JFET OFF

Fig. 10: JFET switching waveforms comparison of condition 3

V. Conclusion

A virtual prototyping (VP) design tool using power semiconductor device behavioural models is presented in the paper. Different modelling techniques are used to model different components in the design tool and by using model order reduction algorithms, simulation speed could be increased.

A behavioural model of a SiC-JFET is then presented, in which device static and dynamic characteristics are represented by mathematical functions. The model is then implemented in the VP design tool, where a SiC-JFET based half bridge circuit is represented. By comparing with the simulation of a simple device model and the simulation without parasitic inductances extraction, it is shown that circuit electromagnetic model together with power semiconductor device behavioural model could represent well device switching waveforms, so device switching losses can be accurately calculated. Future work will include thermal model based on the presented results, so as to evaluate device electrical thermal performance.

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