Submodule Power Losses Balancing Algorithms for the Modular Multilevel Converter

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***Abstract*—Tolerance and component aging can cause significant differences in the capacitance values of the submodules (SMs) in a modular multilevel converter (MMC). Depending on the modulation technique, capacitance mismatches may produce uneven switching transitions of the SMs, hence imbalances in the power losses that can lead to reliability problems. In this paper, a new algorithm that helps to achieve evenly distributed switching and conduction losses within the converter SMs is presented. The proposed algorithm is based on a modification of the common voltage balancing algorithms, balancing a weighted function of voltage and losses. Even distribution of power losses is achieved at the cost of slightly increasing the capacitor voltage ripples. The effectiveness of the strategy has been demonstrated by simulation results of a high-power grid-connected MMC.**

***Index Terms*—Modular multilevel converter, power losses, capacitor voltage ripples, reliability improvement.**

I. Introduction

The modular multilevel converter (MMC) [1], [2] is one of the most attractive topologies for medium- and high-power applications like high-voltage direct current (HVDC) transmission systems [3]. The main features of the MMC are [1]: (i) its modularity and scalability to different power and voltage levels, (ii) its high efficiency, (iii) the high quality of the output voltages, and (iv) the absence of additional capacitors on the dc link, as the storage is distributed among the capacitors in the submodules (SMs) of the converter.

Reliability is one of the most important challenges in MMCs, since they include many switching devices, which are the weakest components in power converters [4], [5]. One of the main reasons for failure of high-power semiconductors is the aging produced by mechanical and thermal stresses [6], [7], caused by semiconductor power losses. For low and medium voltage applications, where a low number of SMs is used, the switching and conduction power losses are evenly distributed among the SMs [8]. However, in HVDC applications, the high number of SMs per phase-leg may result in significant imbalance distribution of power losses and temperature in the semiconductors [9]. Consequently, uneven degradation of the semiconductors is produced, reducing the converter reliability.

Capacitance values are different among SM capacitors due to both fabrication tolerance and aging of the capacitors [10], [11]. This may produce uneven distribution of switching transitions and power losses in the SMs. The effect is more significant in high-power MMCs, which already have unbalanced power loss distribution. In this paper, in addition to studying the loss distribution in converters with mismatched capacitances, a power loss balancing strategy is presented. The strategy is based on modifying the input of the voltage balancing algorithm based on sorting the SM capacitor voltages [12]. The presented strategy is based on adding an offset to the input of the voltage balancing algorithm, modifying the activation priority of the SMs according to the losses balancing objective. Two algorithms for calculating the losses balancing offset are presented. The first algorithm is based on balancing the number of switching transitions of each SM, and the second one is based on balancing the estimation of both switching and conduction losses. In this paper, a level-shifted pulse-width modulation (LS-PWM) is used, and a voltage balancing algorithm with reduced switching frequency is used [13], [14].

The remainder of this paper is organized as follows. Section II describes the converter topology and summarizes the modulation and control methods applied. Section III analyzes power loss distribution among the SMs of the converter when there are mismatches in the capacitance values. Section IV introduces the loss balancing strategy, and Section V analyzes the performance of the proposed strategy by simulation. Finally, Section VI concludes the paper.

II. MMC Topology and Basic Operation

The general topology of an MMC consists of two arms per phase-leg, where each arm comprises N series-connected, identical SMs and a series arm inductor, L. Each SM contains a half-bridge circuit and a capacitor C. The output voltage of each SM equals to its capacitor voltage (v_C) when the SM is activated, or zero when it is deactivated. A circuit diagram of the MMC is depicted in Fig. 1.

The voltage waveforms at the ac-side of the MMC are synthesized by a modulation algorithm that defines the number of SMs to be activated in each of the arms, and the particular SMs to be activated are determined by a voltage balancing algorithm. In this paper, a level-shifted pulse-width modulation (LS-PWM) technique is used, which compares the reference signal with a set of level shifted carriers. Capacitor voltage

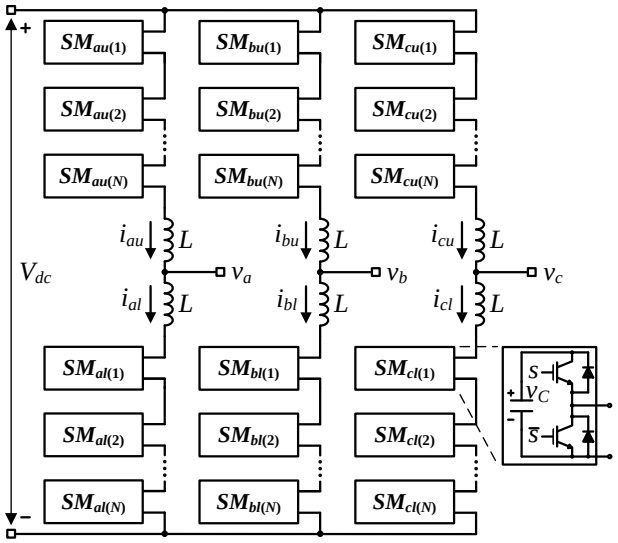


Fig. 1. Circuit diagram of a three-phase MMC with N basic SMs and M additional SMs per arm.

balancing is achieved by selecting the SM with lower voltage when the arm current is positive, and the SM with higher voltage when the arm current is negative. In order to reduce the switching losses, an algorithm that limits the number of SM transitions per switching period is implemented [13]. The voltage reference for the modulation algorithm is provided by a typical d-q current controller for grid-connected applications.

Moreover, a circulating current control technique has also been implemented [15]. This technique improves the converter dynamics and controls the harmonic components in the circulating current with the aim of reducing the capacitor voltage ripples.

III. Power Loss Distribution with Unbalanced SM Capacitances

The main factors for capacitance mismatches in SM capacitors are fabrication tolerance, which can reach 20% in electrolytic capacitors, and aging degradation. Small differences between the SM capacitors does not affect significantly the quality of the output voltages and currents, and neither the capacitor voltage ripples, since those variables are usually regulated through closed-loop techniques. However, the control action to balance the capacitor voltages can lead to uneven distribution of power losses among the SMs, which reduces the converter reliability.

A. System Definition

The effects of nonidentical capacitances in the SMs are evaluated through simulation analysis. A simulation model of a 70-MW high-power grid-connected MMC is implemented in MATLAB/Simulink with the PLECS toolbox. The control system described in Section II is applied. The main characteristics of the MMC simulation model are shown in Table I.

TABLE I
Specifications of the Simulation Model of the MMC

Parameter	Value
Number of SMs per Arm, N	10
SM Capacitors, C	1500 μF
Arm Inductors, L	9 mH
DC-Link Voltage, V_{dc}	100 kV
Nominal Output Power, P	70 MW
Carrier Frequency, f_s	2 kHz
Output Frequency, f	50 Hz

TABLE II
Linearized Static and Dynamic Semiconductor Specifications at 125°C

Parameter	Value
Diode Forward Voltage, V_F	1.15 V
Diode Equivalent Series Resistor, R_D	0.7 mΩ
IGBT Collector-Emitter Saturation Voltage, V_{CE}	1.3 V
IGBT Equivalent Series Resistor, R_{CE}	1.1 mΩ
Diode Reverse Recovery Energy at 800 A, E_{rec}	218 mJ
IGBT Turn-on Energy Loss at 800 A, E_{on}	242 mJ
IGBT Turn-off Energy Loss at 800 A, E_{off}	320 mJ

The power losses of each SM are calculated using the simulation model and considering the use of commercial semiconductors, particularly, the insulated-gate bipolar transistor (IGBT) Fuji Electric 1MBI1200U4C-170, which maximum ratings are forward current 1200 A and direct voltage 1700 V. In order to fulfill the voltage ratings of the SM, the use of seven semiconductors connected in-series has been considered. For the sake of simplification, the losses have been calculated considering the same voltage drop in each of the semiconductors. The semiconductors (IGBT and diode) characteristics used for the power losses calculation are shown at Table II. Those characteristics have been obtained from the semiconductor datasheet by linearizing the static and dynamic curves at 125°C.

The conduction losses for the IGBTs ($P_{con\,T}$) and diodes ($P_{con\,D}$) are calculated from linearizing the datasheet characteristics. The simplified model of the switches in the on state can be represented by a voltage source (V_{CE} and V_F for the IGBT and the diode, respectively) and a series equivalent resistor (R_{CE} and R_D for the IGBT and the diode, respectively). The average conduction power losses are calculated over a fundamental period (T):

$$P_{con\,T} = \frac{1}{T}\int_0^T \left(V_{CE} + R_{CE}\, i_T\right) i_T \, dt \text{ and} \qquad (1)$$

$$P_{con\,D} = \frac{1}{T}\int_0^T \left(V_F + R_D\, i_D\right) i_D \, dt\,, \qquad (2)$$

where i_T and i_D represent the currents through the IGBT and diode, respectively.

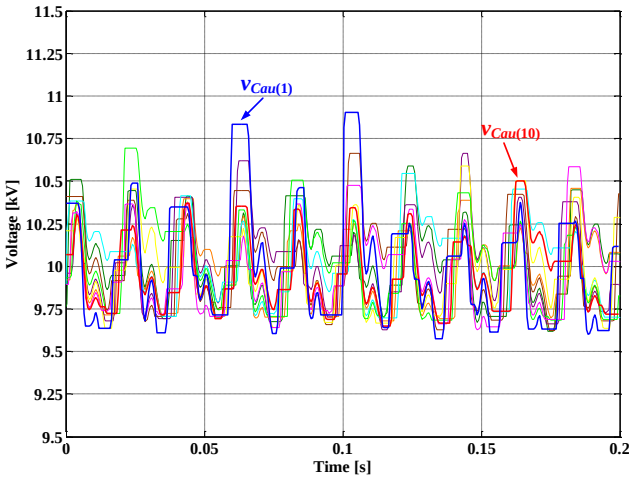


Fig. 2. Upper arm capacitor voltages when using mismatched capacitances in the SMs.

The switching losses for the IGBT are calculated as individual energy losses during the turn-on and turn-off transients. For the diode, only the turn-off transients are considered, since the turn-on losses can be considered negligible. The energy loss functions have been obtained by approximating the datasheet curves to second order polynomials with the current as a variable. The functions is also scaled to the off-state collector-emitter voltage (capacitor voltage v_C). The average power losses are calculated as the sum of all the individual energy losses over a fundamental period:

$$P_{sw\,T} = \frac{1}{T}\sum_{j=1}^{n}\left[E_{on_j}(i_T, v_C) + E_{off_j}(i_T, v_C)\right] \text{ and} \quad (3)$$

$$P_{sw\,D} = \frac{1}{T}\sum_{j=1}^{n}\left[E_{rec_j}(i_D, v_C)\right], \quad (4)$$

where n is the number of transitions in one fundamental period, and v_C is the voltage of the SM, which is the voltage across the semiconductor in the off state.

B. Performance with Unbalanced Capacitances

The following study shows power losses distribution when the capacitances in the SMs are different. In the simulations, the SM capacitors have been modified, using 50% of the nominal capacitance in the first SM of phase a ($C_{au(1)}$), and using values for the rest fo SMs that increase gradually from 85% of the nominal capacitance in the second SM ($C_{au(2)}$), to 115% of the nominal capacitance in the last SM of the upper arm ($C_{au(10)}$). The output is controlled to provide 70 MW of active power, which corresponds to 777 A rms output current.

Fig. 2 shows the upper arm capacitor voltages of phase a. Despite the capacitance mismatch, the capacitor voltages are relatively balanced, maintaining their values within acceptable limits. The capacitor voltage of SMau(1), which has the smallest capacitance, presents a faster dynamic than the other capacitors, with a peak-to-peak voltage ripple 35% larger than the average value. On the contrary, the SM with the highest capacitance, i.e. SMau(10), presents the lowest ripple, with a peak-to-peak value 20% lower than the average one.

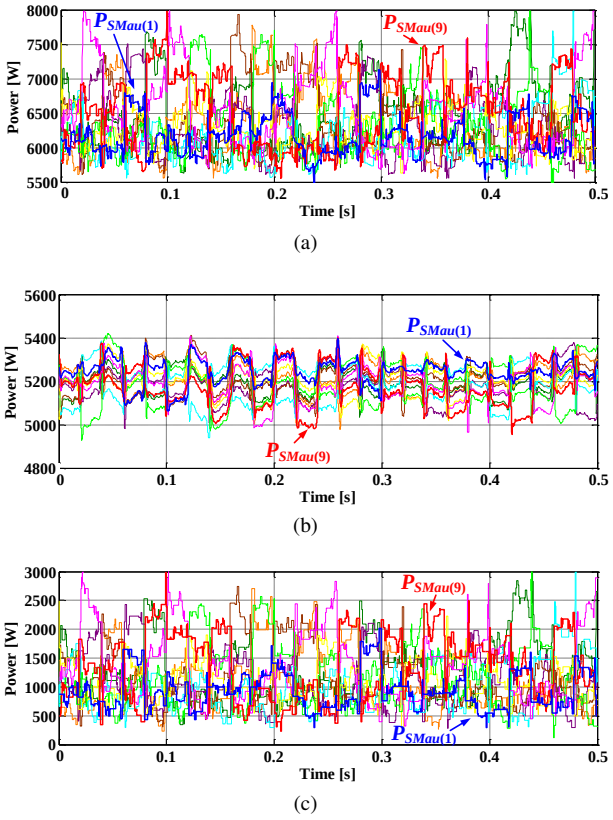


Fig. 3. Power losses of the upper arm SMs when using mismatched capacitances in the SMs: (a) total power losses, (b) conduction power losses and (c) switching power losses.

On the contrary, the semiconductor power losses are significantly unbalanced. Fig. 3 shows the averaged values of the total, switching and conduction losses. The power losses have been averaged over a fundamental period using a moving average window for all the represented period. Fig. 3(a) shows the total power losses in each SM. Due to the reduced switching frequency of each SM, the power losses show oscillating dynamics, with a frequency lower than the fundamental of the output current. It can be observed that the total power losses of SMau(1) are lower than the average. On the contrary, the power losses of SMau(9), where the capacitance is increased by 10%, are the highest ones. The total power losses averaged over a long period (4 s) are 6.12 kW and 6.47 kW for SMau(1) and SMau(9), respectively, which means an unbalance of 5.7% in the power losses.

As it can be seen in Fig. 3(b), the conduction losses are not the main reason for power loss imbalance, which are well balanced. The switching power losses are represented in Fig. 3(c), which are significantly unbalanced. An imbalance of 47% can be observed between SMau(1) and SMau(9), with total average power losses of 875 W and 1.28 kW, respectively.

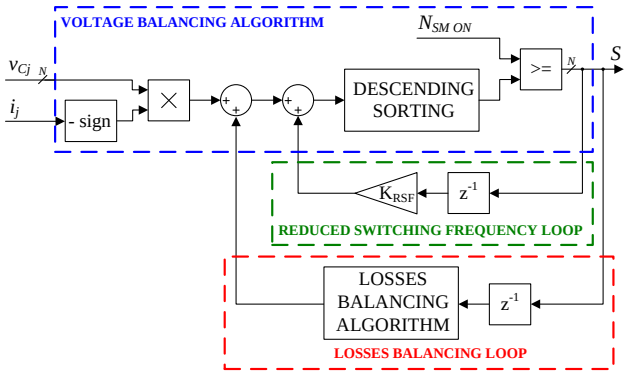


Fig. 4. Block diagram of the losses balancing strategy.

IV. Power Losses Balancing Algorithms

The proposed strategy to achieve balanced power losses among the SMs of an arm is based on the degree of freedom that the MMC offers when selecting the particular SMs to be activated. This degree of freedom is generally used for balancing the capacitor voltage ripples. In this paper, the SM selection is based on a weighting function, where both the SM capacitor voltages and the SM power losses are considered.

The voltage balancing algorithm used in this application is based on multiplying the capacitor voltages by the opposite sign of the arm current and sorting them in descending order [13]. That is, when the current goes in the charging direction (positive), the voltages are multiplied by -1, giving higher priority of activation to the ones that have the lowest values (highest values when inverted). On the contrary, when the current is in the discharging direction (negative), the SMs with the highest voltages have higher priority to be activated. The algorithm also includes a feedback loop that adds a constant offset to the already activated SMs. With this feedback, the already activated SMs increase their priority, and the number of transitions is reduced to the minimum as possible, i.e. two per switching period.

The proposed energy balancing strategy modifies the input to the sorting algorithm by adding a second offset. The offset is calculated to change the priority of activation of the SMs to balance the SM power losses. Fig. 4 shows the block diagram of this strategy integrated with the voltage balancing algorithm. Two different algorithms are proposed to calculate the offset added to the input of the sorting algorithm.

A. Switching Balancing Algorithm

As shown in Section III, capacitance variation can create significant imbalances in the switching power losses among the SMs. For this reason, a first approach is to balance the switching power losses by distributing the number of transitions evenly among the SMs. The hereinafter called switching balancing (SB) algorithm aims to achieve this objective.

The SB algorithm starts by counting the number of transitions of each SM. Then, the average number of transitions is calculated by adding all the SM transitions and dividing by the number of SMs. Finally, the deviation of each SM from the average value is calculated. If the deviation is positive (the number of transitions of the SM is higher than the average) the algorithm tries to avoid the change of state of the SM. On the contrary, if the deviation is negative, the algorithm tries to change the state of the SM.

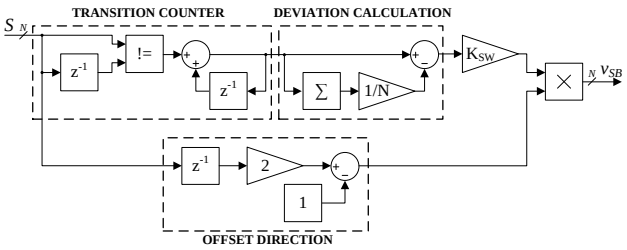


Fig. 5. Block diagram of the Switching Balancing Algorithm.

In order to reduce the probability of changing the state, the activation priority is increased when the SM is activated, and reduced when the SM is deactivated. That is, a positive offset is added when the SM is activated and a negative one when it is deactivated. The value of the offset consists on the deviation multiplied by a feedback gain, therefore, when the deviation is negative, the offset is applied in the opposite direction. A block diagram of the SB algorithm is depicted in Fig. 5.

The feedback gain has to be adjusted to the specifications of each converter. In this study, it has been approximated to 20% of the capacitor voltage ripples when the switching deviation is the number of transitions performed by a SM over a fundamental period:

$$K_{sw} = \frac{0.2\Delta V_c N}{f_s T} \,. \tag{5}$$

B. Total Losses Balancing Algorithm

The second algorithm proposed in this study is called the total losses balancing (TLB) algorithm. It directly balances the power losses of each semiconductor. For this purpose, the conduction power losses of the upper and lower IGBTs and diodes are estimated and their deviation calculated. Since the states of the upper and lower switches are complementary, the switching losses are estimated and balanced for the whole SM, not for each semiconductor.

The conduction power losses depend on the sign of the current, i.e., when the current is positive, the upper diode or lower IGBT will carry the arm current, while the upper IGBT or lower diode will carry the arm current when it is negative. For this reason, the output offset is calculated differently when the current is positive or negative and using only the deviations that can be controlled at each moment. To reduce the power losses in the upper semiconductors, the activation priority should decrease, facilitating SM deactivation. On the contrary, the priority should increase to reduce the power losses of the lower semiconductors. Since the sorting algorithm is calculated in descending order, a positive offset means an increase in the activation priority, and a negative offset a

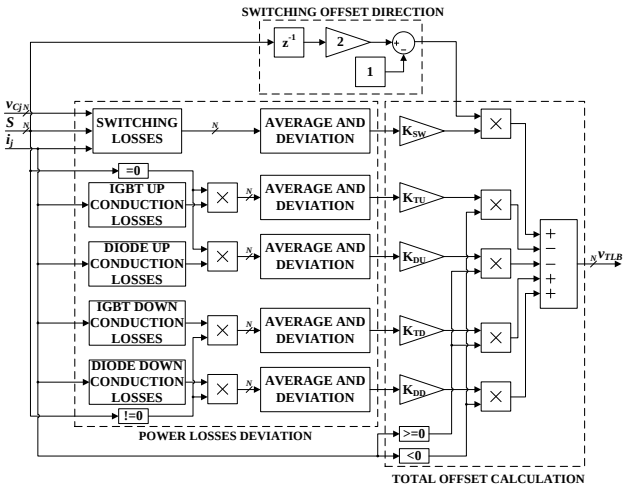


Fig. 6. Block diagram of the SB algorithm.

decrease in such priority.

The switching power losses are estimated according to the dynamic characteristics of the semiconductors, approximated from the datasheet to a second order polynomial, and the measured values of voltages and currents in the SMs. Once the power losses and their deviations are calculated, they are balanced in a similar way the number of switching transitions in the SB algorithm, thus increasing the priority of changing the state when the deviation is negative and decreasing the priority of changing the state when it is positive.

The total offset of the TLB algorithm is calculated as the sum of all the correcting actions. Fig. 6 shows a block diagram of the TLB algorithm. Each one of the correction offsets is multiplied by a feedback gain, which can be calculated similarly to the SB algorithm. In this case, the offset has been adjusted to 50% of the capacitor voltage ripple when the deviation is equal to the average power in the semiconductor:

$$K_{P\,device} = \frac{0.5\Delta V_c}{P_{device}}\,, \tag{6}$$

where the subindex *device* indicates the semiconductor where the conduction power losses are balanced (upper IGBT, upper diode, lower IGBT or lower diode) or the SM switching power losses.

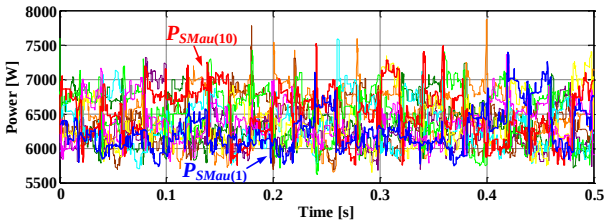
V. Simulation Results

The proposed power losses balancing strategy is tested by simulation, and the performance of the two proposed algorithms is compared, i.e. the SB and the TLB algorithms. The same mismatches in the capacitor values detailed in Subsection III-B are assumed.

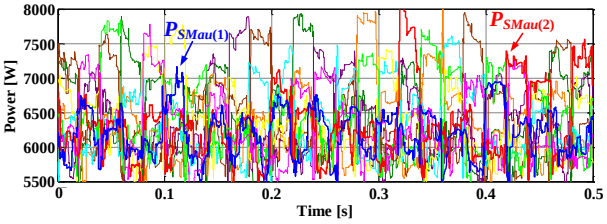
Fig. 7 shows the total averaged power losses of the SMs in the upper arm of phase a. Fig. 7(a) represents the power losses when applying the SB algorithm. Since the main imbalance without control appears in the switching power losses, balancing the number of switching transitions improves the overall balance of total power losses in the SMs. The figure depicts averaged power losses with less oscillations than when

TABLE III
Power Losses Imbalances with Different Strategies

Strategies	Maximum Power Loss Imbalance
No power losses balancing strategy	5.7%
SB algorithm	3.8%
TLB algorithm	1.4%



(a)



(b)

Fig. 7. Power losses of the upper arm SMs when using the balancing strategy: (a) SB algorithm and (b) TLB algorithm.

no balancing strategy is applied (Fig. 3(c)). The total average power losses for a long period (4 s) are 6.18 kW and 6.42 kW for the SM with the highest capacitance (SMau(1)) and the lowest capacitance (SMau(10)), respectively. This means that the maximum power losses imbalance among SMs has been reduced to 3.9%.

Fig. 7(b) represents the power losses when applying the TLB algorithm. Although the figure depicts averaged power losses with low frequency oscillations, the total averaged value for a long term demonstrates that this algorithm efficiently balances the power losses. The SM with the lowest losses is the on with lowest capacitance, SMau(1), which presents an average of 6.32 kW, while the SM with the lowest losses is SMau(2), the second SM with less capacitance (a reduction of a 15%), with an averaged value of 6.41 kW. Therefore, the maximum unbalance is only a 1.4%. A summary of the power losses unbalance with the different algorithms is shown in Table III.

Since the objective of the power losses balancing strategy is to reduce the aging of the SMs with the highest power losses, it is interesting to see that both power losses balancing algorithms reduce the maximum value of power losses. While the converter without control strategy presents a power loss of 6.47 kW, the maximum obtained with the SB algorithm is 6.42 kW, and with the TLB algorighm is 6.41 kW. Therefore, it can be stated that the proposed algorithms reduce the

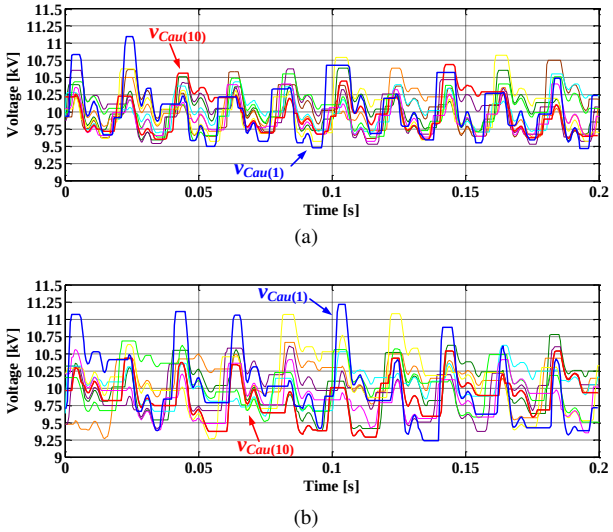


Fig. 8. Upper arm capacitor voltages: (a) SB algorithm and (b) TLB algorithm.

accelerated aging of some semiconductors.

Since the proposed algorithms are based on modifying the input signals of the capacitor voltage balancing algorithm, the capacitor voltage ripples should also be evaluated. Fig. 8 shows the SM capacitor voltages of the upper arm. Fig. 8(a) shows the SM capacitor voltages when using the SB algorithm. As observed, the SM capacitor voltages have the same average value, but the voltage ripples are higher compared with the case of not using power losses balancing control (Fig. 2). While the original voltage ripples have a peak-to-peak value of 1.2 kV, the voltages obtained with the SB algorithm present a peak-to-peak value of 1.6 kV.

As shown in Fig. 8(b), the capacitor voltage ripples are similar when using the TLB algorithm. Since the offset applied with this algorithm is larger, the capacitor voltage ripples are slightly increased. The maximum peak-to-peak voltage ripple in the smallest capacitor is now 2 kV.

The increase of the capacitor voltage ripples can cause some negative effects, such as worsening the quality of the output voltages and reducing the lifetime of the capacitors. Nevertheless, the maximum peak-to-peak value of the capacitor voltage ripples is maintained within a reasonable value, i.e. 20% of the nominal voltage. These effects have not been considered in this paper and will be studied in future research.

VI. Conclusion

In this paper, the effects of difference capacitance values among SMs of an MMC have been studied. The capacitance differences can cause uneven distribution of the semiconductor power losses, accelerating the aging of some semiconductors, and hence, reducing converter reliability. To address this problem, a power losses balancing strategy has been presented, which is based on modifying the input signals of the capacitor voltage balancing algorithm. Two solutions are proposed: an algorithm based on balancing the number of switching transitions and another algorithm based on balancing the estimated power losses in the semiconductors. The effectiveness of the proposed algorithms has been studied through simulation results. It has been demonstrated that the two algorithms reduce power losses imbalances, although they increase the capacitor voltage ripples. The proposed strategy can also be used to force imbalances in the distribution of semiconductor power losses. This can be useful in MMC where the physical location and cooling conditions of the SMs produce uneven distribution of heat dissipation, which can be compensated by forcing imbalances in the SM power losses.

Acknowledgment

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