Hybrid Inverter Arrangements to Facilitate Reduced Switching Losses of the Main Inverter

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***Abstract*— This paper investigates two hybrid inverter topologies consisting of a slow switching DC/AC main voltage source inverter and output series connected low-voltage rated, fast switching auxiliary inverters that may be suitable for medium and high voltage AC grids. Two topologies of auxiliary inverters are investigated: the use of AC choppers implemented with bidirectional switches as well as using the more traditional H-bridge inverter. A modified modulation scheme for the main inverter enables the elimination of the zero voltage vectors which allows the use of only two switchings per switching period which may reduce significantly the associated switching losses. As the result is a quasi-trapezoidal output phase voltage, the auxiliary inverters are controlled to remove the differential mode distortion. Simulation results prove that the proposed hybrid grid interface is able to provide low harmonic voltage content.**

Keywords*— *AC-DC power conversion, Active filters, AC-AC power conversion, Space-vector modulation, Harmonic Injection.

I. INTRODUCTION

Power transmission through DC grids over long distances is expected to be the adopted technology in the future, offering benefits like lower installation costs in power cables and minimization of transmission losses. This means that the power electronics which will facilitate the interface between the DC and the AC systems with become the most expensive part subject to significant challenges such as supplying high quality power at high conversion efficiency, control fast and accurately the active and reactive power, maintain the stability of the grid as well as the quality of AC voltage, and be able to operate in unbalanced/distorted AC voltage conditions.

For medium voltage applications implementing a multi-level converter [1]-[5] is an interesting choice to overcome the voltage limitations imposed by the available switching devices when used in a 2-level inverter. In addition, it is able to supply voltage waveforms with smaller voltage steps and lower harmonic content that require smaller passive filters. In particular, Cascaded based H-bridge topologies (including the MMC) are commonly used to provide direct interface with medium voltage AC grids because of advantages like modularity that enables cost savings and easy scaling up to customized voltage levels, but the implementation is complex. Two level voltage source inverters are simpler to implement but would require high voltage rated switches, which have significantly poorer switching performance (higher switching loss per same kVA switched) and need large LCL filters when used in medium/high voltage inverter applications.

This paper explore the possibility to employ a hybrid arrangement consisting of a slow switching inverter suitable to use a 2-level topology with medium voltage power semiconductors that processes the bulk power in conjunction with auxiliary inverters that remove the low order harmonics caused by the reduction of switching effort of the main converter. First, a variation of the Space Vector Modulation (SVM) is presented that enables a significant reduction of the number of switchings resulting in a single inverter leg commutating during the switching period. The impact in the output phase voltage waveform is analyzed compared to a standard six pulse square wave with a view to identify the voltage rating requirements in the auxiliary inverters. Two solutions for the auxiliary inverters, an AC chopper powered via auxiliary transformers and the use of H-bridge inverters are proposed. The quality of the output waveform is analysed in conjunction with a passive loads. The limitation of using the AC chopper in controlling the power flow when connected to an AC grid are identified but it is proven that the auxiliary H-bridge inverters can provide accurate and fast active and reactive power flow control. Finally, a solution to synchronise the switching of the main and auxiliary inverters is proposed to enable overall reduction of switching loss].

II. MODIFIED SPACE VECTOR MODULATION WITH ZERO VOLTAGE STATE ELIMINATION

When SVM is used for a two level VSI, it utilizes a combination of two adjacent active voltage vectors to control the direction and a zero-voltage vector to control the magnitude of the output voltage vector V_{out} as illustrated in Fig. 1. The proportion between the duty-cycles of the two active adjacent voltage vectors V_α, V_β gives the direction whilst the duty-cycle of the zero-vector is critical in determining the magnitude of the reference voltage vector.

$$d_\alpha = m_U \cdot \sin\left(\pi/3 - \theta^*_{out}\right); d_\beta = m_U \cdot \sin\theta^*_{out}; d_0 = 1 - d_\alpha - d_\beta \qquad (1)$$

where m_U is the modulation index and ϑ^*_{out} is the angle within the sector of the output voltage reference vector.

For converters aiming to produce a sinusoidal wave, V_{out} needs to follow smoothly (constant rotational velocity) the

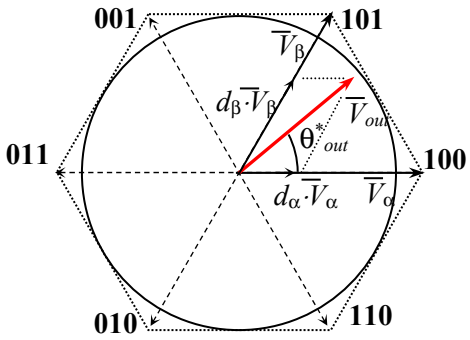

Fig. 1. The synthesis of the voltage reference space vector using the two adjacent active vectors.

trajectory of a circle (constant magnitude). For this reason, the duration of the zero state cannot remain constant during the switching period; it is larger when the reference voltage vector gets closer to the sector boundaries and has a minimum value in the middle of the sector when the resulting combined magnitude of V_α, V_β is minimum. It is possible to remove completely the zero switching state with positive impact in reducing the number of switchings (and associated losses) and still produce a resulting voltage vector that has a constant rotation velocity by maintaining the same relative duration of the two active dutycycles, which means the dutycycles need to be multiplied by:

$$k_{duty}=1/\left[\sin(\theta)+\sin(\pi/3-\theta)\right] \quad (2)$$

However, the magnitude of the resulting voltage vector will follow a hexagonal path rather than a circle and this may cause low order (5th, 7th etc) harmonics which can be corrected by means of inserting a series active filter which adds additional switching devices but of significantly smaller voltage ratings (and associated switching losses). Before developing solutions for controlling such auxiliary active filters, it is important to assess the added installed power of the auxiliary inverters.

III. Analysing the Waveform Profile of the Single Leg Switched VSI

The simplest waveform a 2-level VSI can synthetize is a pure square wave when each of the three phases of a VSI produces a given state for the whole duration of a sector as shown in Fig. 1. If the common mode voltage (Va+Vb+Vc)/3 is removed from the resulting phase voltage waveform, which is the case for an 3-phase/3 wire AC load with no ground connection of the neutral, the result is a 4-voltage level waveform as shown in Fig. 2a. The fundamental waveform content has a peak larger than the available DC-link voltage ($4/\pi$) but also a large level of low order harmonics (5th, 7th etc). The voltage waveform synthetized by a VSI that switches a single leg (no zeros state), is a trapezoidal waveform as shown in Fig. 2b. Whilst the trapezoidal waveform contains also a significant level of distortion, most is common mode (multiple of 3rd) which will not cause harmonic currents in a 3-phase load with a floating neutral. Fig. 2b shows the resulting waveform if this common mode component is subtracted from the trapezoidal modulating wave whist Fig. 2c shows the comparison of the harmonic residual voltage that needs to be synthetized by the series auxiliary phase inverter in order to clean these two non-sinusoidal voltages. The important finding is that an auxiliary inverter with a significant voltage rating ($233V_{pk}$) will be needed in the case of the VSI with 6-pulse voltage waveform, which represents 33.3% of the main inverter DC-link voltage (700V) whilst for the inverter that switches with PWM only one leg and produces a trapezoidal waveform, the harmonic residual voltage peak is only 40.7V which represents only 5.8% of the voltage rating of the main VSI. This means that if the main VSI works with 10kV in the DC-link, the switches in the auxiliary inverter will be subject to $580V_{pk}$ stress. It should be noted that this voltage level does not include the additional extra voltage needed to control the current in the line side inductors when grid connected. A significant shortcoming of such a solution, is that as the main inverter works without zero states, its voltage ratio is fixed which means that for a given AC grid, the DC-link voltage needs to be controlled by the converter at the other end of the HVDC line. With regards to Fig. 2, it should be noted that the peak of the residual harmonic signal is matching the peak of the fundamental component as highlighted in Fig. 2b-c.

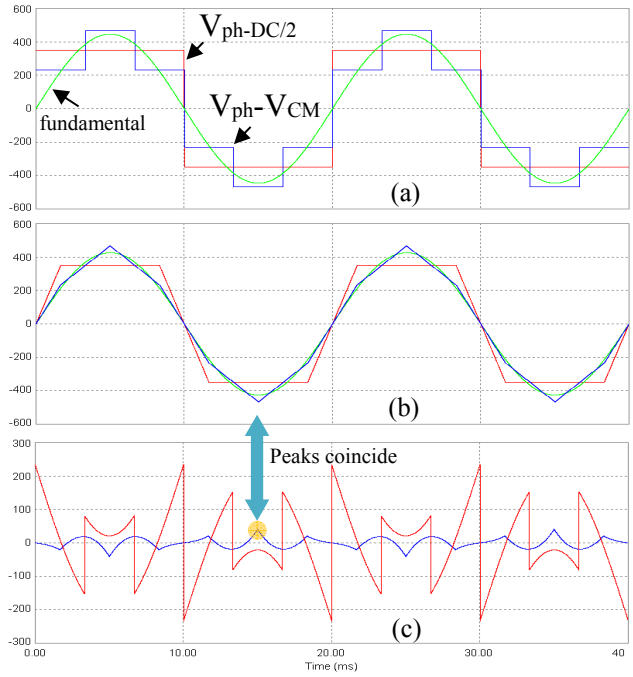

Fig. 2. a-b) Fundamental output voltage component (green), Phase to mid-DC-link output voltage (red) and output phase voltage without common mode voltage component (blue) for the a) six pulse (square wave) VSI; b) VSI with single leg commutating (trapezoidal); c) comparison of residual harmonic phase voltage to be synthetized by an auxiliary inverter.

Multiple hardware solutions can be imagined to take advantage of the idea to use series active filters to correct the residual harmonic voltages. In [6], a solution to use an H-bridge inverter in the DC-link to compensate the magnitude ripple caused by removing the zero states from the SVM pattern was proposed. The series connected H-bridge inverter in the DC-link was also used in conjunction with a 2-stage matrix converter to increase the voltage transfer ratio and improve the robustness to supply unbalance [7]-[8]. In this paper, the connection of the auxiliary inverters in the AC output side of the main VSI will be explored. First, the use of

AC-chopper cells [9] supplied via transformers as proposed in [10] and depicted in Fig. 3a will be investigated. This may in fact be a viable solution for substations that interconnect AC distribution systems to HVDC transmission systems. Then the use of three H-bridge inverters shown in Fig. 3b will be investigated.

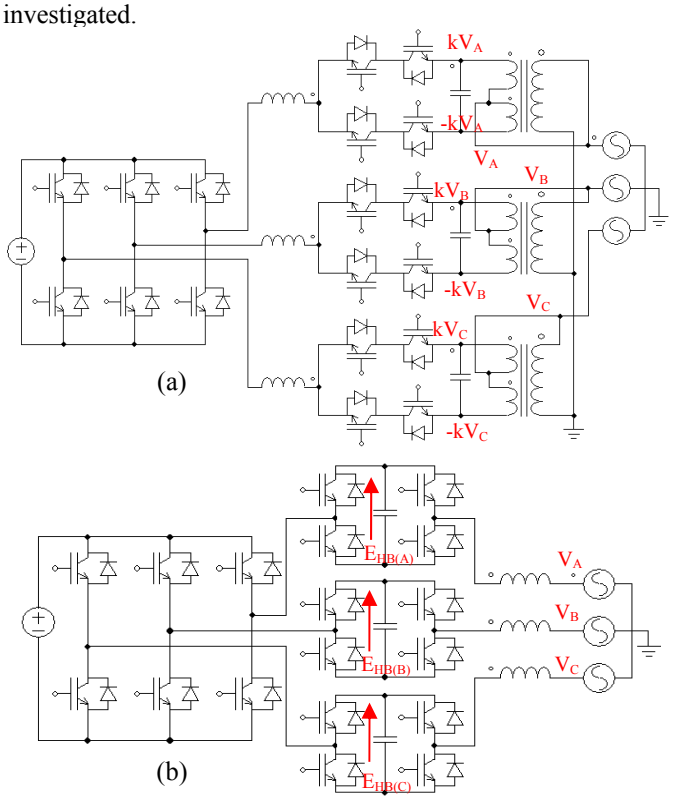

Fig. 3. Hybrid converter topologies using a main VSI with a single switching leg and a) AC choppers; b) H-bridge inverters used as auxiliary inverters.

IV. Modulation of the Auxiliary AC Chopper to Mitigate the Distortion of the Main VSI

In the previous section, it has been shown that for the trapezoidal waveform, the peak of the residual harmonic signal that needs to be synthetized by the auxiliary inverter coincides with the peak of the fundamental phase voltage. This is why the hybrid inverter topology shown in Fig. 3a consists of an AC chopper that can feed a fraction "k" of the AC source phase voltage in series with the main VSI. Two transformer secondaries (k:1 transformer ratio) are used to make available any half-wave of the sinusoidal wave as needed at any given time. By modulating the two bidirectional switches with a given dutycycle "$d_{aux(x)}$", the required series injected voltage is obtained.

$$V_{ref\_X} = d_{aux(X)} \cdot k \cdot V_X + (1 - d_{aux(X)}) \cdot k \cdot (-V_X) \quad (3)$$

where "X" represents the index of each of the three AC supply phases A, B, C. By knowing V_{ref_X} and the corresponding phase voltage V_X, it is possible to determine the value of the dutycycle for each AC chopper cell:

$$V_{ref\_x}/(k \cdot V_x) + 1 = 2 \cdot d_{aux(X)} \quad (4)$$

$$d_{aux(X)} = (VR_x+1)/2 \text{ , where } VR_x = V_{ref\_x}/(k \cdot V_x) \quad (5)$$

The implementation of the modulation for phase A auxiliary chopper is illustrated in Fig. 4a whilst the resulting AC chopper voltage waveforms (both PWM and also low pass filtered to reveal modulating shape) are shown in Fig. 4b.

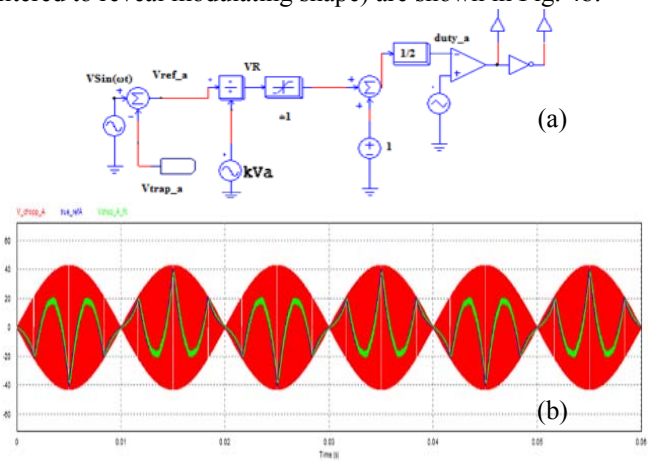

Fig 4. a) Modulation block for phase A Chopper; b) phase A PWM voltage (red), reference waveform (blue), chopper low-pass filtered waveform (green).

The hybrids system consisting of a main VSI powered by a 700V DC-voltage source and using AC choppers fed from $42V_{pk}$ secondary voltage is simulated at the switching frequency of 3kHz for the main inverter whilst the chopper is switched at 35kHz, to reduce delays effects. The hybrid inverter is connected to a passive RL load instead of an AC source because the power flow controller has not been properly developped for reasons that will be explained later.

The simulation results are presented in Fig. 5. Fig. 5a shows the main VSI phase to mid DC-link voltage shows commutation during two sectors per fundamental period, whilst for the rest of the period, it oputputs the possitive or the negative DC-link voltage potential (+/- 350V). The low pass (RC) filtered voltage reveals that the output voltage follows the expected trapezoidal shape. Fig. 5b shows the resulting phase voltage of the hybrid assembly. The visible difference compared to the main VSI voltage is that during the time intervals where the constant DC-link voltage potential would be visible, now the sinusoidal envelope of the AC chopper input voltage is visible. The currents in the passive load (R=100Ω; L= 20mH star connected) are shown in Fig. 5c and are fairly sinusoidal in shape with still some low order harmonic present. The detailed effect of correcting the residual harmonic signal present in the trapezoidal voltage is revealed by analyzing the FFT of the main VSI and the output hybrid converter voltage shown in Table 1. This comparison of the FFT of the two voltages shows that besides the 3rd harmonic voltage which is deliberately left uncompensated to minimize the voltage ratings and stresses in the auxiliary converter, all low order harmonics are successfully compensated by the AC chopper. The main reason why the low order harmonics are not removed completely are the errors in estimating the actual

voltage produced by the main VSI, as a pure trapezoidal wave was used in the compensator. Additional distortion may be due to delays that cause phase errors for the injected auxiliary inverter voltage. Table 1 also summarizes the numerical amplitude of each low order relevant harmonic present in the output of the main VSI, the load and the reference and the actual AC chopper voltages. It can be seen that the chopper is synthetizing well the reference but the errors in harmonic amplitude are smaller at lower order (5^{th}) and increase above 11^{th} order confirming that the main error is probably in the phase shift, more significant at higher frequency. This may be addressed in the future by employing repetitive control.

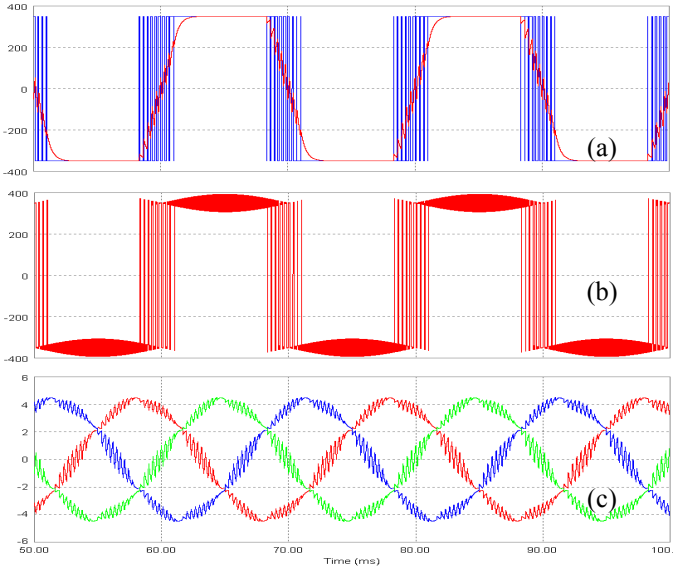

Fig 5. a) Main VSI phase to DC-link midpoint voltage (blue) and the low-pass (RC) filtered (red); b) output phase to DC-link midpoint corrected voltage waveform; c) output currents in a passive RL load.

TABLE I. FFT ANALYSIS OF PHASE A VOLTAGES

Frequency (Hz)	Input Voltage (V)	Output Voltage (V)	Reference Voltage (V)	Chopper Voltage (V)	V_o/V_{in}
50	427.62	427.41	0.045	0.21	0.9995
250	21.35	4.33	17.03	17.06	0.20
350	7.60	1.07	8.67	8.66	0.14
550	8.13	4.83	3.52	3.30	0.59
650	1.37	4.00	2.51	2.68	2.91

In order to provide full power flow control, it is necessary to be able to phase shift the fundamental component of the hybrid converter voltage in respect to the supply voltage, such that the phasorial difference that is equivalent to the voltage drop across the line side inductance, leads to a 90° lagging supply current that matches the desired active and reactive power flow. To achieve this, both the main and the auxiliary inverter need to inject fundamental voltage components in phase (possible, as Vx has same grid voltage phasing) and in quadrature (the current arrangement cannot allow this) to the supply voltage. The main VSI however, can only adjust its relative voltage phase shift compared to the grid voltage, whilst the auxiliary AC chopper, needs to remain locked to the supply voltage as its input voltage is the secondary transformer winding. On the other hand, in order to minimize voltage stress, the peak of the residual harmonic, locked with the trapezoidal signal, needs to meet a sufficiently large transformer secondary voltage to avoid overmodulation. This results in a limitation in the operation of the proposed circuit that is subject to future work. Using H-bridge inverters with floating DC-link capacitors on the other hand, gives a wider degree of freedom therefore these will be used to explore the capability of the hybrid converter to control the power flow.

V. CONTROL OF THE HYBRID CONVERTER USING H-BRIDGE INVERTERS

The use of series connected H-bridge inverters to perform active filtering has been explored in [11]-[12] whilst the use of H-bridge inverters to provide power flow control has been proposed in [13]. In this paper both functionalities will be used. Fig. 6a shows the altered modulation scheme to facilitate the replacement of the AC chopper with the H-bridges.

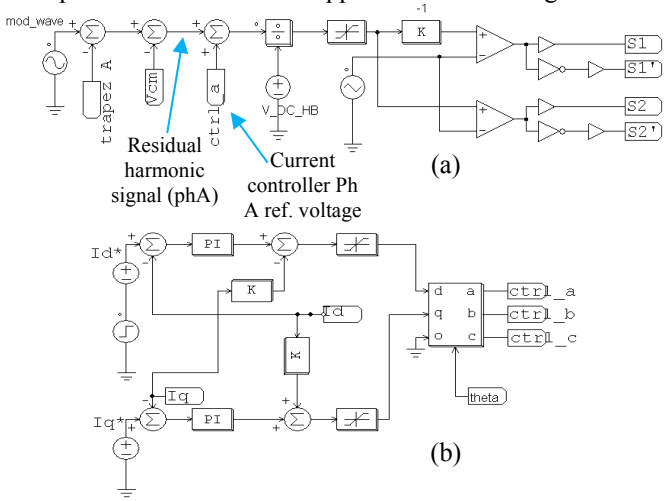

Fig. 6. a) The modulation scheme for the auxiliary H-bridge inverters; b) The decoupled current control implemented in DQ synchronous reference frame

First, the ability of the H-bridge inverters to correct the distortion contained in the trapezoidal voltage synthetized by the main VSI is assessed and the result is shown in Fig. 7. Since a 3-level modulation is employed by the auxiliary H-bridge inverters ($E_{HB(X)}$=42V), the polarity of the residual harmonic signal to be canceled is visible in the output voltage. Even though the injected PWM signal is better synthetized, the quality of the AC currents produced by the hybrid converter voltage in the same RL passive load (R=100Ω; L= 20mH) is similar, since it is dependent on the level of switching ripple produced by the main VSI (V_{dc}=700V) that switches at 3kHz.

In order to control the power flow, a control structure that outputs the fundamental voltage components "ctrl_x" to be injected by the series H-bridge inverters is implemented. This relies on a standard PI current control implemented in the rotating DQ reference frame as shown in Fig. 6b, synchronized with the supply voltage vector.

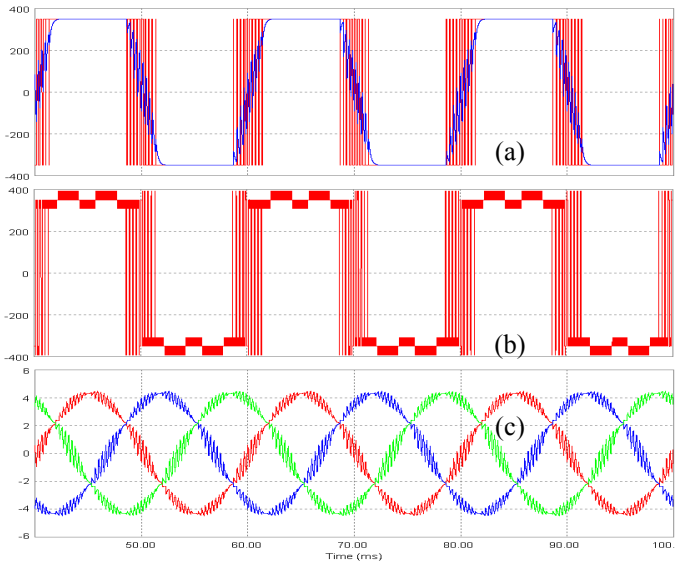

Fig. 7 a) Main VSI phase to DC-link midpoint voltage (blue) and the low-pass (RC) filtered (red); b) output phase to DC-link midpoint corrected voltage waveform; c) output currents in a passive RL load.

In order to assess the performance of the hybrid converter arrangement to control the active and reactive power flow, a step transient response test is carried out. To make sure that the H-bridges have the capability to control the current in the line side inductors (6mH per phase), a higher DC-link voltage ($E_{HB(X)}$=100V) was used for the H-bridge inverters. Fig. 8 shows the simulation results. First step change is commanded at t=50ms for the reactive current to change from 10A to 0A and the response is fast with no notable details. At t=80ms, an active power reversal is commanded (Id= -10A to +10A). Since the current step is significantly larger (20A), it results in a large voltage deviation to be produced and this results in a large deviation of the PI d-current component which raises to 300V. Since the H-bridges cannot synthetize more than 100V peak, the hybrid converter loses momentarily the capability to control the current. This is reflected in a large overshoot in the d-component current and also in a spike in the phase B grid current. An improvement in the grid side currents compared to the passive load is visible which can be explained by the fact that the auxiliary H-bridge inverters switching significantly faster (35kHz), have a current controller capable to react very fast, smoothing in fact part of the switching ripple produced by the main VSI. This may be a feature that is desired in a particular application or may be a feature that needs to be removed, since large current ripples caused by slow converters commutating large voltages, would require similarly large voltage capability in the auxiliary H-bridge inverters to cancel the ripple, since the pk-pk current ripple is dictated by the line inductance and the voltage switched. In other words, the voltage generation capability of the H-bridge needs to be directed to control the target parameters rather than to be wasted on controlling less important variables.

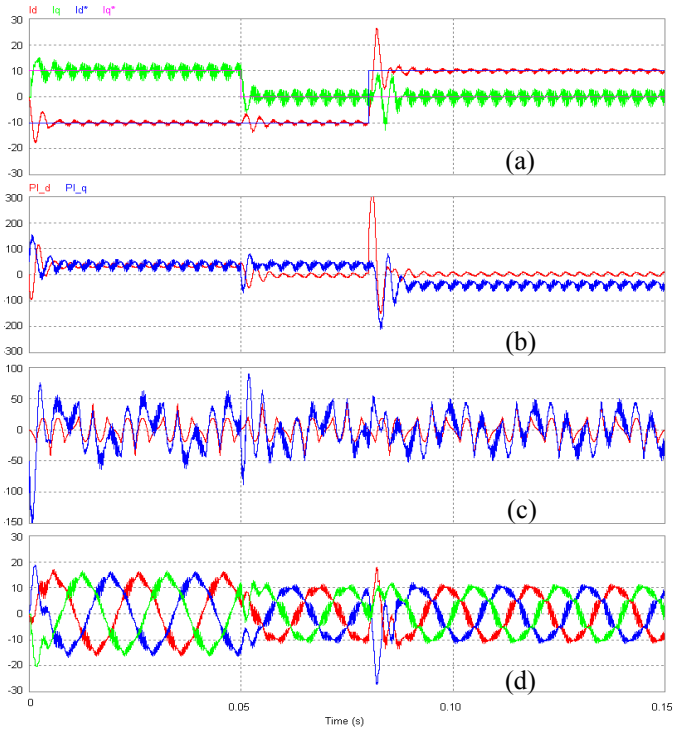

Fig. 8. Transient response of the hybrid converter subject to 10A to 0A Iq step change at t=50ms and -10A to +10A Id step change at t=80ms. a) reference and actual D and Q grid currents; b) ouput of the D and Q PI current controllers; c) reference signal to cancel phase A residual harmonic signal (red) and cummulated with the currnet controller output; d) grid currents.

VI. Synchronising the Switching Pattern of the Auxiliary Inverters

In the implementation proposed above, an unusually high switching frequency was used for the auxiliary inverters, the main reason being the need to minimize the distortion of the output waveform created by the mismatch in main vs auxiliary inverter switching period which can create unwanted inter-harmonics. In [7]-[8], a solution to enable synchronization of switching pulses of hybrid converter was proposed, which enabled the auxiliary inverter to operate with the same switching frequency as the main inverter, resulting in a more realistic switching effort. This requires the auxiliary inverter to perform a full switching cycle within the duration of each given switching state of the main inverter. This is illustrated in Fig. 9 whilst the calculation of the synchronization delay $t_{HB1(X)}$ is calculated based on (1), (2), (5) where x=A,B,C:

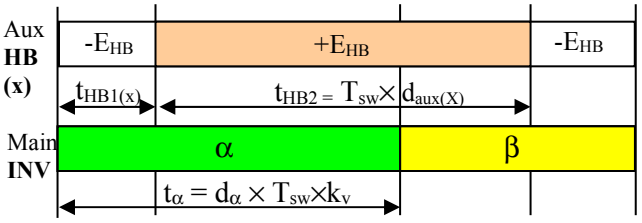

Fig. 9. Switching states combination for the hybrid VSI+series HBs

$$t_{HB1(X)} = d_{\alpha} \cdot T_{sw} \cdot k_v \cdot (1 - d_{aux(X)}) \quad (6)$$

The results of applying this switching pattern is shown in Fig. 10 where both the main and the auxiliary inverters ($E_{HB(X)}$ = 50V) are switching with 3kHz. Fig. 10b shows the reference signal and the low pass filtered of the resulting signal injected by H-bridge inverter of phase A. It can be seen that whilst the basic shape is similar, there is a noticeable delay which means that even though the injected harmonics match the required level (revealed also in Fig. 10e that shows the FFT of the reference and low pass filtered signal injected by the HB), due to the delay (phase shift) this leads to poorer cancelation. The quality of the AC currents produced by the cumulated PWM output voltage (Fig. 10c) into the 100Ω + 20mH passive load is seen in Fig. 10d. Besides the switching ripple, the shape is fairly sinusoidal which means that a significant proportion of the low order harmonics (5^{th}, 7^{th}) have been reduced.

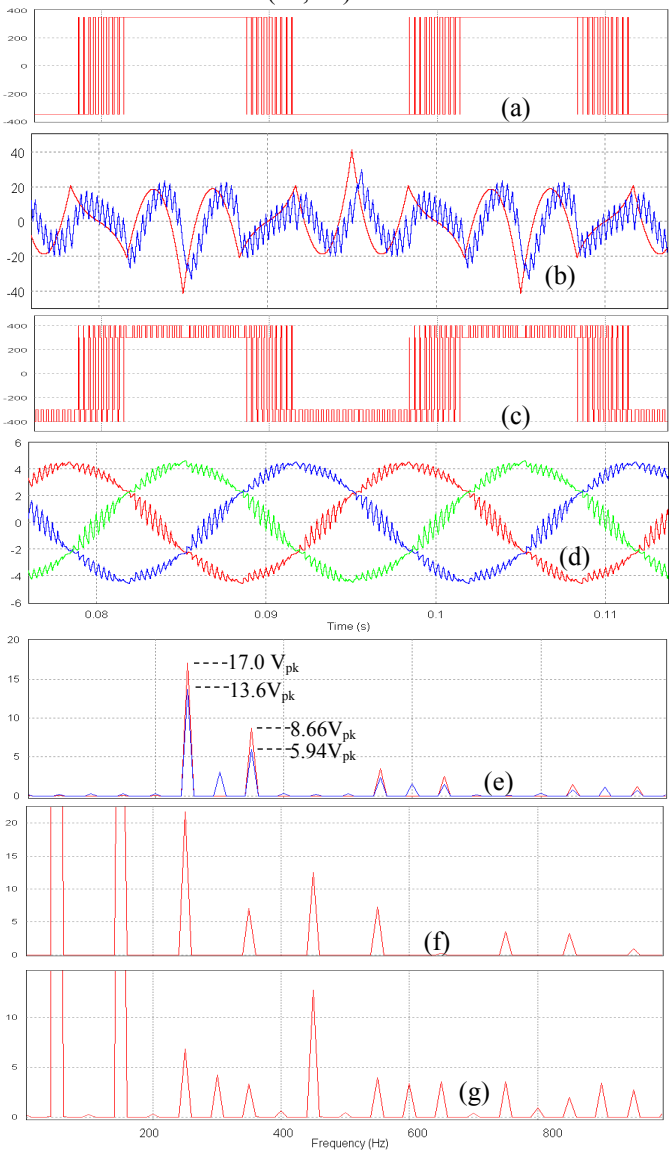

Fig. 10. Hybrid converter using three H-bridge inverters in series with each AC output having synchronized switching: a) main inverter phase voltage; b) reference H-bridge voltage and low pass filtered actual phase A voltage; c) resulting hybrid inverter output phase voltage; d) output currents into a 100Ω + 20mH passive load; e) FFT of b); f) FFT of A; g) FFT of c.

This can also be seen when comparing the FFT of the phase to main DC-link midpoint voltages shown in Fig. 10f and g. One problem still to be solved is the presence of 300Hz multiples that show there are still some problems with the decoupling of modulation of the main inverter and the H-bridge inverters but the resulting harmonics are small (4Vpk).

VII. CONCLUSION

This paper investigated the implementation of two hybrid converter topologies that use a main VSI controlled such that only one of the legs performs PWM switching. The paper evaluates the use of an AC chopper and of H-bridge inverters as auxiliary inverters connected in series with the AC output to correct the resulting distortion but due to the trapezoidal shape, it requires small peak injected voltage (6%). PSIM simulations show the auxiliary inverters are able to improve significantly the shape of the voltage delivered to the load. A limitation in terms of active power flor control is identified for the AC chopper whilst the full active and reactive current/power flow control capability of the hybrid converter using series H-bridge inverters is demonstrated in transient step change tests. Finally, a modulation scheme that minimizes the switching stress of the auxiliary inverters is also proposed allowing them to commutate with the same switching frequency as the main VSI.

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