Fixed Frequency Finite-State Model Predictive Control for Indirect Matrix Converters with Optimal Switching Pattern

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Abstract— **Finite States Model Predictive Control (MPC) has been recently applied to several converters topologies for the many advantages it can provide such as fast dynamics, multi-target control capabilities, easy implementation on digital control board and capability of including constraints in the control law. However, its variable switching frequency and lower steady state waveform quality, with respect to standard control plus modulator systems, represents a limitation to its applicability. Modulated Model Predictive Control (M^2PC) combines all the advantages of the simple concept of MPC together with the fixed switching frequency characteristic of PWM algorithms. In particular this work focuses on the Indirect Matrix Converter (IMC), where the tight coupling between rectifier stage and inverter stage has to be taken into account in the M^2PC design. This paper proposes an M^2PC solution, suitable for IMC, with an optimal switching pattern to emulate the desired waveform quality features of Space Vector Modulation (SVM). In the optimal pattern, the switching sequences of the rectifier stage and inverter stage are rearranged in order to always achieve zero-current switching on the rectifier stage, thus simplifying its commutation strategy. In addition, the optimal pattern enables M^2PC to produce sinusoidal source current, sinusoidal output current and maintain all desirable characteristics of MPC.**

Keywords—Indirect Matrix Converter (IMC), Modulated Model Predictive Control (M^2PC), Switching Pattern

I. INTRODUCTION

Matrix converters have been frequently investigated during the past years for their capability of obtaining direct AC-AC power conversion without the need of an intermediate DC stage. Matrix converters minimize the number of required passives components, thus increasing the converter power density and reliability [1]-[2]. Among all the possible topologies in the matrix converter family, Indirect Matrix Converter (IMC) represents a straight forward solution to obtain direct AC-AC power conversion. In fact, the IMC is composed by a rectifier stage and an inverter stage directly connected together, without dc-link energy storage elements [3]-[5]. However, in order to perform AC commutations on the rectifier stage, bidirectional switches are required [6]. IMC features bidirectional power flow ability, sinusoidal input and output currents, and controllable input power factor. It has been suggested as a potential alternative topology to conventional voltage source AC-AC converters, due to its attractive advantages of more compact size, lighter weight, and longer lifetime [7]. The current research efforts directed to IMC cover control strategies, modulation algorithms, extended topologies and applications [8]-[13].

Compared with the traditional Back-To-Back converter, the IMC requires a higher number of power switches and a direct coupling between the converter input and output is present. As a result, the modulation algorithms and control strategies complexity is increased [13]. Space Vector Modulation (SVM) is widely applied to IMC [14]: in every sampling period, the expected input current vector and output voltage vector are synthesized by multiple basic vectors. However, with the rapid development of digital processors and power devices, SVM used in conjunction with linear controllers is now being challenged by model predictive control (MPC). In fact MPC provides numerous advantages such as the capability of achieving several control targets with a single loop, easy implementation, capability of include constraints in the control system and better dynamic performances [15]. MPC has been used for IMC to obtain sinusoidal input and output currents, control the input reactive power, increase efficiency and reduce common mode voltages [16]-[19]. Considering all the possible switching states of IMC, MPC selects the best one to minimize a cost function in every sampling period. The cost function is usually composed by the difference between the predictions of the system variables to be controlled and their reference values.. However, a critical issue of MPC is that, due to the lack of a modulator, only one switching state is applied to the converter in one sampling period. As a result, compared to conventional PWM algorithms, MPC leads to larger ripple in the system waveforms [20]. Besides, the switching frequency in MPC is variable and harmonics spread in a wide range of frequency [21], which in turn requires the average switching frequency to be much higher than in PWM algorithms in order to achieve similar waveform quality.

With the aim of improving the performance of MPC by incorporating a modulation technique inside the MPC algorithm, the Modulated Model Predictive Control (M^2PC)

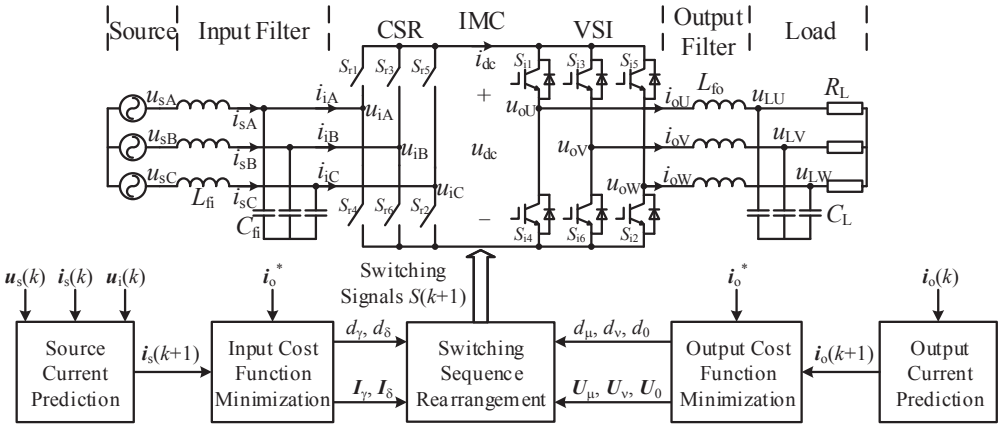

Fig.1 IMC System and Control Block Diagram of the Improved M^{2}PC

concept has been introduced and applied to several power converters structures [22]-[24]. In M^{2}PC, two or more switching states are selected by the cost function minimization algorithm and applied to the converter within a fixed switching cycle with appropriately chosen application times. In such way the switching frequency of M^{2}PC is kept constant, thus improving waveform quality.

In [25] M^{2}PC has been applied to the IMC. However, since the switching sequences of rectifier stage and inverter stages are implemented separately, the results show input and output current distortions. Focusing on the M^{2}PC for IMC, this paper introduces substantial improvement to the switching pattern presented in [25] to obtain largely enhanced control performances, which are validated by simulation and experimental results.

II. Converter Description

This section describes the implemented IMC system where the M^{2}PC technique is applied. The IMC consists of a current source rectifier (CSR) and a voltage source inverter (VSI), as shown in Fig.1. The rectifier stage and inverter stage are coupled by a common virtual DC-link.

For the rectifier stage, its output voltage, i.e. the dc-link voltage u_{dc}, are defined by the switches state accordingly with the following expression

$$u_{dc} = \begin{bmatrix} S_{r1} - S_{r4} & S_{r3} - S_{r6} & S_{r5} - S_{r2} \end{bmatrix} \boldsymbol{u}_i \tag{1}$$

where S_{ri} ($i \in \{1,2,3,4,5,6\}$) represents the switching state of the six switches in the rectifier stage, whose value is 1 or 0 for closed state and open state respectively; $\boldsymbol{u}_i$ is the input voltage vector. Correspondingly, the input current vector $\boldsymbol{i}_i$ is calculated by

$$\boldsymbol{i}_i = \begin{bmatrix} S_{r1} - S_{r4} & S_{r3} - S_{r6} & S_{r5} - S_{r2} \end{bmatrix}^T i_{dc} \tag{2}$$

where i_{dc} is the dc-link current.

Similarly, the equations for the inverter stage are defined as follows

$$i_{dc} = \begin{bmatrix} S_{i1} - S_{i4} & S_{i3} - S_{i6} & S_{i5} - S_{i2} \end{bmatrix} \boldsymbol{i}_o \tag{3}$$

$$\boldsymbol{u}_o = \begin{bmatrix} S_{i1} - S_{i4} & S_{i3} - S_{i6} & S_{i5} - S_{i2} \end{bmatrix}^T u_{dc} \tag{4}$$

where $\boldsymbol{u}_o$ and $\boldsymbol{i}_o$ are the output voltage vector and output current vector respectively.

In order to properly operate the IMC requires a capacitive input filter on the CSR and an inductive output filter on the VSI. However in order to improve the waveforms quality usually LC filter are preferred.

For the safety operation of IMC, the following three conditions are mandatory to be met:

- Any two input phases cannot be short circuited.
- Any one output phase cannot be open circuited.
- The dc-link voltage must be positive.

According to these constraints, there are 9 valid switching states for the rectifier stage and 8 valid switching states for the inverter stage [25].

III. M^{2}PC Design

As shown in Fig. 1, the M^{2}PC algorithm can be divided in five sections. Initially, source and output current prediction generate $\boldsymbol{i}_s(k+1)$ and $\boldsymbol{i}_o(k+1)$ which are the predicted input and output currents at the $(k+1)^{th}$ sampling period respectively; next the input/output cost function minimization algorithms decide which switching states will be applied to the IMC. Then, the switching sequence rearrangement allocates the time of each states applied to IMC. It can be seen in Fig. 1 that M^{2}PC selects two switching states for rectifier stage and three switching states for the inverter stage in one sampling period. This is a procedure, similar to PWM algorithms, while traditional MPC generates only one switching state for each stage, as presented in [15]. The M^{2}PC with optimal switching pattern is presented in details in the following subsections.

A. Input and Output Current Prediction

The discrete state-space equation for the input side, with source current $\boldsymbol{i}_s$ and input voltage $\boldsymbol{u}_i$ as state variables, is obtained from Fig. 1:

$$\begin{bmatrix} \boldsymbol{i}_s(k+1) \\ \boldsymbol{u}_i(k+1) \end{bmatrix} = \Phi_i \begin{bmatrix} \boldsymbol{i}_s(k) \\ \boldsymbol{u}_i(k) \end{bmatrix} + \Gamma_i \begin{bmatrix} \boldsymbol{u}_s(k) \\ \boldsymbol{i}_i(k) \end{bmatrix} \tag{5}$$

where matrices Φ_i and Γ_i are calculated by[16]:

$$\Phi_i = e^{A_i T_s},\ \Gamma_i = A_i^{-1}(\Phi_i - I) B_i \tag{6}$$

$$A_i = \begin{bmatrix} -R_f / L_f & -1/L_f \\ 1/C_f & 0 \end{bmatrix},\ B_i = \begin{bmatrix} 1/L_f & 0 \\ 0 & -1/C_f \end{bmatrix} \tag{7}$$

L_f, R_f, and C_f are the parameters of the input filter; T_s is the sampling time.

Similarly, the discrete state-space equation for the output stage, having the output current $\boldsymbol{i}_o$ as the single state variable, is

$$\boldsymbol{i}_o(k+1) = \Phi_o \boldsymbol{i}_o(k) + \Gamma_o \boldsymbol{u}_o(k) \tag{8}$$

where

$$\Phi_o = e^{-\frac{R_o}{L_o}T_s},\ \Gamma_o = -\frac{1}{R_o}(\Phi_o - 1) \tag{9}$$

where L_o and R_o represents the output filter inductance and load resistance, respectively. Equations (5) and (8) are then used to predict the values of the state variables at the k+1 sampling period and are calculated for every possible switching states of rectifier stage and inverter stages.

B. Cost Function Minimization

The cost function g for each switching state is defined as the square of the difference between the predicted values and the reference values for input and output currents:

$$g = \left| \boldsymbol{i}^* - \boldsymbol{i}(k+1) \right|^2 \tag{10}$$

This definition is suitable for all the switching states of both the rectifier stage and inverter stage.

In the implementation of the control algorithm, the M^{2}PC is first executed for the rectifier stage. In this stage, $g_{i\gamma}$ is defined as the cost function of one switching state $\boldsymbol{I}_\gamma$ and $g_{i\delta}$ as the cost function of the next adjacent switching state $\boldsymbol{I}_\delta$ (i.e. only one device commutation separates the states $\boldsymbol{I}_\gamma$ and $\boldsymbol{I}_\delta$) [25]. The values $g_{i\gamma}$ and $g_{i\delta}$ are calculated according to (10) considering the two states $\boldsymbol{I}_\gamma$ and $\boldsymbol{I}_\delta$ respectively. Therefore the cost function for the rectifier stage is

$$g_i = \frac{g_{i\gamma} g_{i\delta}}{g_{i\gamma} + g_{i\delta}} \tag{11}$$

The duty cycles within a switching period associated with $\boldsymbol{I}_\gamma$ and $\boldsymbol{I}_\delta$ applied to the rectifier stage are

$$d_{i\gamma} = \frac{g_{i\delta}}{g_{i\gamma} + g_{i\delta}},\ d_{i\delta} = \frac{g_{i\gamma}}{g_{i\gamma} + g_{i\delta}} = 1 - d_{i\gamma} \tag{12}$$

Hence the best couple of adjacent switching states $\boldsymbol{I}_\gamma$ and $\boldsymbol{I}_\delta$ of the rectifier stage are selected to minimize g_i shown in (11), and then their duty cycles can be calculated using (12).

From the control of the rectifier stage, the average dc-link voltage required by the control of the inverter stage is also obtained:

$$u_{dc} = d_{i\gamma} u_{dc\gamma} + d_{i\delta} u_{dc\delta} \tag{13}$$

where $u_{dc\gamma}$ and $u_{dc\delta}$ are the corresponding dc-link voltages when state $\boldsymbol{I}_\gamma$ and $\boldsymbol{I}_\delta$ are applied to the rectifier stage separately. The value of dc-link voltage corresponding to each state can be found from [25].

After the implementation of the control of the rectifier stage, the control of the inverter stage is implemented in a similar way. The cost functions of two adjacent switching states $\boldsymbol{U}_\mu$ and $\boldsymbol{U}_\nu$ plus a zero voltage state $\boldsymbol{U}_0$ are calculated according to (10) and expressed as $g_{u\mu}$, g_{uv}, and g_{u0} respectively. The cost function for the inverter stage is defined as:

$$g_u = \frac{g_{u\mu} g_{uv} g_{u0}}{g_{u\mu} g_{uv} + g_{uv} g_{u0} + g_{u\mu} g_{u0}} \tag{14}$$

The associated duty cycles of $\boldsymbol{U}_\mu$, $\boldsymbol{U}_\nu$, and $\boldsymbol{U}_0$ are expressed as

$$\begin{cases} d_{u\mu} = \dfrac{g_{uv} g_{u0}}{g_{u\mu} g_{uv} + g_{uv} g_{u0} + g_{u\mu} g_{u0}} \\ d_{uv} = \dfrac{g_{u\mu} g_{u0}}{g_{u\mu} g_{uv} + g_{uv} g_{u0} + g_{u\mu} g_{u0}} \\ d_{u0} = \dfrac{g_{u\mu} g_{uv}}{g_{u\mu} g_{uv} + g_{uv} g_{u0} + g_{u\mu} g_{u0}} = 1 - d_{u\mu} - d_{uv} \end{cases} \tag{15}$$

By minimizing g_u shown in eq. (14), the best couple of adjacent switching states $\boldsymbol{U}_\mu$ and $\boldsymbol{U}_\nu$ in the inverter stage are selected, with the zero voltage state $\boldsymbol{U}_0$ selected to minimize the number of devices commutations. Duty cycles of $\boldsymbol{U}_\mu$, $\boldsymbol{U}_\nu$, and $\boldsymbol{U}_0$ are then calculated using eq. (15).

The control of the inverter stage also generates the average dc-link current i_{dc} to be used in the control of the rectifier stage. Though i_{dc} can be calculated as in (13), it can also be expressed as in eq. (16) in order to reduce the control computational burden

$$i_{dc} = \frac{P_o^*}{u_{dc}} \tag{16}$$

where u_{dc} is obtained by (13) and P_o^* is the reference value of the output active power, and is calculated as in eq. (17) from the reference value of the output current amplitude I_{om}^*.

$$P_o^* = 1.5 I_{om}^* R_o \tag{17}$$

Eq. (16) derives from power balance considerations on the IMC converter. In fact, since the IMC does not presents any energy storage elements on the DC-link, the input active power, DC-link power, output active power are always equal to each other, assuming lossless power devices.

Since the control of the rectifier stage and the inverter stage are executed sequentially, one sample delay appears on the

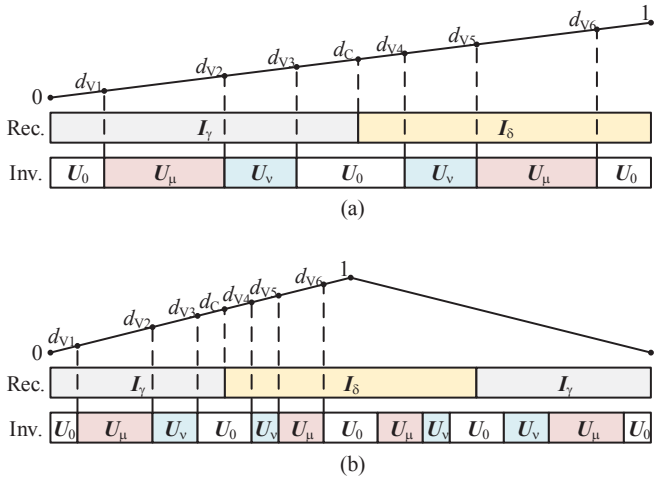

Fig. 2 Switching pattern of IMC with M^{2}PC: (a) existing M^{2}PC [25]; (b) Optimal

calculation of i_{dc}. In fact, while the value of u_{dc} is calculated by the rectifier stage controller and instantaneously applied to the inverter stage control, the value of i_{dc} is calculated by the inverter stage controller and applied to the rectifier stage control at the next sampling period. This approximation may degrade the input performances, even if its effect may be considered negligible for the considered sampling frequency.

C. Optimal Switching Pattern

Due to the absence of dc-link energy storage elements, the switching sequences of the rectifier stage and inverter stage should be coupled, in order to obtain the expected input and output currents. In the M^{2}PC-IMC switching pattern, presented in [25] and illustrated in Fig. 2(a), the switching states of the rectifier stage change only once while those of the inverter stage change six times within one sampling period. The duty cycle d_C associated with the rectifier stage is identified by the duty cycle obtained by the rectifier stage cost function minimization, namely

$$d_C = d_{i\gamma} \tag{18}$$

The duty cycles d_{V1}~d_{V6} associated with the inverter stage are

$$\begin{cases} d_{V1} = d_{u0}/4 \\ d_{V2} = d_{V1} + d_{u\mu}/2 \\ d_{V3} = d_{V2} + d_{uv}/2 \\ d_{V4} = d_{V3} + 2d_{V1} \\ d_{V5} = d_{V4} + d_{uv}/2 \\ d_{V6} = d_{V5} + d_{u\mu}/2 \end{cases} \tag{19}$$

As it is shown in Fig. 2 (a), (18), and (19), the switching sequence of the rectifier stage does not depend on from that of the inverter stage one, and the application times of the three switching states of the inverter stage are allocated symmetrically to the first half and the second half of the sequence period.

Since the two stages are not decoupled due to the absence of a dc-link capacitor, this pattern has two drawbacks. On one hand, the commutation of the rectifier stage does not always happen when the dc-link current i_{dc} is zero (i.e. when the switching state of the inverter stage is $\boldsymbol{U}_0$). For example, if the calculated d_C is larger than d_{V1} but lower than d_{V2}, the commutation of the rectifier stage happens when i_{dc} is not zero since $\boldsymbol{U}_\mu$ is applied to the inverter stage at that moment. Therefore, the implementation of this pattern needs to adopt a complicated commutation strategy (e.g. four-step commutation) for the rectifier stage. On the other hand, the M^{2}PC is separately applied to the two stages. This operation assumes that both dc-link voltage u_{dc} and current i_{dc} are constant throughout the whole sampling period. Nevertheless, the waveforms of u_{dc} and i_{dc} are segments decided by the switching states of the two stages. As a result, the input and output currents will be distorted due to the time-varying u_{dc} and i_{dc}.

An optimal pattern solution that solves the above mentioned issues is the one shown in Fib. 2(b). In this optimal pattern, the switching sequences of the two stages are closely coordinated. The application times of the three switching states of inverter stage are allocated proportionally to the application times of the states applied to the rectifier stage; hence proportionally to $\boldsymbol{I}_\gamma$ in the first part of the switching cycle and to $\boldsymbol{I}_\delta$ in the second part of the switching cycle. The duty cycles d_{V1}~d_{V6} associated with the states of the inverter stage are calculated by:

$$\begin{cases} d_{V1} = d_{u0}/4 \\ d_{V2} = d_{V1} + d_{i\gamma} d_{u\mu} \\ d_{V3} = d_{V2} + d_{i\gamma} d_{uv} \\ d_{V4} = d_{V3} + 2d_{V1} \\ d_{V5} = d_{V4} + d_{i\delta} d_{uv} \\ d_{V6} = d_{V5} + d_{i\delta} d_{u\mu} \end{cases} \tag{20}$$

And the duty cycle d_C associated with the commutation of the rectifier stage is equal to

$$d_C = d_{V3} + d_{V1} \tag{21}$$

As it is shown in Fig. 2, the optimal pattern is symmetrical, which helps to achieve a switching frequency which is two times the control sampling frequency without increasing the computational burden, and to obtain better waveform quality.

It is clear from (20) and (21) that d_C is always larger than d_{V3} and smaller than d_{V4}. Therefore, the state commutation of the rectifier stage always happens when the dc-link current i_{dc} is zero, since the zero voltage stage $\boldsymbol{U}_0$ is applied to the inverter stage at that moment. This means that zero-current switching is guaranteed for the rectifier stage, simplifying the commutation strategy of the IMC. In addition, similar to the switching pattern in conventional PWM algorithms [18], this pattern adjusts the time of every switching state applied to the inverter stage according to the switching state of the rectifier stage.

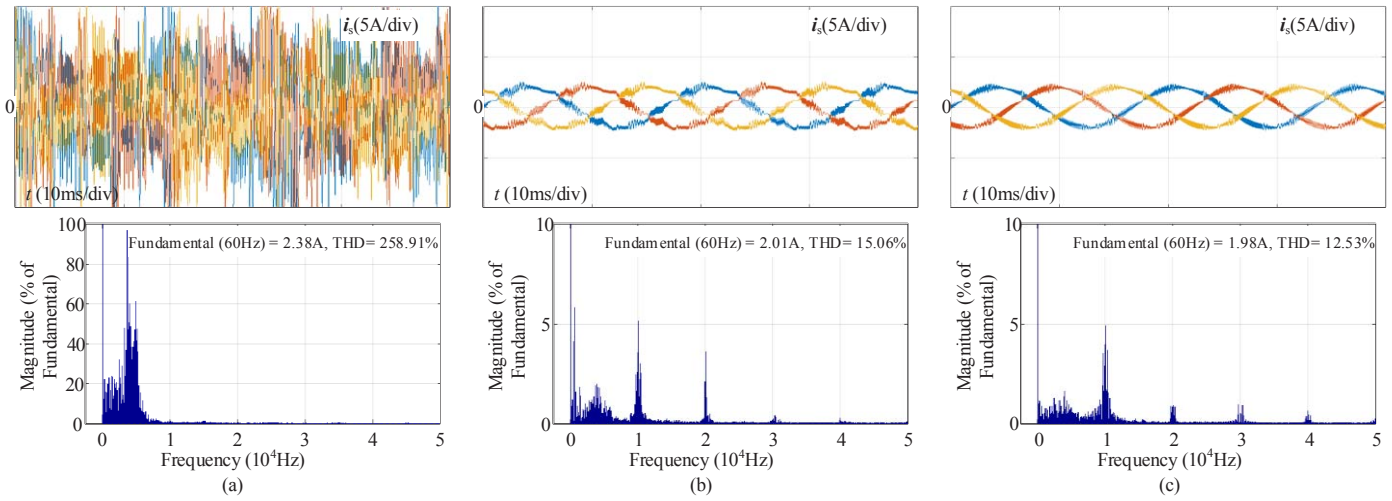

Fig. 3 Waveforms of source current $\boldsymbol{i}_s$ and its FFT result: (a) with the traditional MPC; (b) with the existing M^{2}PC [25]; (c) with the optimal M^{2}PC.

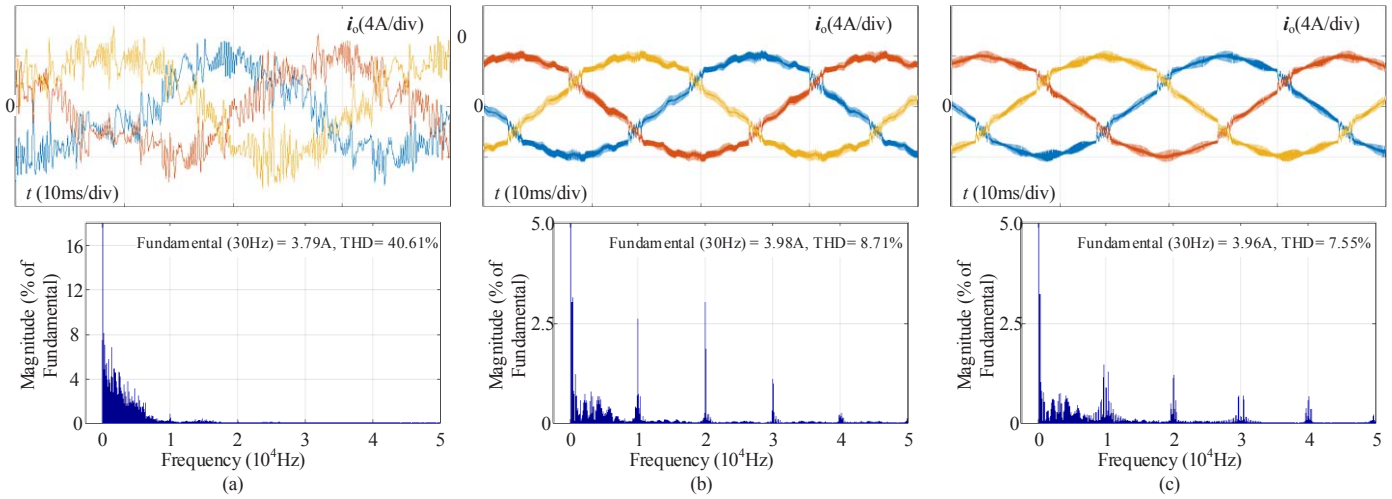

Fig. 4 Waveforms of output current $\boldsymbol{i}_o$ and its FFT result: (a) with the traditional MPC; (b) with the existing M^{2}PC [25]; (c) with the optimal M^{2}PC.

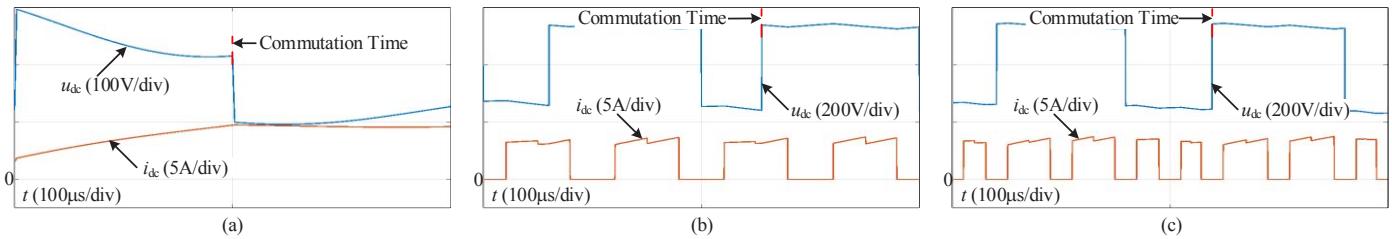

Fig. 5 Waveforms of dc-link voltage u_{dc} and current i_{dc}: (a) with the traditional MPC; (b) with the existing M^{2}PC [25]; (c) with the optimal M^{2}PC.

Only the average voltage produced by the rectifier stage is required to be considered in the M^{2}PC of the inverter stage, and only the average current produced by the inverter stage is required to be considered in the M^{2}PC of the rectifier stage. These patterns ensure that u_{dc} and i_{dc} are constant in order to control the two stages independently and sinusoidal input and output currents are obtained.

IV. Simulation Results

Simulation tests using Matlab/Simulink have been carried out to compare the performance of the M^{2}PC with optimal switching pattern with the existing one presented in [25] and the traditional MPC [16]. The parameters of the simulation model are shown in Table I.

Table I Simulation Parameters

Source	U_s=110V, f_i=60Hz
Input LC Filter	L_f=145μH, C_f=20μF, R_f=0.4Ω
Load	L_o=3mH, R_o=20Ω
Output Current Reference	I_{om}^*=4A, f_o=30Hz
Sampling Time	T_s=100μs

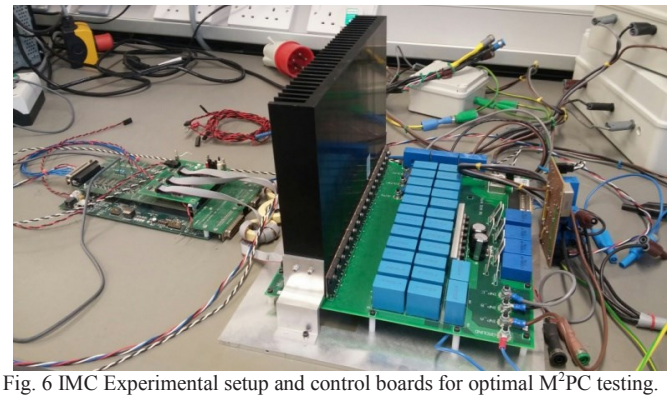

Fig. 6 IMC Experimental setup and control boards for optimal M^{2}PC testing.

The obtained source currents $\boldsymbol{i}_s$ and its FFT are shown in Fig. 3. It is clear from Fig. 3 that $\boldsymbol{i}_s$ is severely distorted when using the traditional MPC working under a relative low sampling frequency (10kHz). By using the existing M^{2}PC, the THD of $\boldsymbol{i}_s$ is reduced to 15.06% while, with the optimal M^{2}PC, the waveform quality of the source currents $\boldsymbol{i}_s$ is further improved, with THD lowered to 12.53% and low-order harmonics suppressed. Similar conclusions can be drawn from the waveforms of output current $\boldsymbol{i}_o$ and its FFT which are shown in Fig. 4. Compared with the traditional MPC and the existing M^{2}PC, the optimal M^{2}PC helps to achieve better waveform quality also on the inverter stage, where the output currents THD is reduced to 7.55%. In addition, the waveforms of dc-link voltage u_{dc} and current i_{dc} are shown in Fig. 5. The commutation of u_{dc} represents the switching state change of the rectifier stage. As illustrated earlier, with the traditional MPC or existing M^{2}PC, it is possible for the rectifier stage to change its switching state when i_{dc} is nonzero. On the contrary, with the optimal M^{2}PC, the commutation of u_{dc} always occurs when i_{dc} is zero, indicating that zero-current switching of the rectifier stage is ensured.

V. Experimental Results

The M^{2}PC with optimal switching pattern is further evaluated experimentally on the prototype shown in Fig. 6. The major parameters of the prototype are the same of the simulation parameters shown in Table I. In addition to the input filter, an EMI filter capacitor is installed at the output of the AC source. More details about the EMI filter can found in [26]. The scheme is implemented on a Spectrum Digital control board featuring a Texas Instruments C6713 DSP together with a ProAsic 3 FPGA.

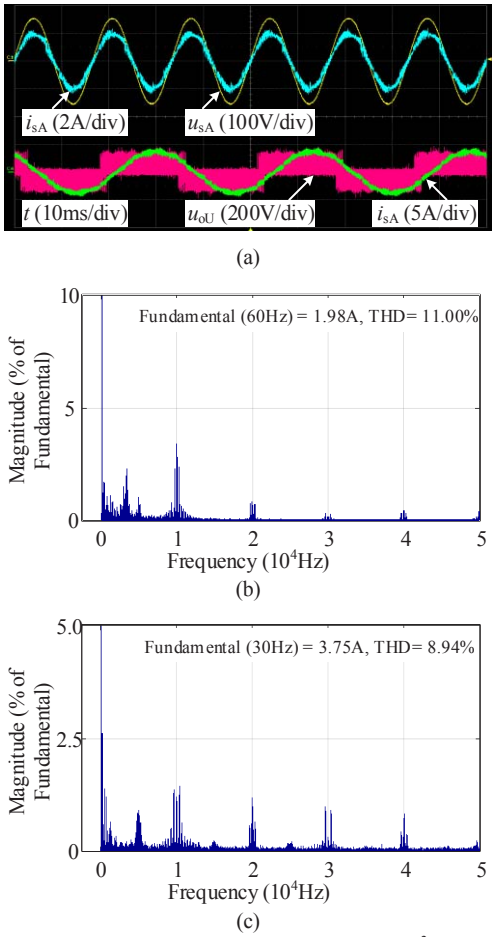

Fig. 7 Experimental results of IMC with the optimal M^{2}PC, where output current amplitude reference is 4A and output frequency is 30Hz: (a) Waveforms of source voltage (u_{sA}), source current (i_{sA}), output line voltage (u_{oUV}), and output current (i_{oU}); (b) Spectrum distribution of i_{sA}; (c) Spectrum distribution of i_{oU}.

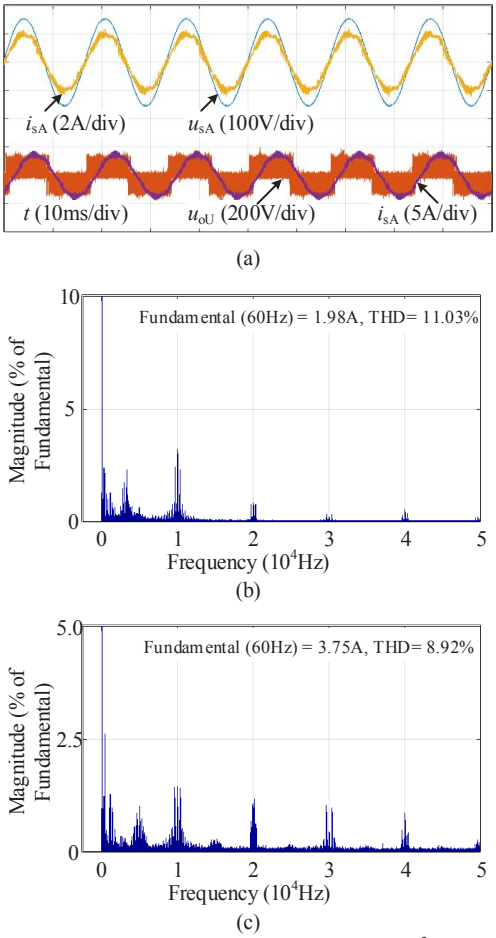

Fig. 8 Experimental results of IMC with the optimal M^{2}PC, where output current amplitude reference is 4A and output frequency is 60Hz: (a) Waveforms of source voltage (u_{sA}), source current (i_{sA}), output line voltage (u_{oUV}), and output current (i_{oU}); (b) Spectrum distribution of i_{sA}; (c) Spectrum distribution of i_{oU}.

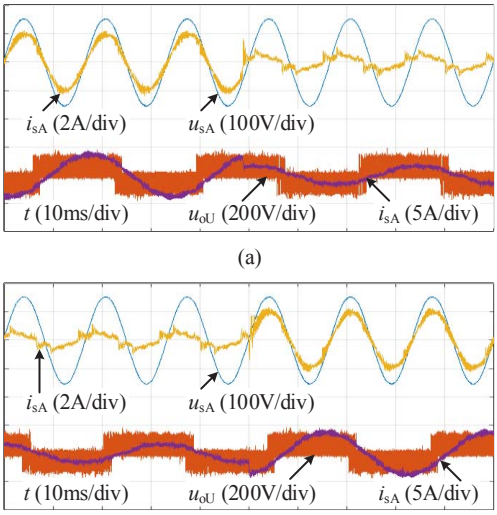

Fig. 9 Experimental results of IMC with the optimal M^{2}PC, where the reference value I_{om}^* of output current amplitude reference steps between 2A and 4A and output frequency keeps at 30Hz: (a) I_{om}^* steps from 4A down to 2A; (b) I_{om}^* steps from 2A up to 4A.

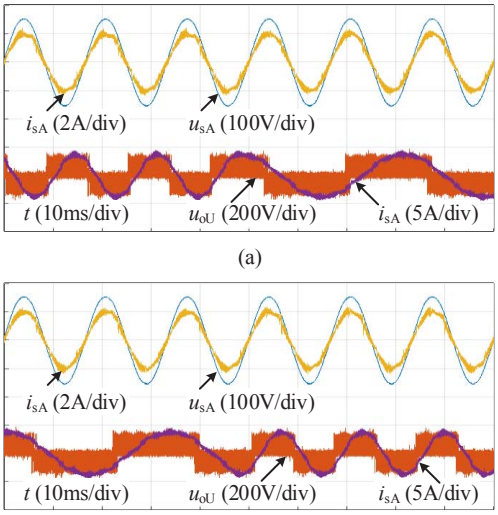

Fig. 10 Experimental results of IMC with the optimal M^{2}PC, where the output frequency f_o steps between 30Hz and 60Hz and the output current amplitude reference keeps at 4A: (a) f_o steps from 60Hz down to 30Hz; (b) f_o steps from 30Hz up to 60Hz.

Firstly, the steady-state performance is evaluated with reference output current amplitude set to 4A and the output frequency set to 30Hz. The obtained experimental result is illustrated in Fig. 7. From Fig. 7(a), it can be found that the source current is in phase with the source voltage, proving that unit power factor operation is achieved. Moreover, both the source current and output current are sinusoidal, with spectrum shown in Fig. 7(b) and Fig. 7(c). By comparing Fig. 7(b) and Fig. 3(c) and comparing Fig. 7(c) and Fig. 4(c), it can be concluded that source current and output current harmonic spectrum validate the simulation results. However the output current first harmonic amplitude is 3.75A, presenting a steady state error of 6.25%. This is a common problem related with model based control techniques, where the inevitable inaccuracies of the system model results in a steady-state error on the controlled variables. Regarding the harmonic content of the source current around the sampling frequency (10kHz), it can be noted a discrepancy between simulation and experimental results. This difference is related with the EMI filter on the input side, which helps to attenuate the high-order harmonics around the switching frequency and is not included in the discretized model used for control design.

In the second set of results, the output current frequency is set to 60Hz, while the other control parameters remain the same as in the previous case. The obtained experimental result is shown in Fig. 7 and Fig. 8 where it can be noted that the source and output current harmonic distribution present minimal variation when the output current frequency varies, resulting in stable control performances for a wide variations of the output current frequency.

Finally, the dynamic performances are evaluated with step changes of both output current amplitude and frequency; these results are shown in Fig. 9 and Fig. 10, respectively. As expected, the control presents a fast dynamic response on both input and output currents.

VI. Conclusion

A fixed switching frequency Finite-States Model Predictive Control, named Modulated Model Predictive Control (M^{2}PC) with optimal switching pattern has been proposed in this paper for indirect matrix converters. Compared with the existing solution and traditional MPC, the proposed approach is demonstrated by simulation results to have sustantial advantages. On one hand, zero-current switching of the rectifier stage is achieved, which benefits simplifying the commutation strategy of IMC in practical implementations. On the other hand, the control performance of M^{2}PC is improved dramatically. Both sinusoidal source current and sinusoidal output current are obtained, with control accuracy largely improved. The research of this paper makes M^{2}PC more competitive with respect to conventional PWM algorithms when applied to IMC. The satisfactory steady-state and dynamic performance of this M^{2}PC is verified both by simulation and experimental results.

M^{2}PC retains all the desirable advantages of MPC [22], such as fast dynamic performance and multi-objective control. Besides, the advantages of using a PWM scheme, such as a fixed switching frequency, are obtained with optimal M^{2}PC. From such considerations, M^{2}PC can be regarded as the beneficial combination of MPC and PWM algorithms.

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