

Analysis of Hybrid Energy Storage Systems with DC Link Fault Ride-Through Capability

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Abstract—In this work, a Fault Ride-Through control scheme for a non-isolated power topology for Hybrid Energy Storage Systems in a DC microgrid is presented. The Hybrid System is created from a Lithium-Ion Battery and a Supercapacitor Module coordinated to achieve a high-energy and high-power storage system; it is connected to a DC link to interface to the outer system. The power topology under consideration is based on the buck-boost bidirectional converter, and it is controlled through a bespoke modulation scheme in order to obtain low losses in nominal operation. The operation of the proposed control during a DC link short-circuit failure is shown as well as a modification to the standard control in order to achieve Fault Ride-Through once the fault is over. The operation of the converter is theoretically developed and it is verified through simulation and experimental validation.

Keywords—hybrid; Energy Storage System; buck-boost converter; Fault Ride-Through capability;

I. INTRODUCTION

The simplest topology for interfacing the Energy Storage devices in Hybrid Energy Storage Systems (HESS) to a DC microgrid is the direct connection of two parallel bidirectional boost converters to the DC link, as shown in Fig. 1. This is a cost-effective and reliable solution for low-to-medium power range applications, as the number of elements and devices is relatively low [1]–[7]. This solution is valid if galvanic isolation is not a requirement. The case studied here considers the simple parallel connection of two distinct Energy Storage devices. One port consists of a Lithium-Ion Battery (LIB), which will provide a high energy density with slow dynamic response. The other port interfaces to a Supercapacitor Module (SM) intended to support a high power density and faster dynamic response [1]–[8]. Therefore, provided that the control strategy is managed correctly, the resulting HESS has a better overall performance than either of the individual systems, allowing for a sustained, high-power high-dynamic performance of the storage system, and potentially a longer battery lifetime.

In addition to the lack of galvanic isolation, a major disadvantage of this system is its sensitivity to short circuit faults on the DC link. If a short circuit occurs, the current drawn from

both the LIB and the SM will increase without control, as the anti-parallel diodes of the upper switches in the legs of the boost converters would allow large short-circuit currents. This will cause damage to the inductors, the storage devices (LIB and SM), and the switches themselves. This paper describes a new circuit and control topology which will limit operation during DC side short circuit faults and can also recover quickly once the fault has been cleared.

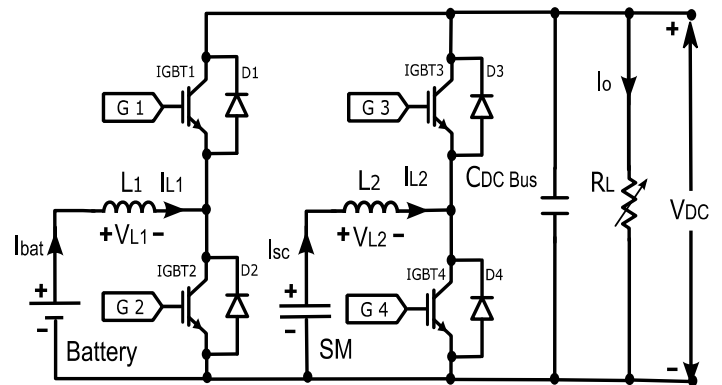


Fig. 1. Two parallel bidirectional boost converters connected to Lithium Ion Battery (LIB) and Supercapacitor Module (SM) and sharing the DC link.

II. FAULT-TOLERANT TOPOLOGIES

The solution to the DC link fault ride through problem is the connection of a device that is able to limit/interrupt the fault currents coming from the storage units. One option is to connect switches in series with the storage units and the inductors of the converters (see Fig. 2). These switches can be opened during the fault in order to prevent the LIB and SM short-circuit currents. In addition, in order to allow a discharge path for any current flowing through the inductors when the series switches are opened, additional free-wheeling switches for each leg are required. Otherwise, a voltage spike will occur, causing arcing or even destruction of the switches. This yields a final configuration of two parallel bidirectional buck-boost converters, as shown in Fig. 3.

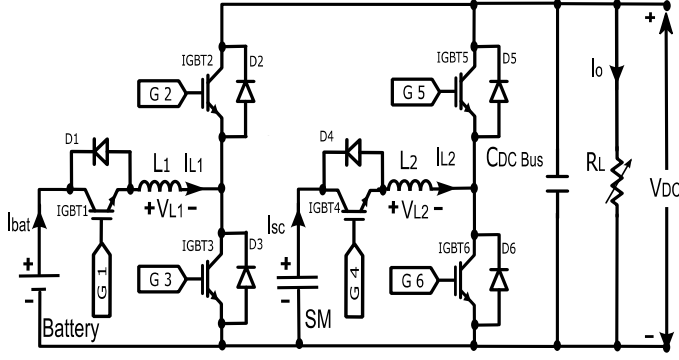


Fig. 2. Two parallel bidirectional boost converters with a switch in series between the storage devices and inductors.

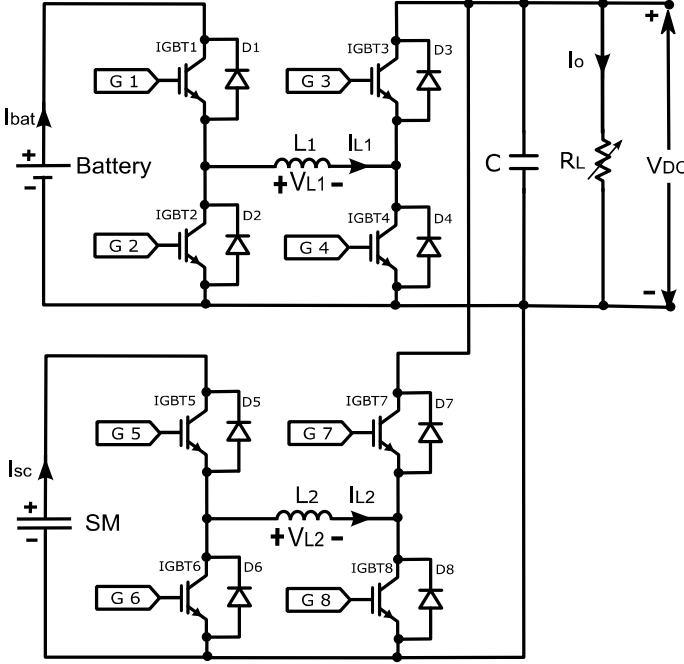


Fig. 3. Two parallel bidirectional buck-boost converters connected to Lithium Ion Battery (LIB) and Supercapacitor Module (SM) and sharing the DC link.

It can be seen that the inclusion of the short-circuit fault tolerant features in the converter adds four more switches compared to the original topology (Fig. 1), therefore resulting in higher costs and size than in the initial case. However, by using a proper control, (as will be demonstrated), the losses of the two topologies can be made very similar. The operation under fault mode will be discussed in this work; however, the studied system with the proposed control strategy has the capability of operating in a step-down voltage mode. Provided that a suitable control strategy is implemented, this voltage mode enables for a swift system reset once the fault is cleared. A proposal for such a fault ride-through feature will also be demonstrated in the following sections.

III. PROPOSED CONTROL STRATEGY

In the case under study, the main goal of the control of the battery converter is to maintain the DC link voltage constant,

while the aim of the control of the SM converter is to provide or absorb transient power during load variations. This control strategy is implemented through three control loops: one outer voltage control loop that controls the DC link voltage, plus two inner current loops in order to control the current flowing through the inductors [2],[3],[6], as shown in Fig. 4.

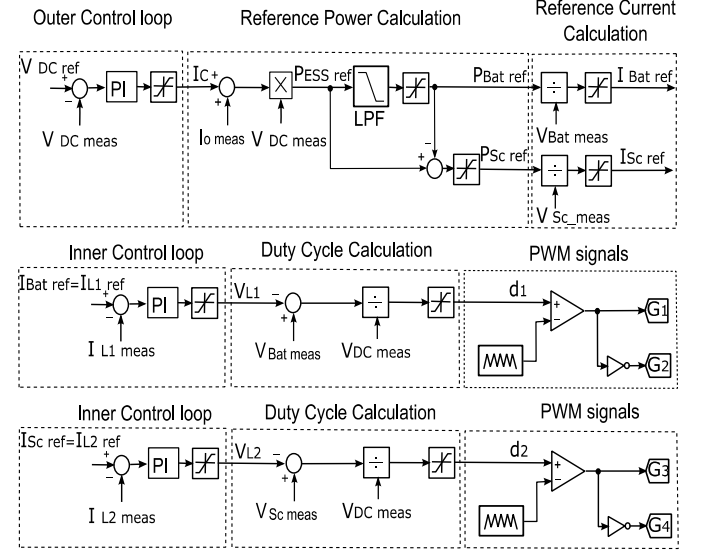


Fig. 4. Control of the two parallel bidirectional Boost Converters in order to maintain the DC link voltage constant (LIB converter) and provide or absorb transient power during load variations (SM converter).

The Energy Storage System (ESS) power reference is calculated from the control action of the voltage control loop (I_c) and the feedforward term (I_{o_meas}) to improve the recovery of the DC Link due to load variations. The limits of the control action are obtained from (1) and (2).

$$I_{c_min} = \frac{-V_{dc_ref}}{R_{L_min}} \quad (1)$$

$$I_{c_max} = I_{Bat_max} - \frac{V_{dc_ref}}{R_{L_max}} \quad (2)$$

where:

- I_{c_min} and I_{c_max} are the minimum and maximum current limits of the DC link current in Amps,
- V_{DC_ref} is the reference DC link voltage in Volts,
- R_{L_min} and R_{L_max} are the minimum and maximum load resistance in Ohms and can be obtained from the load profile,
- I_{bat_max} is the LIB maximum current in Amps.

The SM reference power is calculated as the difference between the references for the ESS and LIB power values. A limiter is used to ensure that SM power limits are not exceeded. The LIB power reference is calculated by using a Low Pass

Filter (LPF) to ensure that the SM is providing or absorbing the peak transient power during load variations. Also another limiter is used here, to ensure that the SM provides (or absorbs) the excess power that LIB cannot provide (or absorb) during steady state. The power references are calculated according to the following equations:

$$P_{ESS_ref} = (I_c + I_{o_meas}) * V_{DC_meas} \quad (3)$$

$$P_{Bat_ref} = \frac{1}{1+Ts} * P_{ESS_ref} \quad (4)$$

$$P_{Sc_ref} = P_{ESS_ref} - P_{Bat_ref} \quad (5)$$

where:

- P_{ESS_ref} , P_{Bat_ref} and P_{Sc_ref} are the reference powers of the ESS, LIB and SM respectively in Watts,
- I_c is the current in the DC link (control action of the voltage controller) in Amps,
- I_{o_meas} is the measured output current of the two converters in Amps,
- V_{DC_meas} is the measured DC link voltage in Volts,
- T is the time constant of the LPF in Secs,
- s is the Laplace complex variable; $s=\sigma+j\omega d$.

The bandwidth of the controller for the current in L2 (inductor in SM converter) is faster than the bandwidth of the controller for inductor L1 (LIB converter). This control scheme considers the inductor voltages, V_{L1} and V_{L2} in Fig. 3 to be the control actions at the output of the current regulators. The limits for the inductor voltages are developed as in (6) - (9). Therefore an adaptation between these control actions and the applied duty cycles in both converters, d_1 and d_2 , is implemented in the control (Duty Cycle Calculation blocks in Fig. 4).

$$V_{L1_min} = V_{Bat_meas} - V_{DC_ref} \quad (6)$$

$$V_{L1_max} = V_{Bat_meas} \quad (7)$$

$$V_{L2_min} = V_{Sc_meas} - V_{DC_ref} \quad (8)$$

$$V_{L2_max} = V_{Sc_meas} \quad (9)$$

$$d_1 = \frac{-V_{L1} + V_{Bat_meas}}{V_{DC_meas}} \quad (10)$$

$$d_2 = \frac{-V_{L2} + V_{Sc_meas}}{V_{DC_meas}} \quad (11)$$

where:

- V_{L1_min} , V_{L1_max} , V_{L2_min} and V_{L2_max} are the minimum and maximum inductor voltages for the LIB and SM boost converters respectively.
- V_{Bat_meas} and V_{Sc_meas} are the measured storage device voltages in Volts,

- d_1 and d_2 are the duty ratios of the LIB and SM converters respectively,
- V_{L1} and V_{L2} are the inductor voltages (control action of the current controller) for the LIB and SM boost converters respectively.

If these inductor voltage control schemes are implemented in the buck-boost converters, some modifications are required in order to calculate the duty cycle from the output of the regulator (Duty Cycle Calculation block), as shown in Fig. 5. With this direct approach, the diagonal switches (S1 and S4) and (S5 and S8) will commutate with the values of the duty cycle for the LIB and SM converters respectively, while the other diagonal switches (S2 and S3) and (S5 and S6) are complementary. This approach will increase the switching losses and the total efficiency of the system will drop. The expressions to calculate the duty ratio for both the LIB and SM converters and the limits for the inductor voltages in this case are shown in (12) - (17).

$$V_{L1_min} = -V_{DC_ref} \quad (12)$$

$$V_{L1_max} = V_{Bat_meas} \quad (13)$$

$$V_{L2_min} = -V_{DC_ref} \quad (14)$$

$$V_{L2_max} = V_{Sc_meas} \quad (15)$$

$$d_1 = \frac{V_{L1} + V_{DC_meas}}{V_{Bat_meas} + V_{DC_meas}} \quad (16)$$

$$d_2 = \frac{V_{L2} + V_{DC_meas}}{V_{Sc_meas} + V_{DC_meas}} \quad (17)$$

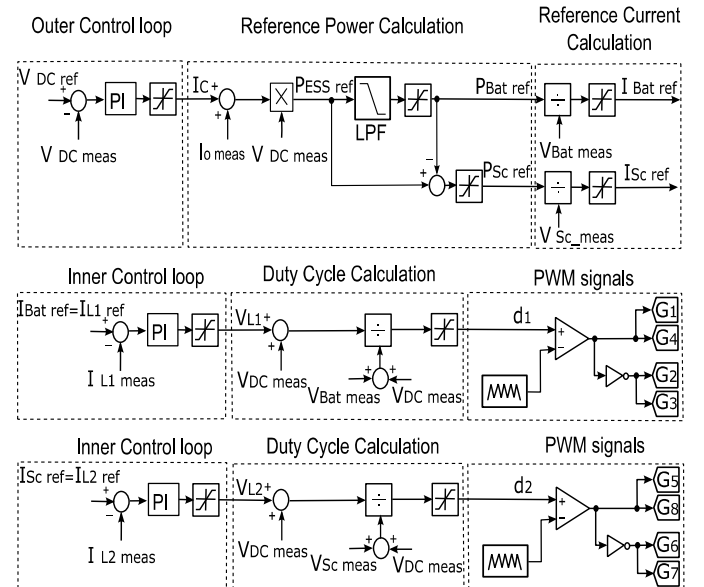


Fig. 5. Control of two parallel bidirectional buck-boost converters with the same carrier in order to maintain the DC link voltage constant (LIB converter) and provide or absorb transient power during load variations (SM converter).

The idea of the proposed control strategy deals with using two independent modes of operation for each converter during the healthy condition (Normal Operation) i.e. Buck Mode and Boost Mode, aiming to decrease the number of commutating switches in each converter, in order to decrease the switching losses [9]-[11]. In order to achieve a swift transition between the two switching modes, a PWM modulation of the converters through a triangle waveform will be implemented. However, this modulation will be based on two different triangle carriers signals: one carrier for the Buck mode (using peak values of the triangular waveform from 0.0 to 0.5), and another carrier for the Boost mode (using values from 0.5 to 1.0).

This structure implies no overlapping of the switching intervals, which yields two different switching patterns for the switches. For example (as shown in Fig. 6.), if the desired duty cycle is between 0.0 and 0.5, the bidirectional buck-boost converter operates in Buck mode, and therefore switches S4 and S8 are turned off, while switches S3 and S7 remain turned on continuously. The switches S1 and S5 switch with the value of the duty cycle and the switches S2 and S6 are their complement. For the Boost mode, when the duty cycle is between 0.5 and 1.0, switches S1 and S5 are turned on and switches S2 and S6 remain off continuously. Switches S4 and S8 switch with value of the duty cycle and the switches S3 and S7 are their complement. Fig. 7 depicts the implementation of this dual carrier control for the two parallel bidirectional buck-boost converters. The limits of the inductor voltage are the same as the case of the boost converter (6) - (9).

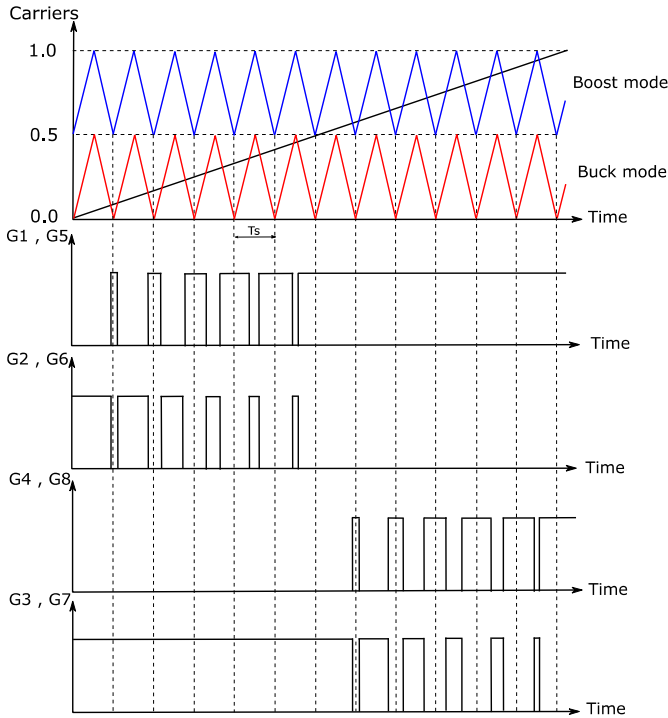


Fig. 6. PWM modulation of the two parallel bidirectional buck-boost converters based on two different carriers.

The possible short-circuit faults types in DC microgrids are short-circuit between positive and negative bus, or a short-circuit

between any bus and ground [12]. Once a short-circuit fault is detected in the DC link (for instance by detecting a DC link voltage below a threshold level), all the switches of the storage converters will be turned off. This control scheme does not have ride-through capability, and therefore if the fault is removed, the system by itself has no ability for returning to the initial operation mode, unless the control is reset manually and the DC link is charged. By making a modification to the control scheme, as show in Fig. 8, the converter can still operate in a controlled manner under fault conditions, and can resume normal operation once the fault is over.

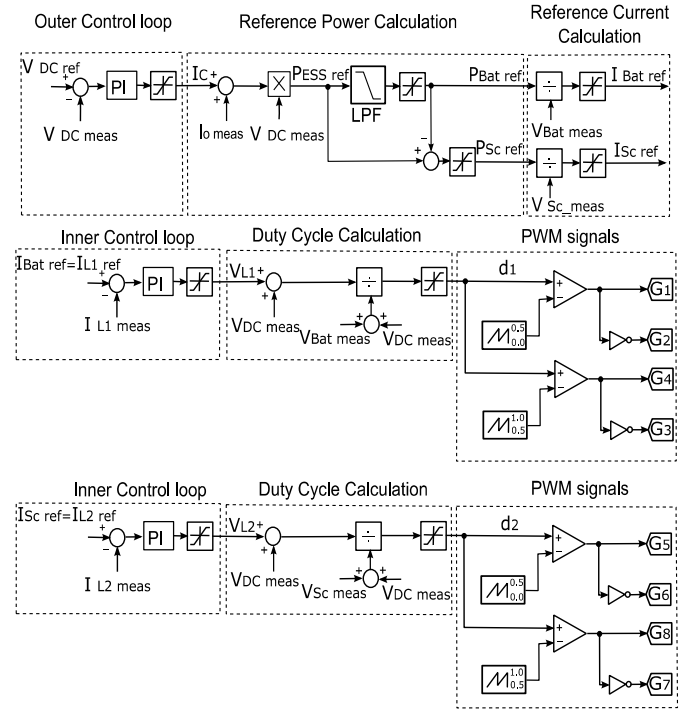


Fig. 7. Control of the two parallel bidirectional buck-boost converters with two different carriers in order to maintain the DC link voltage constant (LIB converter) and provide or absorb transient power during load variations (SM converter).

In this proposed control, while the short-circuit fault is present, a small safe current reference is applied to the LIB converter. This current reference depends on the DC link capacitance and how quickly the DC link charges after the fault is cleared. However, the switches of the SM converter will be turned off. The voltage across the inductor is limited and the duty cycle for LIB is therefore given by (18) to (20). Once the fault is cleared, this LIB current charges the DC link capacitors up to a specific value below the DC link reference voltage value. Once this value is detected, the control returns to the normal control scheme. If the fault is permanent, the control operates for a specific time and then the switches of the LIB converters will be turned off. Another advantage is that this control can be used to charge the DC link when the converter starts.

$$V_{L1_min} = 0 \quad (18)$$

$$V_{L1_max} = V_{Bat_meas} \quad (19)$$

$$d_1 = \frac{V_{L1}}{V_{Bat_meas}} \quad (20)$$

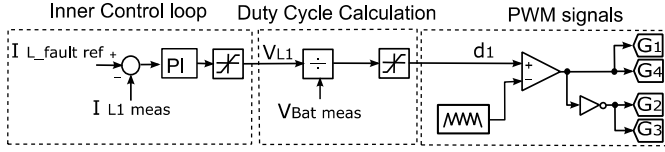


Fig. 8. Proposed control of the two parallel bidirectional buck-boost converters during the DC link fault.

IV. VALIDATION OF THE SYSTEM OPERATION UNDER NORMAL AND FAULT CONDITIONS THROUGH SIMULATION

Simulations of the full system operation have been carried out with MATLAB/SIMULINK/PLECS. The operating conditions of the systems for these simulations are listed in Table 1. Considering the ideal form of PI controller which is tuned by zero-pole cancellation, the transfer function is given by (21). The control parameters of the converters are listed in Table 2. Special attention has been put on the calculation of the losses in the switches (both conduction and switching losses) during the normal operation of the converters. The conduction and the switching losses of the switches are calculated according to (22) – (27). With this calculation of the losses, a comparison between the original and the new buck-boost topologies has been carried out. As can be seen Table 3, the losses (switching and conduction) using the original switching mode are high. However, the switching losses using the proposed dual carrier control scheme are almost equal compared to the original boost converters, while the conduction losses are higher as switches 1 and 5 are turned on during boost mode. In general, the total losses with the dual carrier scheme are similar to the original boost converter case.

Table 1. Parameters of the converters.

Parameter	Symbol	Value
Nominal Battery voltage	V_{Bat}	300 V
Nominal SM voltage	V_{SC}	96 V
Capacitance of the SM	C_{SC}	82.5 F
DC link voltage	V_{DC}	500 V
Capacitance of the DC link	C_{DC}	470 μ F
Maximum load power	P_{L_max}	1666.7 W
Inductance of the inductors	L	21 mH
Resistance of the inductors	R	0.3 Ω

$$C(s) = K_p * (1 + \frac{K_i}{s}) \quad (21)$$

where:

- $C(s)$ is the transfer function of the PI controller,
- K_p is the proportional gain,

- K_i is the integral gain.

Table 2. Parameters of the control of the converters.

Parameter	Symbol	Value
Voltage Control Loop		
Bandwidth	BW_v	30 Hz
Proportional gain	K_{P_v}	0.088548
Integral gain	K_{I_v}	7.09
Current Control Loop for LIB		
Bandwidth	BW_{LIB}	300 Hz
Proportional gain	K_{P_LIB}	39.564
Integral gain	K_{I_LIB}	22.8571
Current Control Loop for SM		
Bandwidth	BW_{SM}	500 Hz
Proportional gain	K_{P_SM}	65.94
Integral gain	K_{I_SM}	22.8571
Cut off frequency of LPF	f_{LPF}	8 Hz

$$P_{avg.cond.} = P_{avg.cond.IGBT} + P_{avg.cond.Diode} \quad (22)$$

$$P_{avg.cond.IGBT} = \frac{1}{T} \int_0^T [V_{ce}(t) * I_c(t)] dt \quad (23)$$

$$P_{avg.cond.Diode} = \frac{1}{T} \int_0^T [V_D(t) * I_c(t)] dt \quad (24)$$

where:

- $P_{avg.cond.}$ is the average conduction losses of the switch in Watts,
- $P_{avg.cond.IGBT}$ is the average conduction losses of the IGBT in Watts,
- $P_{avg.cond.Diode}$ is the average conduction losses of the anti-parallel diode in Watts,
- T is the switching time in Secs,
- V_{ce} is the on-state collector emitter voltage of the IGBT in Volts,
- I_c is the on-state collector current of the IGBT in Amps,
- V_D is on-state forward voltage of the anti-parallel diode in Volts.

$$P_{sw.} = P_{sw.IGBT} + P_{rec.Diode} \quad (25)$$

$$P_{sw.IGBT} = (E_{on} + E_{off}) * f_{sw} \quad (26)$$

$$P_{rec.Diode} = E_{rec.} * f_{sw} \quad (27)$$

where:

- $P_{sw.}$ is the switching losses of the switch in Watts,
- $P_{sw.IGBT}$ is the switching losses of the IGBT in Watts,
- $P_{rec.Diode}$ is the reverse recovery losses of the anti-parallel diode in Watts,

- E_{on} is the energy loss at IGBT turn on in Joules,
- E_{off} is the energy loss at IGBT turn off in Joules,
- f_{sw} is the switching frequency in Hz,
- $E_{rec.}$ is the energy loss of the reverse recovery of the antiparallel diode in Joules.

Table 3. The Losses in the topologies.

Topology	Conduction Losses (W)	Switching Losses (W)	Total losses (W)
Boost	10.67 W	49.93 W	60.61 W
Buck-Boost (original switching mode)	29.7 W	96 W	125.7 W
Buck-Boost (proposed 2 control modes)	22.2 W	49.93 W	72.13 W

Fig. 9 shows the operation of both the boost and the buck-boost with the dual carrier scheme solutions, under healthy conditions. The figure shows that these two solutions give the same performance during transient load steps. The LIB controls the DC link around 500V, while the SM delivers and absorbs the transient power required during the load steps (From 833.3 W to 1666.7 W and again to 833.3W) to avoid DC link voltage variation during the transients. This yields a fast recovery of the DC link voltage and a decrease in the power ratings and the stresses (including current ripple) in the battery.

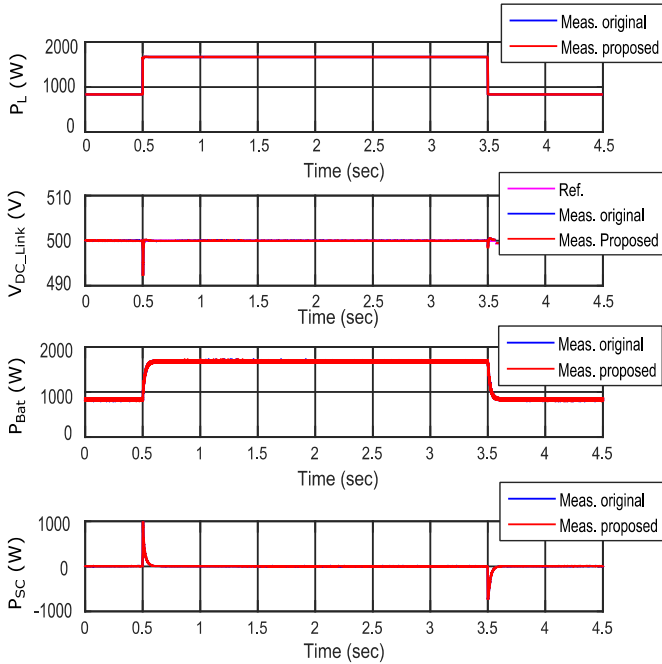


Fig. 9. Simulation results during normal operation for the original topology and the proposed one where the load power (P_L) is changed from 833.3 W to 1666.7 W and then to 833.3 W again.

The fault ride through capability of the buck-boost converter with the proposed dual-carrier control is shown in Fig. 10. The converters are operating under normal control, however when a DC link fault is detected at 0.5 sec (the DC link voltage below 15V threshold), the converters will operate under fault control. In fault control mode, a 4A reference current is applied to the LIB, while the SM leg is disconnected. When the fault is removed at 2.5 sec, this reference will charge the DC link to a specific value (500V threshold in this case). Then, the system is automatically reset to the normal control. The DC link will continue charging with a ramp until the DC link reference voltage value and the converter operate in normal mode.

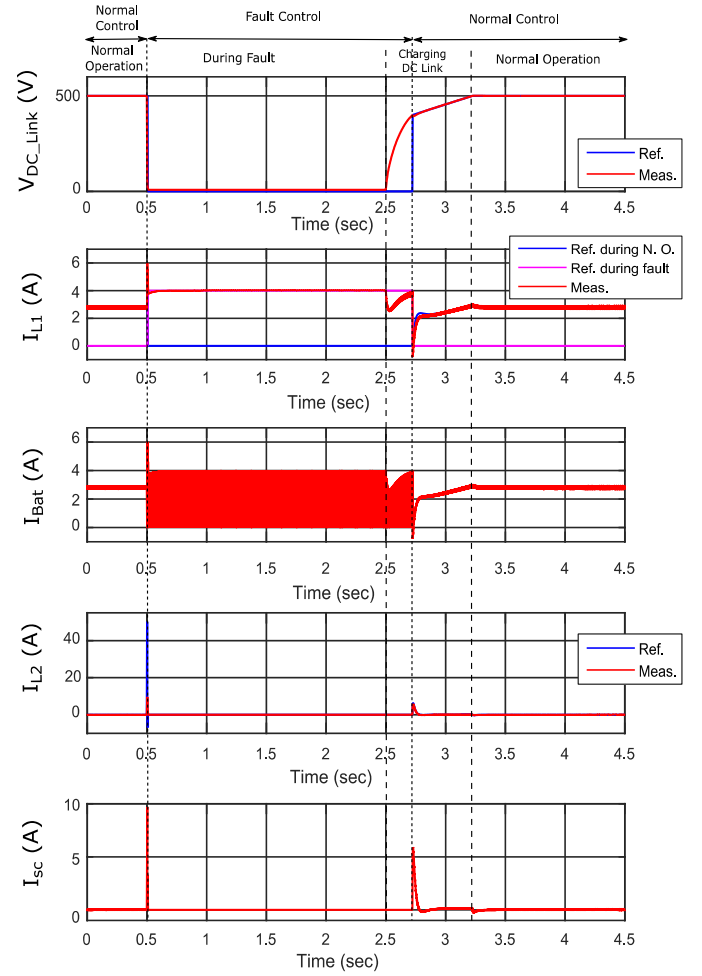


Fig. 10. Simulation results during fault and normal operation with the proposed control, the fault occurred at 0.5 sec and cleared at 2.5 sec.

V. VALIDATION OF THE SYSTEM BY EXPERIMENTAL RESULTS

The proposed control with the proposed topology are validated and tested using experimental setup as shown in Fig. 11. Fig. 12 shows the normal operation of the two parallel bidirectional boost converters and the two parallel bidirectional buck-boost converters. The load is changed at 0.5 sec from

833.3 W to 1666.7 W and at 3.6 sec is changed again to 833.3 W. Fig. 12 fully matches with the simulation results in Fig. 9. Fig. 13 show the operation of the buck-boost converter with the proposed control during the normal operation and fault operation and again fully matches with Fig. 10 from simulations. The fault is occurred at 0.5 sec and is cleared at 2.5 sec.

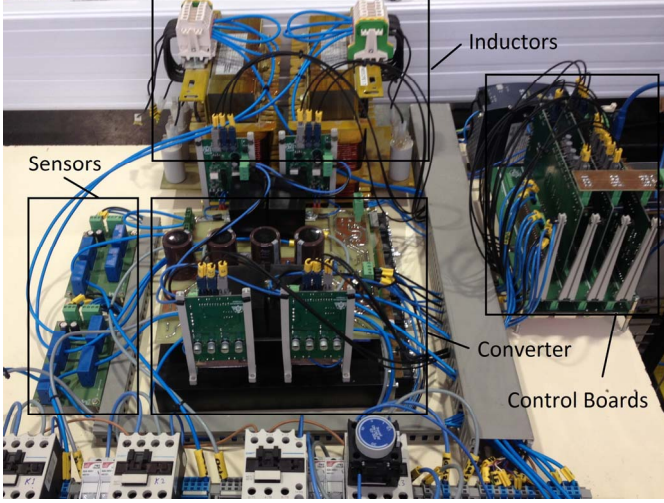


Fig. 11. Experimental setup of four legs of IGBTs and can be connected to be boost converter or buck-boost converter.

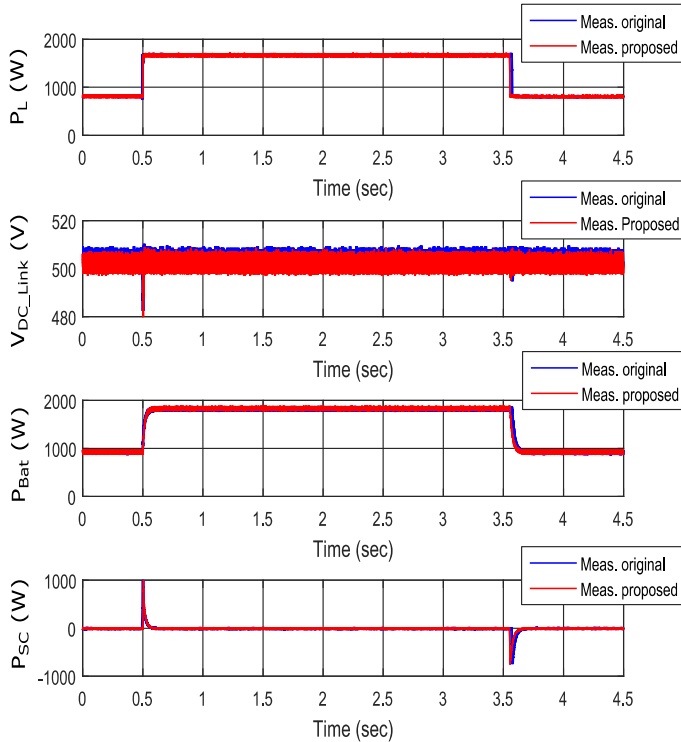


Fig. 12. Experimental results during normal operation for the original topology and the proposed one where the load power (P_L) is changed from 833.3 W to 1666.7 W and then to 833.3 W again.

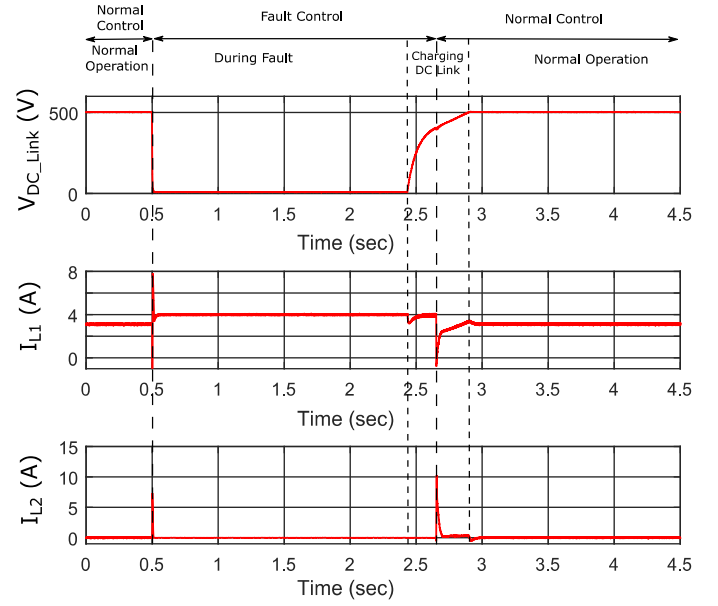


Fig. 13. Experimental results during fault and normal operation with the proposed control, the fault occurred at 0.5 sec and cleared at 2.4 sec.

VI. CONCLUSIONS AND FUTURE DEVELOPMENTS

In this paper, a DC link short-circuit fault-tolerant, fault ride-through control scheme for a non-isolated topology for Hybrid Energy Storage Systems has been presented, analyzed and verified through simulations and validated by experiments. This configuration has a higher component count than the bidirectional boost version which is the simplest topology able to provide hybrid performance. However, it has been stated that the inclusion of the fault-tolerant, fault-ride through capability does not significantly increase the power losses in the switches. The proposed configuration, with the two control modes using two carrier signals can operate in buck or boost mode, making this scheme useful for different applications.

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