

# Modeling and Impedance Analysis of a Single DC Bus-based Multiple Sources Multiple Loads Electrical Power System

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**Abstract**—The impedance based stability assessment method has been widely used to assess the stability of interconnected systems in different application areas. This paper deals with the source/load impedance analysis of the droop-controlled multiple sources multiple loads system which is a promising candidate in the future more-electric aircraft (MEA). This paper develops a mathematical model of the PMSG-based variable frequency generation system, derives the output impedance of the source subsystem including converter dynamics and shows the effect of parameters variation on source impedance and load impedance. A dynamic droop controller is proposed to provide the active damping to the system. In addition, the impedance analysis is extended to a generalized single bus-based multiple sources multiple loads system in which power losses are also investigated. The aforementioned analytical result is confirmed by experimental results.

**Index Terms**—Impedance, droop control, constant power load, stability, more electric aircraft, DC power distribution.

## I. INTRODUCTION

The more electric aircraft (MEA) concept is one of the major trends in modern aerospace engineering aiming for reduction of the overall aircraft weight, operation cost and environmental impact. Electrically powered systems are employed to replace existing hydraulic, pneumatic and mechanical devices. Hence the onboard installed electrical power increases significantly and this results in challenges in the design of electrical power systems (EPS). Different EPS architectures are currently being studied by the engineering community. At present, the tendency is to replace traditional ac distribution with high-voltage dc. This has several advantages such as increased efficiency, reduced weight and the absence of reactive power compensation devices [1]-[3].

Different power system architectures have been reviewed in [5]. Comparing with ac systems and used primarily on military vehicles and military aircraft, high voltage DC (HVDC) power distribution structure has advantages with respect to the ease of paralleling dc electrical bus bars and integration with loads such as actuators. Fig. 1 shows a promising EPS architecture with multiple generators feeding into a common dc bus. Two generators  $G_1$  and  $G_2$  connected directly to a shaft in the turbine and output the electrical power directly to the aircraft's electrical system through the active front-end converters (AFE

1, AFE 2). Permanent magnet synchronous generators (PMSGs) have been widely used in aerospace applications due to several advantages such as higher efficiency and power density [4]. This variable-frequency system has the advantage such as a simple and reliable configuration in which gear box is not needed between the generator output and the electrical power system.

The parallel operation topology of multiple generators connecting to one engine is promising in the MEA EPS. Appropriate power sharing among the sources is of importance in such multi-source configuration. So far, two methods have been widely used. The first option is master-slave control [6]. The master module acts as a voltage source and works out the current/voltage reference for slaves. However, communication among the parallel modules is needed. System failure can occur if communication fails. Alternatively, appropriate power sharing can also be achieved by employing droop characteristics [7]-[9]. It is much easier for implementation since no communication among the sources is needed. Meanwhile, higher modularity, higher reliability and lower cost of the system can be realized as well.

In addition, as one can see from Fig. 1, there are plenty of loads such as motor drives and power electronic interfaced converters which can be tightly regulated as constant power loads (CPLs). The negative incremental impedance characteristic of CPLs may result in system oscillations and even instability [10]-[12]. Thus, the candidate architecture should be carefully examined for stability in order to guarantee safe EPS operation for a wide range of operation scenarios. The stability of a 270V dc EPS has been analyzed in [13]. A switch reluctance motor is used to investigate the small signal stability. Since it is a standalone generation system, droop control is not used. In terms of small signal stability analysis, two dominant approaches are eigenvalues theorem and the impedance/admittance method. The impedance analysis method has been successfully applied for MEA EPS studies in [14], [15] since it provides an insight into shaping the impedance to assure a stable system. Stability for hybrid ac-dc MEA EPS is investigated in [16], [17] and the influence of some parameters variations on system stability is presented. However, so far there are no published works in regard to the stability analysis of the new power system architecture consisting of multiple sources and multiple loads (see Fig. 1). The main contributions of this paper can be summarized as follows:

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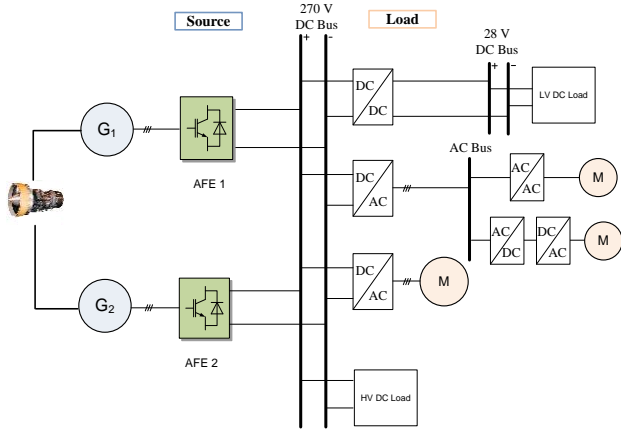


Fig. 1. Single line diagram of one power system architecture in future MEA.

- (1) Mathematical equation of source and load impedance of the droop-controlled EPS in future MEA applications is derived taking into account the generator-converter control dynamics. A set of parameters (mainly control parameters) are analyzed in order to specify the power interface characteristic of the cascaded system, such as the output impedance.
- (2) A dynamic droop controller, which reshapes the impedance under stability challenging condition, is proposed to provide active damping to the system.
- (3) Impedance analysis and subsequent stability investigation has been extended to a generalized power system of multiple loads feeding by parallel sources.

The rest of the paper is organized as follows: In Section II, the control design for the generator-active front end rectifier is presented. The transfer function for dc voltage tracking performance is also derived in the small signal manner. Section III derives the source impedance expression including system dynamics, discusses the source and load impedance for varying parameters and leads to stability assessment. Section IV extends the impedance analysis to a generalized multiple source multiple load dc power system. Experimental validation is shown in Section V in order to confirm the corresponding theoretical results. Section VI draws together the conclusions in this paper.

## II. SYSTEM MODELING AND CONTROL DESIGN

Fig. 2 presents the vector control scheme of the core system. The synchronously rotating reference frame has been widely used to model the PMSG [18]. After transforming the three phase measured currents into the rotating reference frame, conventional PI controllers adjust the stator currents in the  $dq$  domain and output  $dq$  voltage demands. The voltage demands are inversely transformed into 3-phase modulation indexes for PWM. By controlling the flux in the  $d$ -axis and the active power in the  $q$ -axis, the PMSG can operate in generating mode within the high speed region. Detailed control design for the PMSG system is discussed in [19].

The dynamic voltage equations of the PMSG can be expressed as follows:

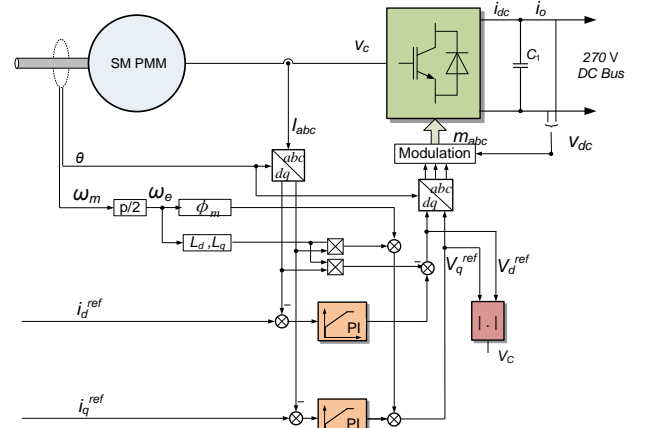


Fig. 2. Vector control scheme in the single generator-AFE based core system [19].

$$\begin{cases} v_d = R_s i_d + \frac{d\lambda_d}{dt} - \lambda_q \frac{d\theta}{dt} \\ v_q = R_s i_q + \frac{d\lambda_q}{dt} - \lambda_d \frac{d\theta}{dt} \\ \lambda_d = L_d i_d + \phi_m, \quad \lambda_q = L_q i_q \end{cases} \quad (1)$$

where  $v_d, v_q$ :  $d$ -axis,  $q$ -axis component of stator voltage;  $i_d, i_q$ :  $d$ -axis,  $q$ -axis component of stator current;  $\lambda_d, \lambda_q$ :  $d$ -axis,  $q$ -axis component of flux linkage;  $R_s$ : stator resistance;  $\phi_m$ : the flux linkage of permanent magnet;  $\theta$ : rotor position;  $L_d, L_q$ :  $d$ -axis,  $q$ -axis inductance. In this study, a surface-mounted permanent magnet machine (SMPMM) is used. The inductance in the  $d$  and  $q$  axes are the same and are both expressed as  $L_s$  in the subsequent discussions.

Conventional PI controllers are used to deflux the machine ( $d$ -axis) and control the dc voltage ( $q$ -axis). The stator current references in  $d$  and  $q$  axes are obtained from the output of the flux weakening controller and  $V_{dc}$  controller respectively. The reference of the ac voltage ( $v_c$ ) is dependent on the dc voltage. The peak convention is used for the transformation from three phase to synchronous rotating frame. The dc voltage reference ( $v_{dc}^{ref}$ ) is dependent on the desired droop characteristic.

### A. Inner Current Loop

Considering the inner stator current loop,  $v_d$  and  $v_q$  yield:

$$\begin{cases} v_d = (i_d^{ref} - i_d)G_c - \omega_e L_s i_q \\ v_q = (i_q^{ref} - i_q)G_c + \omega_e L_s i_d + \omega_e \phi_m \end{cases} \quad (2)$$

where  $G_c$  stands for the stator current controller in  $dq$  domain.

Inner current loop is designed to be a first-order system and thus, the zero of the PI compensator is set to cancel the pole of the plant. The proportional gain  $k_{pc}$  and integral gain  $k_{ic}$  are given by:

$$k_{pc} = \omega_c L_s, \quad k_{ic} = \omega_c R_s \quad (3)$$

where  $\omega_c$  is the bandwidth of the current loop.

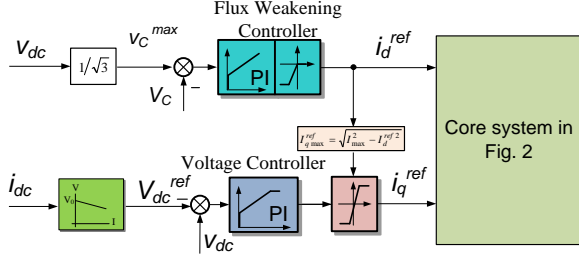


Fig. 3. Outer loop control scheme

### B. Flux Weakening Control

In terms of flux weakening control, one can obtain,

$$i_d^{ref} = (v_c^{max} - v_c) G_{fw} \quad (4)$$

where  $v_c^{max}$  is the maximum phase voltage of the converter and  $v_c$  is the ac side phase voltage.

$$v_c^{max} = \frac{v_{dc}}{\sqrt{3}}, \quad v_c = \sqrt{v_d^2 + v_q^2} \quad (5)$$

where  $v_{dc}$  represents the voltage on the local capacitor  $C_1$ .

### C. DC Voltage Control

The dc voltage reference  $V_{dc}^{ref}$  is obtained by the droop characteristic (shown in Fig. 4) which is expressed as follows:

$$V_{dc}^{ref} = V_o - k I_L \quad (6)$$

where  $k$  is the droop coefficient,  $v_o$  is the nominal voltage (270 V in this study) and  $I_L$  is the load current. The rated voltage of the main bus is 270 V, but the acceptable steady state range is between 250 V and 280 V as depicted in the standard MIL-STD-704F (see Fig. 5) [20]. If only one source is working in the power system, this control strategy is also feasible for the constant voltage control (droop coefficient  $k$  is set to 0).

Fig. 6 shows the control block diagram for the droop-controlled system. According to (1), the linearized q-axis voltage,  $v_q$ , can be expressed as:

$$\Delta v_q = (R_s + L_s s) \Delta i_q + \omega_e L_s \Delta i_d \quad (7)$$

Using the amplitude invariant transformation, the active power can be expressed in  $dq$  frame as:

$$P = \frac{3}{2} (v_d i_d + i_q v_q) \quad (8)$$

where  $v_d, v_q$  are the converter terminal voltages and  $i_d, i_q$  are the ac currents in  $dq$  frame.

Assuming the reactive power component equals zero ( $i_d = 0$ ), equation (8) can be linearized about an operating point (indicated with the subscript "o"):

$$\Delta P = \frac{3}{2} (\Delta v_q i_{qo} + \Delta i_q v_{qo}) \quad (9)$$

By substituting equation (7) into (9), the active power in small signal can be written as:

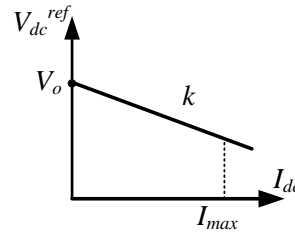


Fig. 4. Droop Characteristic.

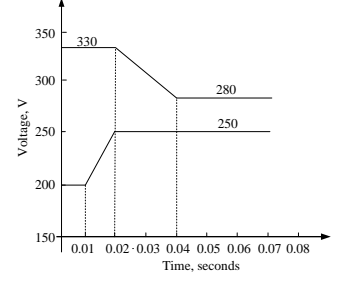


Fig. 5. Voltage requirement for 270 V dc system-MIL-STD-704F.

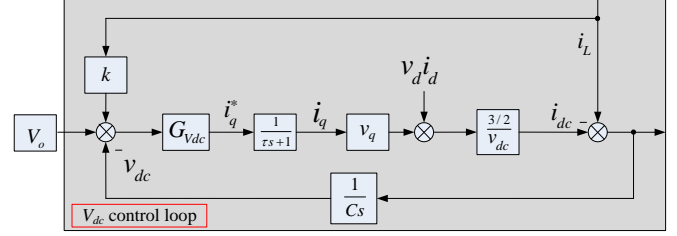


Fig. 6. Control block diagram for the droop-controlled system.

$$\begin{aligned} \Delta P &= \frac{3}{2} [((R_s + L_s s) i_{qo} + v_{qo}) \Delta i_q + \omega_e L_s i_{qo} \Delta i_d] \\ &\approx \frac{3}{2} (L_s i_{qo} s + R_s i_{qo} + v_{qo}) \Delta i_q \end{aligned} \quad (10)$$

Thus, the control-to-output ( $\Delta i_{dc}$  to  $\Delta i_q^{ref}$ ) can be expressed as:

$$\frac{\Delta i_{dc}}{\Delta i_q^{ref}} = \frac{1.5 (i_{qo} L_s s + R_s i_{qo} + v_{qo})}{V_{dco} (\tau s + 1)} \quad (11)$$

The control-to-output ( $\Delta v_{dc}$  to  $\Delta i_q^{ref}$ ) transfer function  $G_{p_v}(s)$  yields,

$$G_{p_v}(s) = \frac{\Delta v_{dc}}{\Delta i_q^{ref}} = \frac{1.5 (i_{qo} L_s s + R_s i_{qo} + v_{qo})}{V_{dco} C s (\tau s + 1)} \quad (12)$$

Since  $v_{qo}$  is positive and  $i_{qo}$  is negative, it can be inferred from (12) that a right half plane (RHP) zero exists in the plant, which can be derived as follows:

$$z = - \frac{R_s i_{qo} + v_{qo}}{i_{qo} L_s} \quad (13)$$

Due to this RHP zero, a faster bandwidth of the  $V_{dc}$  control will challenge stability. A PI compensator  $G_{Vdc}$  can be used as follows to control the dc voltage,

$$G_{Vdc} = k_{p\_Vdc} + \frac{k_{i\_Vdc}}{s} \quad (14)$$

Assuming the 2<sup>nd</sup> order system response with damping ratio  $\zeta$  and natural frequency  $\omega_{Vdc}$ , the dc voltage controller gain can be designed as:

$$k_{p\_vdc} = \frac{4\xi\omega_{vdc}C_{dc}V_{dc}}{3E_q}, \quad k_{i\_vdc} = \frac{2\omega_{vdc}^2C_{dc}V_{dc}}{3E_q} \quad (15)$$

where  $E_q$  is the back electromotive force (EMF) of the machine. Hence, the voltage control dynamics can be expressed as:

$$G_{Dy} = \frac{\Delta v_{dc}}{\Delta v_o} = \frac{G_{vdc}G_{P-v}}{1 + G_{vdc}G_{P-v}} \quad (16)$$

Substituting (12) and (14) into (16), the voltage control dynamics GDy can be obtained as follows:

$$G_{Dy} = \frac{1.5(i_{qo}L_s s + R_s i_{qo} + v_{qo})(k_{pvdc}s + k_{ivdc})}{s(\tau s + 1)(V_{dco}Cs - \frac{P_o}{V_{dco}}) + 1.5(i_{qo}L_s s + R_s i_{qo} + v_{qo})(k_{pvdc}s + k_{ivdc})} \quad (17)$$

If the load disturbance is neglected, it can be inferred that the voltage dynamics are mainly determined by the controller bandwidth instead of the droop coefficient.

### III. IMPEDANCE ANALYSIS

To investigate the influence of parameter variation on stability, it is essential to get a clear view of system characteristic with single source before looking into the complex system with multiple sources and multiple loads.

#### A. Source and Load Impedance

The equivalent circuit for the case of single source operation is presented in Fig. 7. Droop characteristic is implemented by means of an additional current source which is controlled by the main bus voltage  $V_b$ . Since the parasitic capacitance is much smaller than the bus capacitance ( $C_b$ ) and the local capacitance ( $C_l$ ), the cabling is represented by series  $R_c$ - $L_c$  branch in this section. As mentioned previously, tightly controlled power electronic converters and motor drives in the EPS can behave like CPLs. As a result the input impedance of the load subsystem can be seen as a negative incremental resistance. As discussed in [21] and [22], a linearized CPL can be approximately expressed by a negative incremental impedance ( $-R_{CPL}$ ) in parallel with a current source ( $I_{CPL}$ ).

$$R_{CPL} = \frac{V_b^2}{P_{CPL}}, \quad I_{CPL} = 2 \frac{P_{CPL}}{V_b} \quad (18)$$

where  $P_{CPL}$  is the power for the CPL.

The small signal stability of the system is determined by checking the impedance interaction between the source subsystem and load subsystem [23], [24]. Before applying the stability criterion to the cascaded system, it is worth noting that there is a prerequisite for this criterion. The source subsystem and load subsystem must be stable in stand-alone operation. The source impedance in Fig. 6 can be expressed as:

$$Z_s(s) = \frac{L_1 s + R_1 + k_1 G_{Dy}}{C_b s(L_1 s + R_1 + k_1 G_{Dy}) + 1} \quad (19)$$

where  $G_{Dy}$  is the dc voltage tracking performance shown in (16).

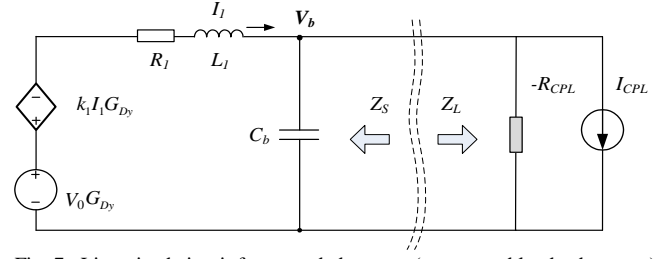


Fig. 7. Linearized circuit for cascaded system (source and load subsystem).

It is obvious that cable impedance ( $R_1, L_1$ ), bus capacitance ( $C_b$ ) and droop coefficient ( $k_1$ ) will affect the source impedance. Furthermore, parameters such as load power and control bandwidth, which have an effect on  $G_{Dy}$ , may also change the output impedance. It is already well known that a large bus capacitance will stabilize the system and increased CPL power will destabilize the system. In the case of a single source feeding a CPL with fixed dc voltage control ( $k_1 = 0$ ), an equilibrium point exists only if the following inequality is satisfied [25],

$$P_{CPL} < \frac{V_b^2}{4R_1} \quad (20)$$

Neglecting the source dynamics, the overall impedance can be written as

$$Z = (R_1 + L_1 s) // \frac{1}{C_b s - \frac{P_{CPL}}{V_b^2}} = \frac{(R_1 + L_1 s)}{C_b L_1 s^2 + (C_b R_1 - \frac{L_1 P_{CPL}}{V_b^2})s + (1 - \frac{R_1 P_{CPL}}{V_b^2})} \quad (21)$$

In order to rule out any RHP poles to ensure a stable operation, the following conditions should be satisfied:

$$(C_b R_1 - \frac{L_1 P_{CPL}}{V_b^2}) > 0, \quad (1 - \frac{R_1 P_{CPL}}{V_b^2}) > 0 \quad (22)$$

Provided that (20) is satisfied, the second term of (22) is already true. Thus, another upper limit of the CPL can be expressed as:

$$P_{CPL} < \frac{C_b R_1 V_b^2}{L_1} \quad (23)$$

Combing (20) and (23), the overall upper limit for the CPL power can be given by:

$$P_{CPL} < \min(\frac{V_b^2}{4R_1}, \frac{C_b R_1 V_b^2}{L_1}) \quad (24)$$

This paper will focus on the control parameters (droop coefficient, control bandwidth) on source/load impedance. The parameters used for the subsequent bode analysis is listed in Table I.

#### B. Effect of Vdc Control Bandwidth

It is mentioned at the beginning of this Section that the prerequisite of the impedance method is that both source and load subsystems are stable in standalone condition. Thus, no RHP poles should appear in the impedance expression.

SYSTEM PARAMETERS

Category	Parameter	Symbol	Value
Inner Loop	Current controller bandwidth	$\omega_c$	500 Hz
	Proportional and integral gain	$k_{pc}, k_{ic}$	6.28, 628.3
	Cable resistance	$R_i$	30 m $\Omega$
DC Link	Cable inductance	$L_i$	1 $\mu$ H
	Local capacitor	$C_i$	1.6 mF
	Bus capacitor	$C_b$	0.8 mF
ac Side	ac inductor	$L_s$	2 mH

Fig. 8 shows the layout of the poles of the source impedance (see (19)) with different control bandwidths. It is seen in Fig. 8(a) that a RHP pole appears when the control bandwidth increases to 60 Hz, which indicates that the source subsystem is unstable in standalone condition. When the control bandwidth increases, the proportional ( $K_{pVdc}$ ) and integral gain ( $K_{iVdc}$ ) increases correspondingly. The root of the polynomial equation of the denominator of the source impedance in (19) will change and could move from left half plane (LHP) to RHP with the increase of the bandwidth. When the control bandwidth reaches over 60 Hz, one pole of the source impedance is located in the RHP. The source subsystem is unstable in standalone condition and consequently, the overall system (source subsystem + load subsystem) will go unstable as well.

Fig. 9 shows the source impedance with varying  $V_{dc}$  control bandwidth. It can be seen that the source impedance decreases with the increase of the control bandwidth. The load impedance is invariant to the source control bandwidth. Although the magnitude of the source impedance tends to become smaller when a higher control bandwidth is applied, the standalone subsystem is unstable as shown in Fig. 8.

Therefore, it can be concluded here that a lower control bandwidth would cause the interaction between source and load subsystem, and the phase discrepancy exceeds  $180^\circ$ . As a consequence, the cascaded system is unstable due to this interaction. Alternatively, a very high control bandwidth (e.g., 60 Hz) will result in instability for the source subsystem itself and as a result, the overall system is still unstable.

### C. Effect of Droop Coefficient

The effect of droop coefficient variations on the source/load impedances is illustrated in Fig. 10. In terms of the steady state value, the voltage at the main bus will be further reduced under the same load when a higher droop coefficient is applied. As can be inferred from (18), the load impedance will be reduced due to the reduced bus voltage. It can be seen from Fig. 10(b) that the magnitude of the load impedance decreases, which is in alignment with the analysis. Alternatively, the magnitude of the source impedance in low frequency domain increases with the increment of droop coefficient. It can be observed from Fig. 10(b) that when the droop coefficient  $k$  is set to 1, the source impedance intersects with the load impedance. Meanwhile, the phase discrepancy between the source and

load impedance is over  $180^\circ$ , leading to an unstable operating point. Overall, it can be concluded that the system stability margin is reduced if a higher droop coefficient is applied.

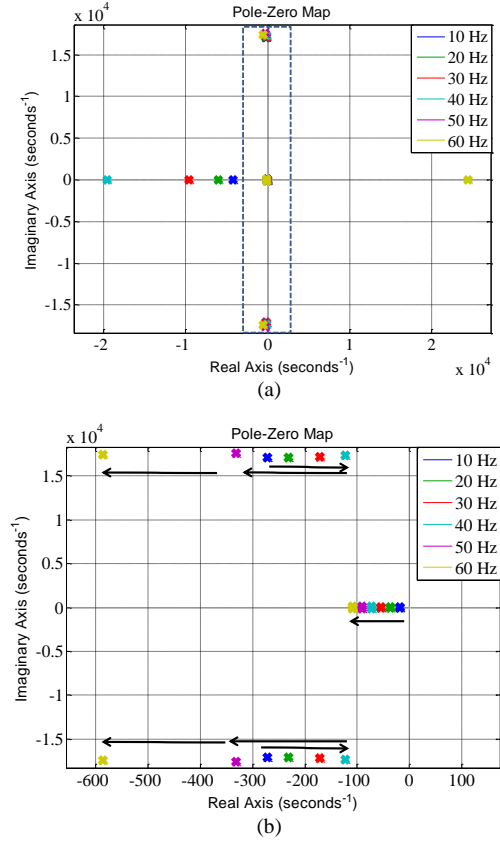


Fig. 8. Pole of the source impedance with respect to different control bandwidth. (a) Overview, (b) Zoomed part of the selected area in (a).

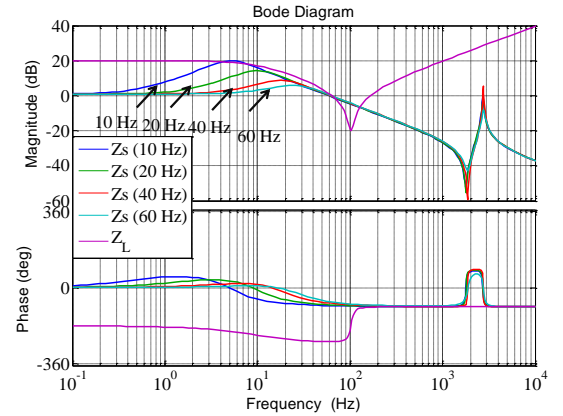


Fig. 9. Source/load impedance with different control bandwidth.

It shows in Fig. 11 that a larger droop constant will cause bigger bus voltage deviation and can even give rise to no intersection point between the source droop curve and CPL hyperbola curve (for example the  $k_3$  curve). As a result, no steady-state solution can be found, leading to instability.

As shown in Fig. 11, the V-I characteristic of the main bus can be expressed as

$$V_b = V_o - (k_i + R_i)I_L \quad (25)$$

For the load side, a CPL creates a hyperbolic line which can be expressed as

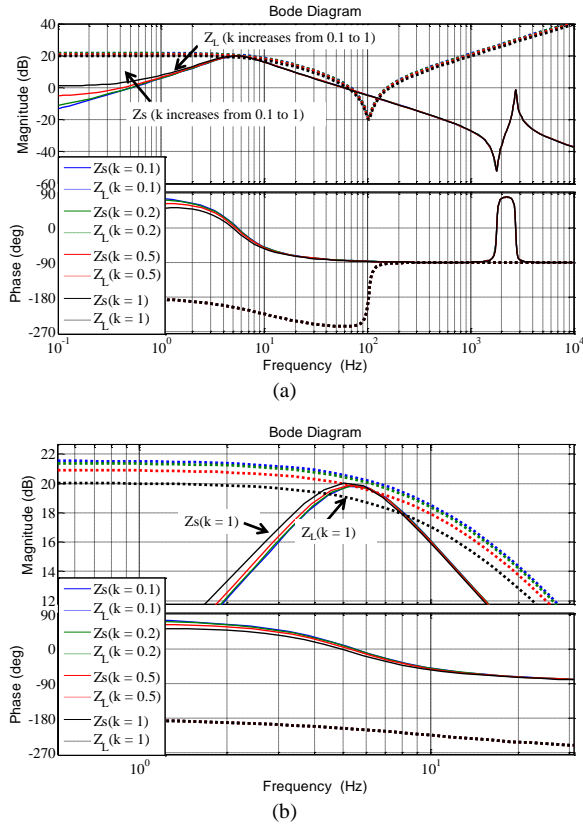


Fig. 10. Source impedance with different droop coefficients under a 6 kW CPL. (a) Overview of the source/load impedance. (b) Zoomed area of the interaction point.

$$P_{CPL} = V_b I_L \quad (26)$$

where  $P_{CPL}$  is the power of CPL and  $I_o$  is the load current. The system can operate normally only if the two curves have an intersection point (equilibrium point). The stable equilibrium point can be derived as follows:

$$V_b = \frac{1}{2} (V_o + \sqrt{V_o^2 - 4(k_i + R_i)P_{CPL}}), \quad (27)$$

$$I_L = \frac{1}{2k_i} (V_o - \sqrt{V_o^2 - 4(k_i + R_i)P_{CPL}})$$

Considering the existing condition of the operating point in (27), the maximum droop coefficient can be derived as

$$k_i < \frac{V_o^2}{4P_{CPL}} - R_i \quad (28)$$

Thus, the upper limit of the droop gain can be formulated using (28) and absence of source/load impedance interactions.

#### D. Proposed Dynamic Droop Controller

In order to enhance the system damping, a dynamic droop coefficient is proposed as:

$$K_{dy}(s) = \frac{k \omega_D}{s + \omega_D} \quad (29)$$

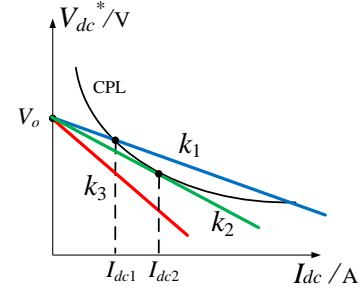


Fig. 11. Intersection between the droop-controlled source subsystem and the CPL load subsystem.

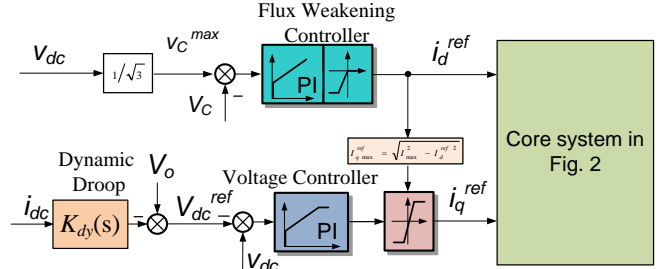


Fig. 12. Proposed dynamic droop controller.

The proposed dynamic droop control is shown in Fig. 12. It can be seen that the proposed dynamic droop controller is employed to replace the conventional fixed droop coefficient. It is virtually a low pass filter with the cutoff frequency  $\omega_D$  followed by a gain as the conventional fixed droop coefficient. The principle is to attenuate peak value around the certain resonant frequency region while keeping the other frequency response invariant. The cut off frequency can be designed according to the  $V_{dc}$  control bandwidth with the damping coefficient  $D$ .

$$\omega_D = \frac{\omega_{vdc}}{D} \quad (30)$$

If the control bandwidth ( $\omega_{vdc}$ ) is set to 10 Hz and the damping coefficient  $D$  is chosen as 2, it can be clearly seen in Fig. 13 that the resonance peak is attenuated by applying the proposed dynamic droop controller. In contrast, the source impedance rarely changes when the droop coefficient is 0.1 or 0.2, as shown in Fig. 14. It can be concluded here that the proposed dynamic droop controller can effectively damp the system under stability challenging condition whilst keeps the performance under lower droop coefficient.

Thus, the system stability cannot be improved by simply increasing  $C_b$ . As the eigenvalue sensitivities, with respect to 2 mF or 3 mF  $C_b$ , are reduced compared to the case of 1 mF  $C_b$ , it can be inferred that all the modes including the critical modes will gradually converge to a single point in the s-plane.

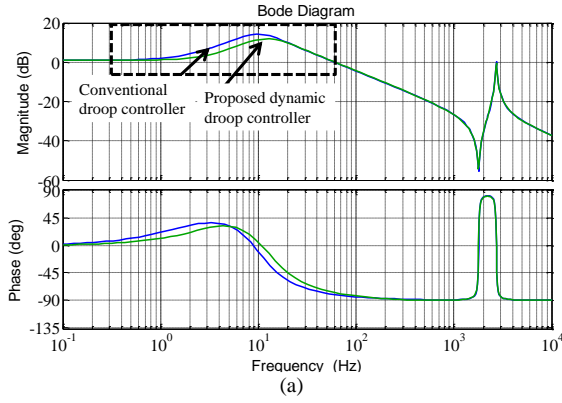


Fig. 13. Bode plot for the proposed dynamic droop controller for stability challenging condition ( $k = 1$ ).

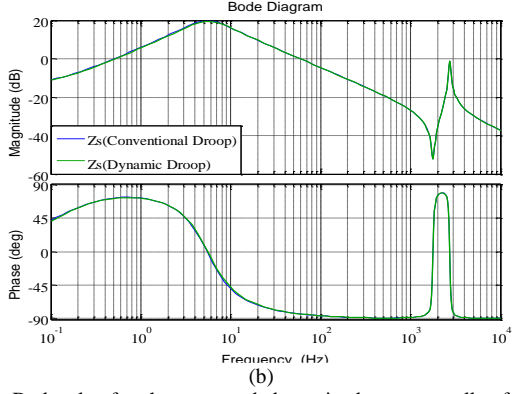
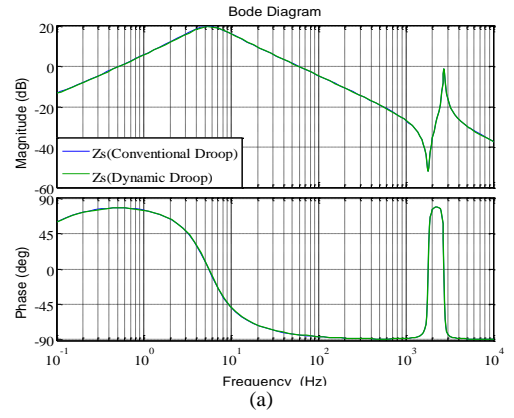
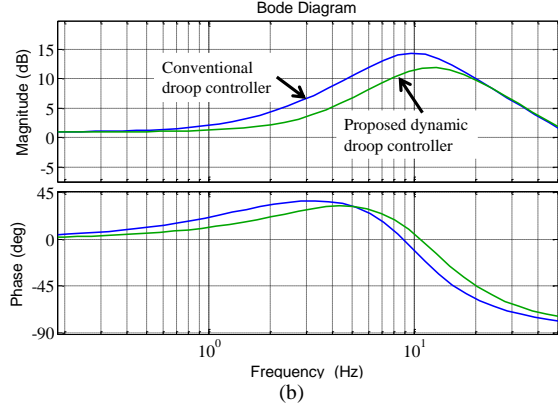


Fig. 14. Bode plot for the proposed dynamic droop controller for smaller droop coefficient: (a)  $k = 0.1$ , (b)  $k = 0.2$ .

#### IV. GENERALIZED MULTIPLE SOURCES MULTIPLE LOADS SYSTEM

As one can see from the power system in Fig. 1, multiple sources provide electrical power to the single dc bus to feed multiple loads. Thus, it is worthwhile looking into the stability of the overall system via impedance as well. This section will extend the impedance analysis to a generalized single dc bus-based multiple source multiple load power system.

##### A. Input Impedance of Multiple Load Subsystem

In a modern EPS, there are plenty of power electronic interfaced loads which may behave like CPLs. For the impedance analysis, the parallel CPLs can be modelled in a small signal manner and thus, the total input load admittance of the cumulative CPLs can be expressed as

$$Z_{CPLi} = \frac{1}{Y_{CPLi}} = \frac{1}{-\frac{P_{CPLi}}{V_b^2}} = -\frac{V_b^2}{\sum_{i=1}^m P_{CPLi}} \quad (31)$$

where  $P_{CPLi}$  is the power of  $i^{\text{th}}$  CPL. Hence, similar to the model of a single CPL in (18), the total CPLs can be represented as a cumulative negative impedance ( $-R_{CPLi}$ ) in parallel with a current source ( $I_{CPLi}$ ).

$$R_{CPLi} = -\frac{V_b^2}{\sum_{i=1}^m P_{CPLi}}, \quad I_{CPLi} = 2 \frac{\sum_{i=1}^m P_{CPLi}}{V_b} \quad (32)$$

Fig. 15 shows the load impedance with the increased number of CPLs.  $M$  denotes the number of parallel CPLs. It can be seen that the increased number of CPLs will reduce the magnitude of the load impedance, particularly in low frequency domain. This may result in interactions with the source impedance and as a consequence, cause instability of the system. Thus, in the view of the impedance analysis, it is in alignment with the well-known destabilizing effect of the CPL power.

##### B. Output Impedance of Multiple Sources Subsystem

The bus voltage with multiple sources can be expressed as follows:

$$V_b = V_1 - I_1 R_1 = \dots = V_N - I_N R_N \quad (33)$$

Considering each voltage terminal is droop-controlled and it can be written as:

$$V_i = V_o - I_i k_i \quad (34)$$

Using (34) to substitute the terminal voltage in (33) yields:

$$V_b = V_o - I_1 (R_1 + k_1) = \dots = V_o - I_N (R_N + k_N) \quad (35)$$

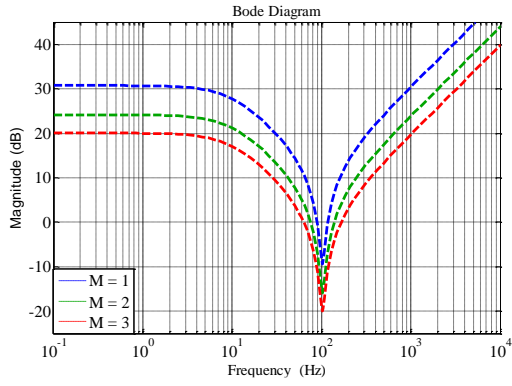


Fig. 15. Load impedance with different number of parallel CPLs (dc/dc buck converters).

Reformatting (35), the total load current which is equal to the sum of the branch current can be derived as:

$$I_L = \sum_{i=1}^N I_i = (V_o - V_b) \sum_{i=1}^N \frac{1}{k_i + R_i} \quad (36)$$

Thus, the bus voltage can be written as:

$$V_b = V_o - I_L \sum_{i=1}^N \frac{1}{k_i + R_i} \quad (37)$$

It can be inferred from (37) that the main bus V-I characteristic still follows a droop line which has a stiffer slope compared to individual droop slopes.

Fig. 16 shows the source subsystem consisting of multiple sources and the corresponding impedance model. Similarly as the derivation process in for the single source system in Section III, the overall source impedance can be computed by the ratio of open circuit voltage and short circuit current of the bus bar. Based on Kirchhoff's circuit laws, open circuit voltage and short circuit current can be calculated as follows:

$$Z_{s-t} = \frac{1}{\sum_{i=1}^N \frac{1}{(L_i s + R_i + k_i G_{dyi})} + C_b s} \quad (38)$$

Fig. 17 shows the output impedance of the source subsystem consisting of multiple sources. N stands for the number of multiple sources. Assuming that the power is shared equally among the parallel sources, it can be seen from Fig. 17 that the magnitude of the source impedance reduces with the increased number of parallel sources. The gain in low frequency domain reduces, indicating that at the steady state, the bus voltage deviation is less with the increment of the number of sources.

### C. Loss Analysis

Assume that the single source can provide enough power to feed the load, it is worthwhile investigating the optimal operating style to minimize the system losses including distribution losses and converter losses.

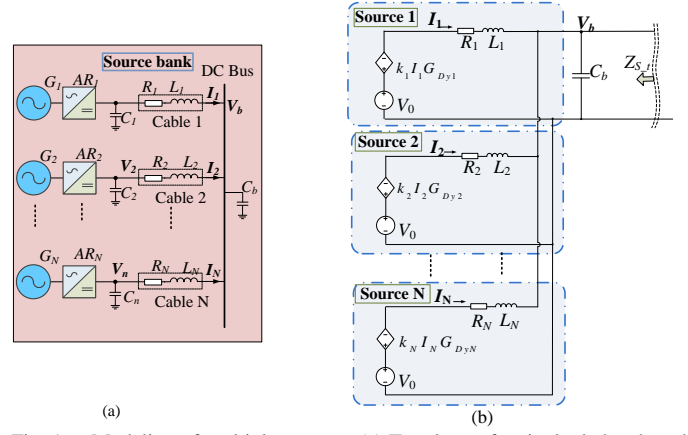


Fig. 16. Modeling of multiple sources. (a) Topology of a single dc bus based multiple sources system. (b) Equivalent circuit.

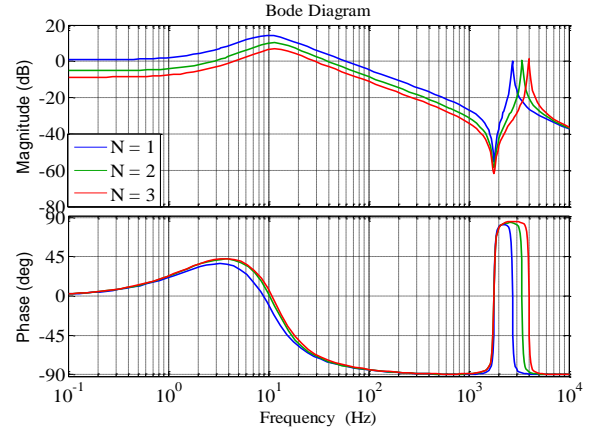


Fig. 17. Source impedance with different number of parallel sources.

Assuming that N sources are operating together in parallel through N parallel AFEs, the line losses can be expressed as follows:

$$P_{L-loss} = \frac{1}{N} I_{dc}^2 R_{dc} \quad (39)$$

where  $I_{dc}$  is the total dc link current and  $R_{dc}$  is the equivalent dc line resistance connecting from each converter to the bus bar. It can be inferred that the line losses in dc transmission/distribution lines are significantly reduced and further loss reduction could be obtained with more number of parallel sources. Alternatively, the converter losses which take switching loss and conduction loss into consideration can be examined as well. Based on a generalized converter loss expression in [26], [27], a single converter loss can be written as:

$$P_{C-loss} = a I_{ac}^2 + b I_{ac} + c \quad (40)$$

The ac side current of each converter is reduced with the increase of the parallel converters. Assuming that the parallel sources share the power equally, the generalized converters loss of N parallel AFEs can be expressed as follows:

$$P_{C-loss\_parallel} = \frac{1}{N} a I_{ac}^2 + b I_{ac} + N * c \quad (41)$$



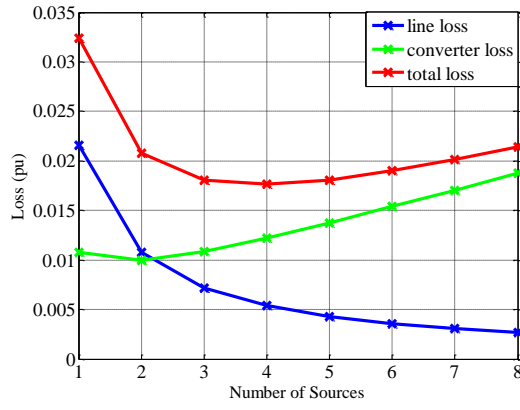


Fig. 18. Power losses with respect to the number of sources.

where  $I_{ac}$  is the total ac side current; a, b, c is the coefficient defined in per unit [27]. Combining the line loss and converter loss shown (39) and (41) respectively, the total loss of N parallel AFEs operation yields,

$$P_{loss\_parallel} = \frac{1}{N} I_{dc}^2 R_{dc} + \left( \frac{a}{N} I_{ac}^2 + b I_{ac} + N * c \right) \quad (42)$$

Fig. 18 shows the power losses (line loss + converter loss) with respect to the number of sources/converters using (39), (41) and (42). It can be seen that the line losses keep reducing with the increase of the number of parallel AFEs. Alternatively, the converter losses reduce to a certain threshold value with the increase of the number of parallel sources initially and then increases with the number of sources. Therefore, with proper selected number of the multiple sources, parallel operation can effectively reduce the losses to some extent.

## V. EXPERIMENTAL RESULTS

To perform the aforementioned analysis, the experimental rig (shown in Fig. 19) was built in the lab to support the theoretical analysis of the proposed multi-source paralleled EPS architecture. As depicted in Fig. 20, the experimental setup contains two active front-end converters AFE 1 and AFE 2 with a programmable ac source (CHROMA QuadTech 31120) isolated by three-winding step-down transformers (TF 1 and TF 2). Two dc/dc (buck) converters (Chopper 1, Chopper 2) are tightly regulated as CPLs. The experimental system parameters are listed in Table II.

### A. Effect of Control Bandwidth

As discussed in Section III-B, due to the existing RHP zero, the  $V_{dc}$  control bandwidth needs to be limited for stable operation. The experiment with a single converter AFE 1 has been conducted to see the effect of the control bandwidth on system stability. Fig. 21 shows the experimental results with different  $V_{dc}$  control bandwidths when the droop coefficient is fixed to  $k_1 = 2$ . It can be seen that with a 8 Hz control bandwidth the system is stable over a CPL power ranging from 0 to 3 kW whilst the system with 80 Hz control bandwidth shows significant oscillation when the load power reaches 3 kW. The result supports the instability discussion in Section III-B.

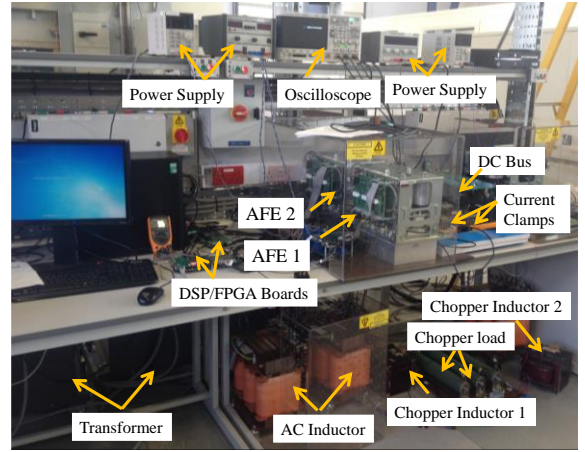


Fig. 19. Lab prototype.

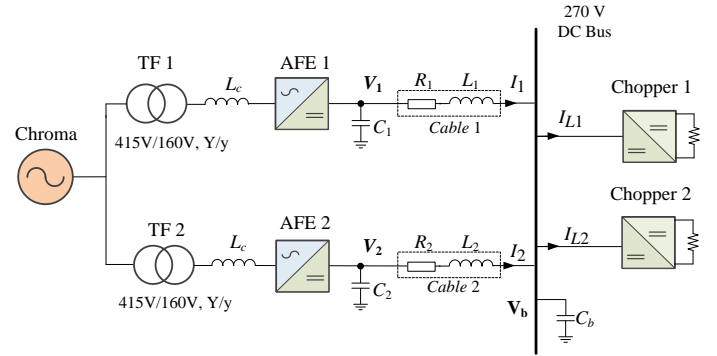


Fig. 20. Schematic of the experimental system.

TABLE II  
EXPERIMENTAL SYSTEM PARAMETERS

Category	Parameter	Value
Transformer ( $TF_1, TF_2$ )	Transformer	415 V/160 V, Y-y
ac Side Inductor ( $L_{in1}, L_{in2}$ )	ac side inductor	1.2 mH
	Load	12 $\Omega$
dc/dc Converter (Chopper 1, Chopper 2)	Inductor	1.3 mH
	Ratings	3 kW
	Switching frequency	20 kHz
PWM Rectifier (AFE 1, AFE 2)	Local capacitor	1.6 mF
	Ratings	100 kW
	dc link capacitor	0.8 mF
dc Link	Nominal bus voltage	270 V
	Line resistance	30 m $\Omega$
Cable ( $R_c, L_c$ )	Line inductance	5 $\mu$ H

### B. Effect of Droop Coefficient

As investigated in Section III-C, the increased droop coefficient will degrade the stability margin. Fig. 22(a) and (b) shows the result when the droop coefficient  $k_1$  is set to 1 and 0.1, respectively. Load power demand increases step-wise every 1.5 s. When the load power demand exceeds 3 kW, Chopper 2 is activated. It is shown in Fig. 22(a) that the system is oscillating at a higher power load (6 kW), which indicates

the interaction between the source and load impedance (see Fig. 10). When the droop coefficient is modified to 0.1, the system can work stably with a 6 kW load, as shown in Fig. 22(b). Thus, it confirms that a smaller droop coefficient can obtain more stability margin and the experimental result agrees with the analysis in Section III-C.

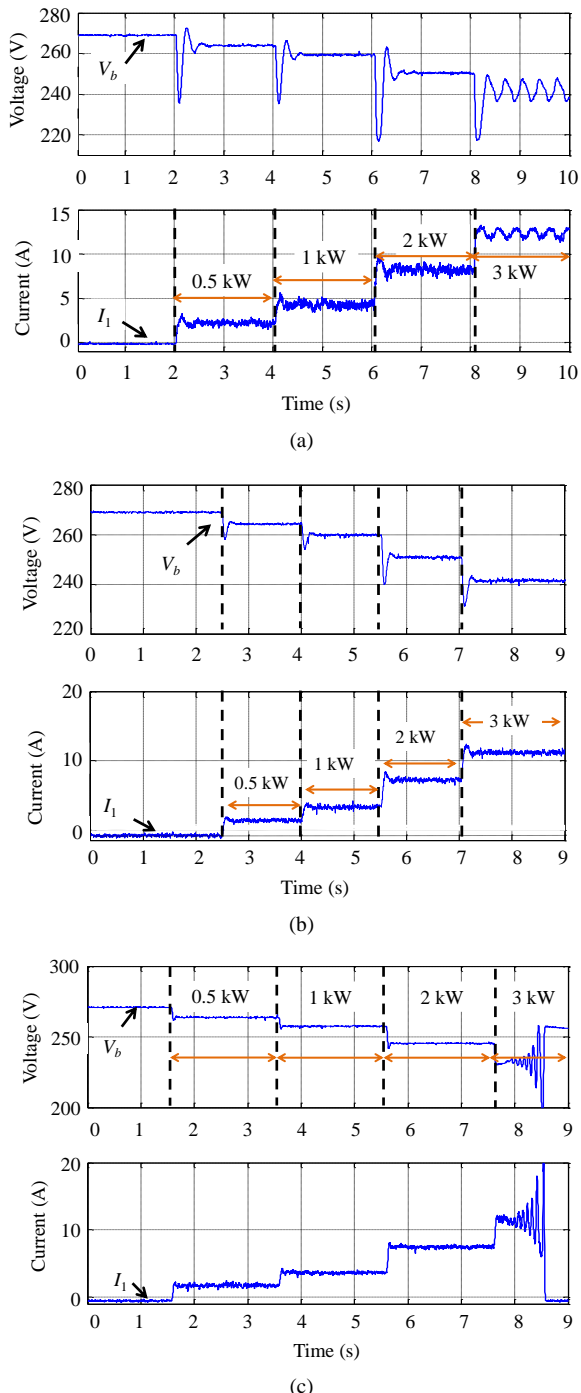


Fig. 21. Experimental result of a single AFE with different control bandwidths when  $k_1 = 2$ . (a) 8 Hz; (b) 20 Hz; (c) 80 Hz.

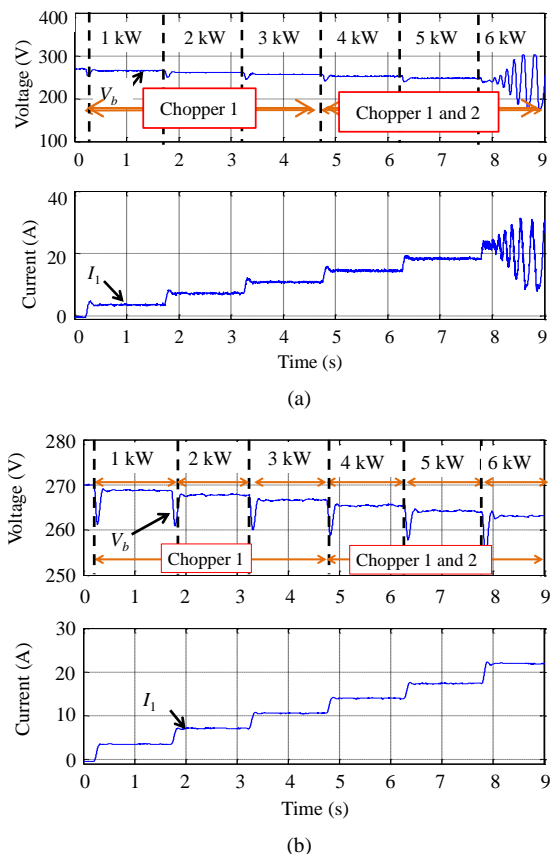


Fig. 22. Experimental result of a single AFE with droop coefficient (a)  $k_1 = 1$ , (b)  $k_1 = 0.1$ .

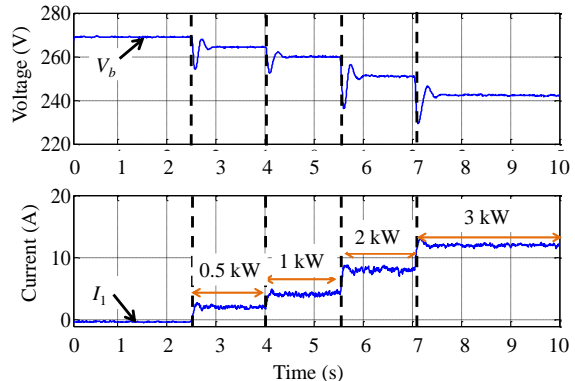


Fig. 23. Experimental result of the proposed dynamic droop controller with 8 Hz control bandwidth ( $k_1 = 2$ ).

### C. Effect of Proposed Dynamic Droop Controller

The proposed dynamic droop controller is also tested with the lab prototype. As discussed in Section III.D, two parameters need to be specified for the proposed dynamic droop controller  $K_{dy}$ : damping coefficient  $D$  and droop coefficient  $k_1$ . The damping coefficient  $D$  is set to 2.

For the sake of comparison between the proposed dynamic droop controller and conventional droop controller, the droop coefficient  $k_1$  is set to 2 and it is identical to the droop coefficient setting in Fig. 21(a). Fig. 23 shows the experimental result when the proposed dynamic droop controller is activated. In contrast with the result shown in Fig.

21(a), it can be seen in Fig. 23 that with the proposed dynamic droop controller, the system is working stably up to 3 kW CPL. Thus, it confirms the effectiveness and damping performance of the proposed dynamic droop approach.

#### D. Multiple Sources Operation

The parallel operation of AFE 1 and AFE 2 were tested and the result is shown in Fig. 24. Following the result shown in Fig. 21(a), at  $t = t_1$ , AFE 2 is connected to the bus with the same droop coefficient ( $k_2 = 2$ ) and control bandwidth (8 Hz). It is seen that the bus voltage increases to 258 V and the overall system is stabilized with the parallel operation. The result is consistent with the analysis in Section IV-B (see Fig. 17). The load impedance magnitude increases with the increase of bus voltage whilst the source impedance reduces at the low frequency region. Hence, it demonstrates that in comparison with single source operation, parallel sources can improve the system stability.

### VI. CONCLUSION

This paper deals with the stability study of a multi-source multi-load based dc EPS using the impedance approach. A mathematical model of the droop-controlled dc system has been developed and the corresponding source/load impedance has been derived taking into account the converter dynamics. The effect of a set of parameters, e.g., droop coefficient, dc voltage control bandwidth, etc on the source impedance and system stability has been discussed. Furthermore, the impedance analysis has been extended to a generalized system consisting of multiple sources and multiple loads. The impedance of the parallel sources and multiple loads has been analyzed and as a consequence, the stability of the parallel operation has been investigated. The main findings of this paper can be summarized here.

(1) Droop coefficient affects both source and load impedance and consequently, influence system stability. In the voltage droop control strategy, the upper limit of the droop coefficient is determined by two factors. One is the interaction between the source impedance and load impedance. The other is the availability of the steady-state equilibrium point between the source droop curve and CPL hyperbola curve.

(2) A dynamic droop controller is proposed to provide the active damping to the system. The experimental results validate the performance and effectiveness of this proposed method.

(3) Parallel sources can improve the system stability margin. In addition, the losses including converter losses and line losses can be effectively reduced by selecting proper number of parallel source converters.

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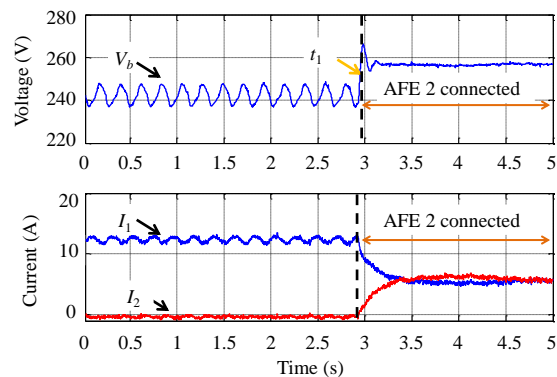


Fig. 24. Experimental result of the multiple sources operation when the AFE 2 is connected ( $k_1 = k_2 = 2$ ).

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