

Control of a Modular Multilevel Converter with Pulsed DC Load

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Abstract—This paper focuses on a Modular Multilevel Converter grid interface for a klystron modulator system that behaves as a pulsed DC load. With such a load, and without mitigating control, the MMC suffers from cell capacitor voltage imbalance between the converter arms which leads to distortion (fluctuation) of the absorbed AC power. This paper proposes an augmented modulation strategy, with a tailored distribution of the modulation signals between the arms within a phase, to ensure low AC power fluctuation. The effectiveness of the method has been verified through simulation and has been experimentally proven on a 7 kW MMC prototype operating with a 3 kA pulsed DC load.

I. INTRODUCTION

The Modular Multilevel Converter (MMC) due to its high modularity, efficiency and good AC waveform quality [1] has been selected as a suitable topology for the grid interface for the klystron modulators used in the Compact Linear Collider (CLIC) [2], [3]. MMCs are typically used in HVDC systems where one of the advantages is the absence of a bulk DC link capacitor. Conversely, in the application of interest, the klystron modulators work in a pulsed mode and are supplied from a capacitor bank that is periodically discharged by the high current pulse. The DC link capacitor is used to suppress pulsed load effects and to limit the DC voltage droop caused by pulsed current to 10 % of the nominal value. The main challenge for the grid interface is to further suppress the pulsed load effects on the AC side, by ensuring AC power fluctuation below 2 %. The converter and klystron modulator parameters for the proposed system are given in Table I. The passive components are rated in correspondence with [3], [4].

Some of the first research efforts associated with this application were focussed on suppressing the DC power fluctuation by inserting a droop compensator [5]. Another option investigated was to have a high bandwidth controller that would ensure a DC current profile that minimises the DC side power fluctuation [2]. Since the MMC has internal energy storage elements it should be possible to achieve low AC power fluctuation despite the presence of higher DC power fluctuation (more than 10 %). A suitable control method is to decouple the AC and DC side control [6], i.e. to decouple the pulsed load from the grid. However, the presence of a 50 Hz component in the DC voltage due to the voltage droop (note that the pulse repetition frequency is 50 Hz), causes imbalances between the cell capacitor voltages of the upper and lower

TABLE I
CONVERTER AND LOAD PARAMETERS.

Description	value
Rated power	16 MW
DC voltage	20 kV
AC voltage	10 kV
Number of cells per arm	20
Nominal cell voltage	1 kV
Phase inductance	3.6 mH
Arm inductance	1.8 mH
Cell capacitance	13 mF
DC link capacitance	8 mF
DC voltage droop	2 kV
Pulse frequency	50 Hz
Pulse duration	140 μ s

arms, which then causes overmodulation and distortion of the AC power. A control method to balance the capacitor voltages was proposed in [7]. This method is based on the addition of a 50 Hz component in the circulating current reference in phase quadrature with the 50 Hz component of the DC voltage ripple. However, this method is sensitive to the load pulse positions within the AC supply voltage period, and, if the pulse is in a critical region, balancing cannot be performed and AC power fluctuation exceeds the specification. A similar balancing method reported in [8], [9] suggests the insertion of a 50 Hz component in the circulating current reference in phase with the AC voltage reference. This method has been proposed for the normal operating mode of the MMC (e.g. HVDC applications) where imbalance between the converter arms is expected only during transients. However, by using appropriate controllers this method can be applied for pulsed DC load applications. Both arm balancing methods require circulating current reference generation and the use of suitable controllers (e.g. PI, PR).

This paper introduces a new control method which ensures low AC power fluctuation regardless of the load pulse position. The method is based on modulation signal redistribution between converter arms while maintaining the correct AC waveforms. The underlying idea behind the method is to avoid overmodulation by reducing the voltage reference of the arm with the lower capacitor voltages. This results in an arm balancing method with lower control complexity.

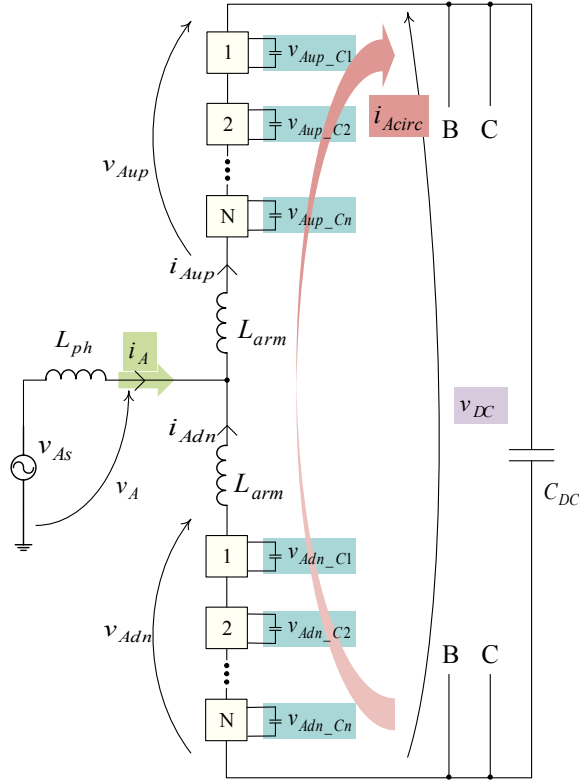


Fig. 1. MMC single phase representation.

The paper is organised as follows. The next section presents the MMC, basic equations and the organisation of the AC and DC side controllers. The following section discusses the pulsed DC load effects on the converter and the arm imbalances that occur to cause overmodulation with a corresponding effect on the AC side operation. Previously reported arm balancing methodologies are also discussed. The fourth section proposes the modified control algorithm to provide both arm balancing and low AC power fluctuation. The fifth and sixth sections validate the control algorithm by simulation and experiment, respectively.

II. MMC, EQUATIONS AND CONTROLLER

The three-phase MMC, represented in detail for phase A, is shown in Fig 1. The grid voltage, arm voltages (chain link voltages of upper and lower arm), phase current, arm currents, and fictitious circulating current are presented. Circulating current of phase A is calculated by (1).

$$i_{Acirc} = \frac{i_{Aup} + i_{Adn}}{2} \quad (1)$$

The equivalent AC side equation is given by (2):

$$v_{As} - L_{eq} \frac{di_A}{dt} + \frac{v_{Aup} - v_{Adn}}{2} = \frac{v^+ + v^-}{2} \approx 0 \quad (2)$$

where v^+ and v^- are positive and negative DC voltage potentials, and $L_{eq} = L_{ph} + \frac{L_{arm}}{2}$ is equivalent AC circuit inductance.

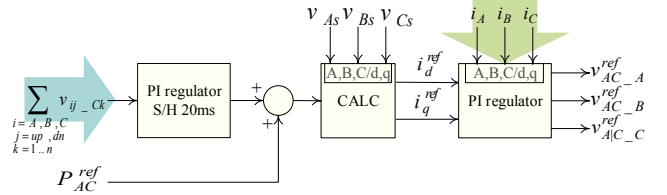


Fig. 2. AC side controller based on the d, q current controller.

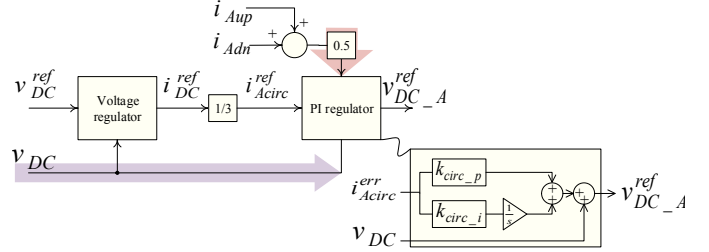


Fig. 3. DC side controller based on the circulating current controller.

Based on the AC side equation, the AC side controller is designed, by implementing a d, q current controller which produces the AC part of the reference, as presented in Fig. 2. The phase A AC side control variable, i.e. the AC part of the reference, is given by (3):

$$v_{AC_A} = -\frac{v_{Aup} - v_{Adn}}{2} \approx v_{AC_A}^{ref} \quad (3)$$

The DC side equation used for the circulating current control is given by (4):

$$v_{Aup} + v_{Adn} - 2L_{arm} \frac{di_{Acirc}}{dt} = v^+ - v^- = v_{DC} \quad (4)$$

The circulating current controller (Fig. 3) is PI based and it compensates for the voltage drop on the two arm inductors, and together with the v_{DC} as a feed-forward term produces the $v_{DC_A}^{ref}$:

$$v_{DC_A} = v_{Aup} + v_{Adn} \approx v_{DC_A}^{ref} \quad (5)$$

The circulating current reference is derived from the DC voltage controller that regulates the average DC voltage value to a constant reference. This reference can be corrected with a small DC component used for phase balancing, i.e. balancing of the capacitor voltages between the phases, as given in [7].

The normal modulation demands for the MMC converter are described by equation (6) for the upper and lower arm, respectively:

$$\begin{aligned} v_{Aup}^{ref} &= \frac{v_{DC_A}^{ref}}{2} - v_{AC_A}^{ref} \\ v_{Adn}^{ref} &= \frac{v_{DC_A}^{ref}}{2} + v_{AC_A}^{ref} \end{aligned} \quad (6)$$

The circulating current reference is typically one third of the DC current reference (here the phase to phase balancing loop is not presented) and it is constant as presented in Fig. 3. In that case, the arm currents have a DC part equal to the circulating current and an AC part equal to one half of the phase current.

The AC power fluctuation should be low, while the DC voltage should be controlled. To ensure this, the AC power is regulated via AC current control, while the DC voltage controller produces the DC current reference. The overall converter energy needs to be maintained, thus an energy controller is used to correct the input power reference (Fig. 2).

III. IMBALANCES CAUSED BY PULSED DC LOAD

In the case of the MMC being used as a rectifier with resistive DC load, arm imbalances can occur as a consequence of transients and unbalanced arm inductances/cell capacitors which are present in a practical system. In the case of perfectly balanced converter arms, as is normal in simulations, the converter arms are naturally perfectly balanced, and there is no need for arm balancing controllers. However, in applications involving a pulsed DC load, arm balancing controllers are necessary to guarantee correct converter operation - even if the converter components and the supply are ideal.

Due to the klystron modulation repetition frequency, the DC voltage ripple has a 50Hz component. If a conventional controller/modulation is used, the DC voltage ripple will produce non-zero average power having opposite signs on the converter arms [7]. This causes divergence of the cell capacitor voltages of the two arms, even if the capacitor voltages within one arm are perfectly balanced. If the sum of capacitor voltages of one arm falls below the modulation signal, overmodulation occurs. As a consequence the overall arm voltage is distorted, leading to distortion of the converter phase voltage and current and an increased AC power distortion [7]. If the modulation strategy follows (6), overmodulation can be avoided by balancing the cell capacitors between two arms. To achieve that, the circulating current reference needs to have a 50Hz component [7]–[9]. For the specific application, the circulating current 50 Hz component should be shifted by $\frac{\pi}{2}$ from the 50 Hz component of the DC voltage ripple [7] in order to create zero average power on both the upper and lower arms. Depending on the pulse position, i.e. the angle of the 50 Hz component in the DC voltage ripple, with respect to the AC voltage and current of a particular phase, different circulating current amplitudes should be used. The amplitude of the 50 Hz circulating current component in a particular phase increases if the pulse position is such that it affects that phase more severely. The method in [7] balances the arm voltages for the majority of the pulse positions. However, due to the sensitivity to pulse position, there are pulse positions for which arm balancing is not possible. In an alternative solution, the 50 Hz component of the circulating current can be aligned with the AC voltage reference [8], [9] and with a suitable amplitude, equal average power is achieved on the upper and lower arm. This provides arm balancing regardless of the pulse position but an additional phase balancing loop should be implemented (this loop is generally present to make sure equal power distribution among phases).

IV. PROPOSED MODULATION CHANGE

An alternative way to avoid overmodulation and ensure low AC power fluctuation is to redistribute the modulation signal in such a way that the AC part of the voltage reference and AC current are not distorted, i.e. that the equation (1) and (3) are satisfied. The distribution of the DC voltage reference should remain unchanged, to avoid zero sequence components in the converter AC voltages. The distribution of the AC part of the reference can be changed however. In that case the references for the upper and lower arm of phase A are given by following equations (7), instead of equation (6).

$$\begin{aligned} v_{Aup}^{ref} &= v_{DC_A}^{ref} - (1 + x_A)v_{AC_A}^{ref} \\ v_{Adn}^{ref} &= v_{DC_A}^{ref} + (1 - x_A)v_{AC_A}^{ref} \end{aligned} \quad (7)$$

where x_A is a parameter that describes redistribution of the AC part of the reference between arms of phase A. In the steady state the parameter x is constant for all of the converter phases. This way, the AC voltage generated by converter is not affected and both AC and DC voltage references can be followed which would provide low AC power fluctuation.

The simplified converter diagram in the case of phase A is given in Fig. 4. From this schematic it can be seen that $x_A v_{AC_A}$ does not affect the AC side equivalent circuit (common circuit, [10]), but only the DC side equivalent circuit (differential circuit, [10]). Thus, uneven distribution of the AC reference between two arms does not cause uneven distribution of the phase current between the two arms. However, the non-zero parameter x_A causes appearance of a 50 Hz component in the circulating current, acting as a disturbance for the circulating current controller which normally tries to maintain a constant reference. The equivalent DC side circuit (with focus on the 50 Hz disturbance) is presented in Fig. 5.

Since the circulating current now has a 50 Hz component, the circulating current controller will have non-zero error in steady state, with the mean value following the reference. Thus, the DC reference, comprised of the DC voltage feed-forward term and the PI controller output, is a function of the circulating current 50 Hz component. Considering the circulating current PI controller parameters (Fig. 3) the DC voltage reference in the steady state can be approximated as:

$$\begin{aligned} v_{DC_A}^{ref} &= v_{DC} + v_{DC_A}^0 - k_{circ_p} \cdot i_{Acirc50} \\ &\quad - k_{circ_i} \int_0^t i_{Acirc50}(\tau) d\tau \end{aligned} \quad (8)$$

Where $v_{DC_A}^0$ ensures that the mean circulating current follows its constant reference, and k_{circ_p} and k_{circ_i} are parameters of the circulating current controller. From (8), and the DC equivalent circuit from Fig. 5, it can be concluded that the controller output can be modelled as a series connection of a resistor with the resistance of k_{circ_p} and capacitor with the capacitance of $\frac{1}{k_{circ_i}}$ at 50 Hz, as presented in Fig. 6.

Based on the equivalent circulating current 50 Hz component circuit, it can be seen that the circulating current is in a counter phase with the $2x_A v_{AC_A}$. The PI controller would have a k_{circ_p} proportional to arm inductance ($\frac{2L_{arm}}{\tau_{circ}}$, where

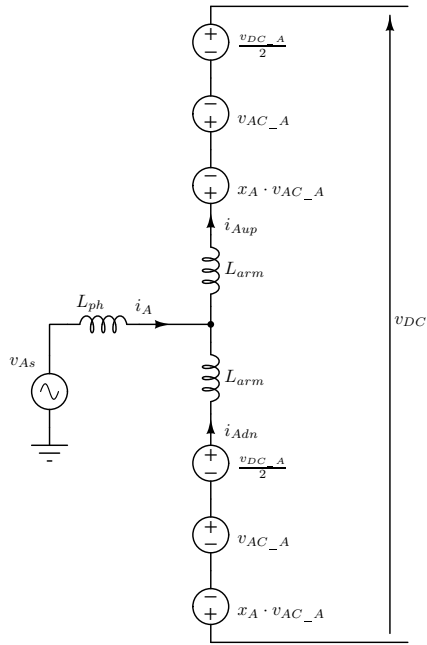


Fig. 4. Simplified schematics of the phase A of an MMC with uneven distribution of AC voltage reference.

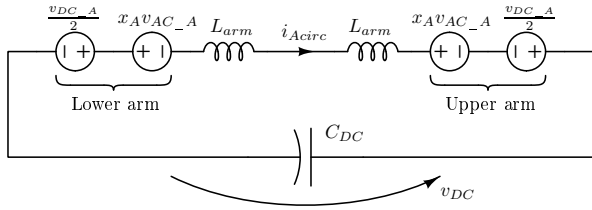


Fig. 5. Equivalent DC side circuit of phase A of an MMC with uneven AC reference distribution.

τ_{circ} is the controller time constant) which at 50 Hz represents a significantly higher impedance than the inductance ($2L_{arm}\omega$) or capacitance $\frac{k_{circ}i}{\omega}$. Thus, for a fast PI controller, the impedance of the circuit from Fig. 6 is dominated by the real component. The resulting 50 Hz component in the circulating current will be proportional to the AC voltage amplitude and the parameter x but with the opposite sign and a small phase shift with respect to the AC voltage reference. Therefore, the operation of the method is related to the method from [8], [9].

The parameter x influences the average power difference between the upper and lower arm. Increasing x decreases the arm power difference, which in turn causes a decrease in the difference between the upper and lower arm cell voltages. The benefit of this method is that it acts directly on the references to avoid overmodulation in the arms. Additionally, there is no need for explicit generation of a 50 Hz component in the circulating current references.

As shown in Fig. 7, the parameter x_A is directly derived from the imbalance between the capacitor voltages of the upper and the lower arm, meaning that the arm with the lower

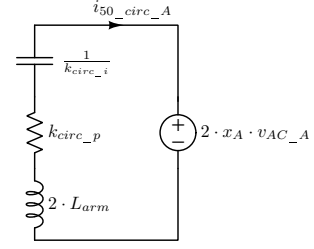


Fig. 6. Circulating current 50 Hz component equivalent circuit in the case of uneven AC reference distribution, assuming PI based circulating current controller.

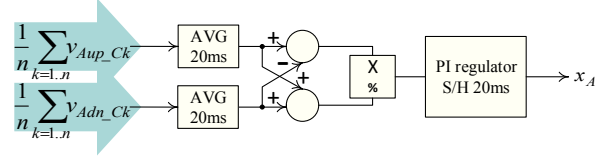


Fig. 7. Parameter x_A generation on the basis of cell capacitor voltages on the example of phase A.

available voltage will have a lower amplitude of modulation signal. Even when imbalance is present, overmodulation is avoided by reducing the modulation amplitude of the arm with lower capacitor voltages. Using this approach further divergence of the voltages is halted and the voltages are re-balanced. The PI controller ensures zero steady state error and proper voltage balancing. The arm balancing controller from Fig. 7 is included in the overall control strategy, as presented in Fig. 8. This control strategy is particularly attractive for the application of interest where the power taken from the DC side is pulsed and the overall converter energy controller operates on the AC power reference. Also, the converter AC and DC sides are still decoupled meaning that low AC power fluctuation will be achieved despite the pulses on the DC side. From the AC phase voltage and DC voltage references, together with the parameter x , the arm modulation signal is formed (7) and normalised with the sum of the cell capacitor voltages of that arm. The number of cells to be inserted is used for modulation, where only one cell performs PWM within an arm. Selection of the cells involves sorting the capacitor voltages within each arm and using the arm current direction information [11].

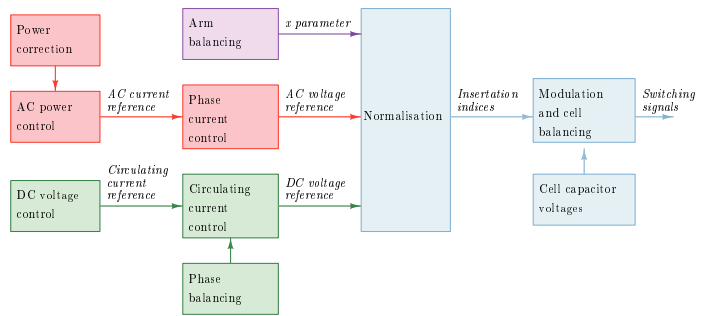


Fig. 8. Controller strategy with the redistributed AC reference for the pulsed load application.

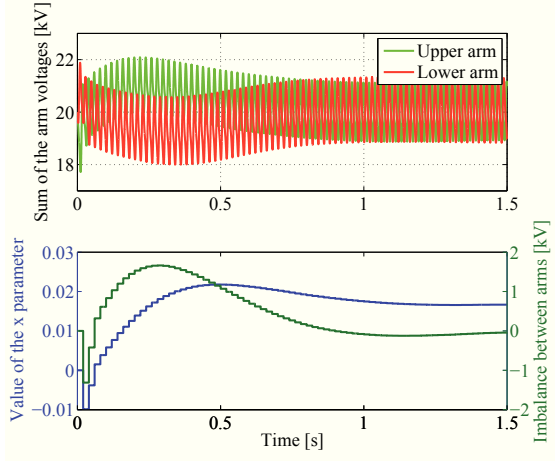


Fig. 9. Phase A arm balancing: Top plot presents the sum of the cell capacitor voltages in the upper and lower arm; The lower plot presents the difference of the sum of the upper and lower arm cell capacitor voltages (averaged at 20 ms), and the resulting x parameter.

V. SIMULATION RESULTS

The MMC converter operating under pulsed load conditions, emulating klystron modulators, with the ratings given by Table I, has been simulated in the PLECS environment. The sampling frequency and equivalent switching frequency is 10 kHz. The relevant controller gain values, are given in the Table II for the d , q and circulating current controller and for the arm balancing controller.

TABLE II
CONTROLLER GAINS.

Controller	Proportional	Integral
Phase currents	k_{dq_p} 9	k_{dq_i} 900
Circulating currents	k_{circ_p} 13.5	k_{circ_i} 540
Arm balancing	k_{x_p} 0.3	k_{x_i} 1

The following results relate to the pulse occurring 1.67 ms after the grid voltage phase A positive zero crossing which corresponds to a pulse position of 0.524 rad. Fig. 9 illustrates the phase A arm balancing principle applying the proposed method. The upper plot shows the sum of the cell capacitor voltages in the upper and lower converter arm, and illustrates their convergence. The reasons for the imbalance between the arms in this case are both the transient (the simulation starts at zero power transmission and ends at 16 MW) and the pulsed-load effects. The lower plot presents the arm balancing controller waveforms (Fig. 7). Based on the normalised difference between the sum of the capacitor voltages in the upper and lower arm (i.e. the error) the PI controller generates a suitable value of the x_A parameter. If the source of imbalance was only the transient, as it is in the case of a resistive load, the steady state value of the parameter x_A would be zero. Here, the steady state value of x_A is a measure of how much the pulsed load affects phase A.

Fig. 10 presents the converter waveforms in the steady state. The converter phase A voltage and current are presented on

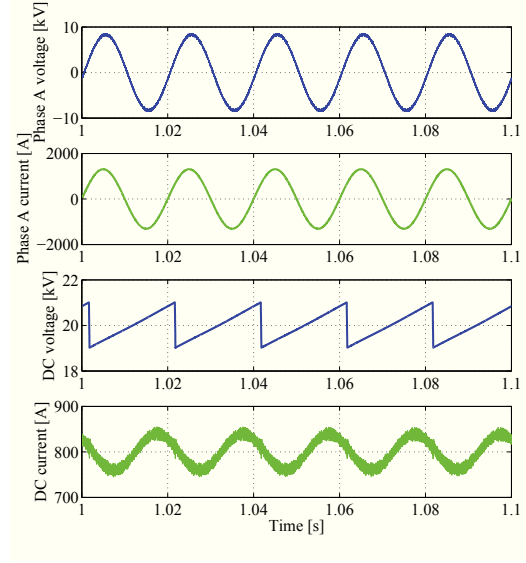


Fig. 10. Converter waveforms vs. time: Phase A voltage (towards grid neutral), phase A current, DC voltage and DC current.

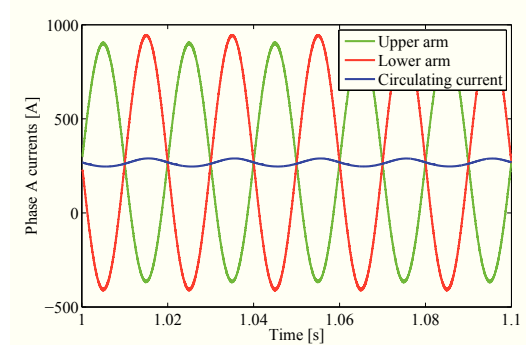


Fig. 11. Phase A arm currents and circulating currents vs. time.

the top two plots, while the DC voltage and the DC current are presented in the two lower plots. During the pulse the one sample delay present in the DC voltage reading, which is used as a feed-forward term in the circulating current controller, causes a spike in the DC and circulating currents. Here, a one sample delay compensation is applied on the DC voltage reading for the sampling instants during the pulse (with 10 kHz switching frequency those are one or two samples), so the spike in the DC current is almost negligible. Despite that, the 50 Hz component is present in the DC current, as a consequence of the 50 Hz component in the circulating currents. The amplitude of the DC current ripple does not vary much with the pulse position, but its phase shift does. Fig. 11 presents the phase A arm currents and circulating current. The arm currents have different amplitudes of the 50 Hz component due to the presence of the fundamental in the circulating current that is almost in phase opposition with the converter phase A voltage (refer to the Fig. 10). Fig. 12 shows the converter AC and DC side power. It can be seen that the AC power ripple is very low, below 0.3 %.

The converter is analysed for different pulse positions with

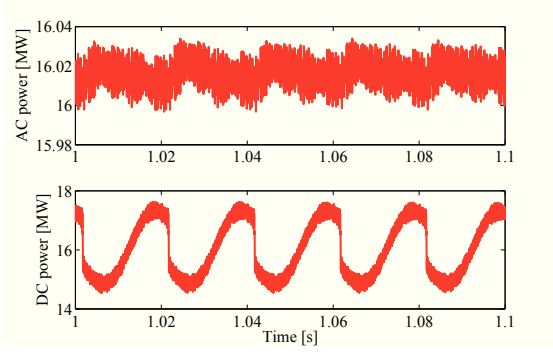


Fig. 12. Converter AC and DC side power vs. time.

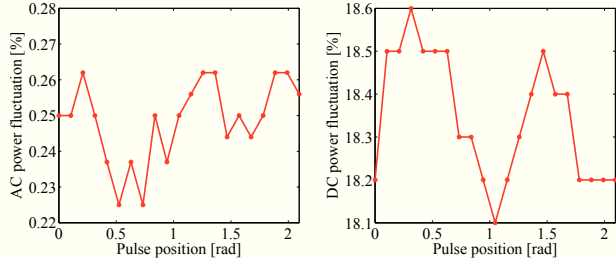


Fig. 13. AC and DC power fluctuation vs. the pulse position obtained by simulation.

respect to the phase A grid voltage zero crossing, covering one third of the grid period. The AC power fluctuation (Fig. 13) is around 0.25 % for all pulse positions, which means the performance of the method is insensitive to the pulse position. The DC power fluctuation (Fig.13) is around 18.5 %, which is increased when compared to the nominal 10 % created by the DC voltage droop. Fig. 14 presents the steady state value of the parameter x for different pulse positions. From the simulation results the values of parameter $x_{A,B,C}$ are below 2 %, meaning that this small redistribution of the modulation signals is enough for achieving arm balancing in the case of 10 % DC voltage droop. It can be seen that pulses positioned at the zero crossing of phase A affect the powers in that phase most significantly (the highest value of x) and this relationship is the same in the other phases.

VI. EXPERIMENTAL RESULTS

A small scale prototype has been built for the purpose of validating the behaviour of the grid connected MMC under pulsed DC load conditions. The 4 cell per arm, 7 kW converter has been designed by scaling down both the converter voltages and currents with the same scaling factor. A photograph of the experimental converter is presented in Fig. 15. A resonant circuit is used to emulate the pulsed DC load, this generates a 3.2 kA current pulse in a shape of half a sinusoidal (Fig. 16) when it is triggered. Table III lists the converter and the load parameters. The load parameters are designed to provide the same average current (16.5 A) as the scaled flat top pulse in the real application (same pulse area and duration). This results in $\approx \frac{\pi}{2}$ times higher peak pulse current.

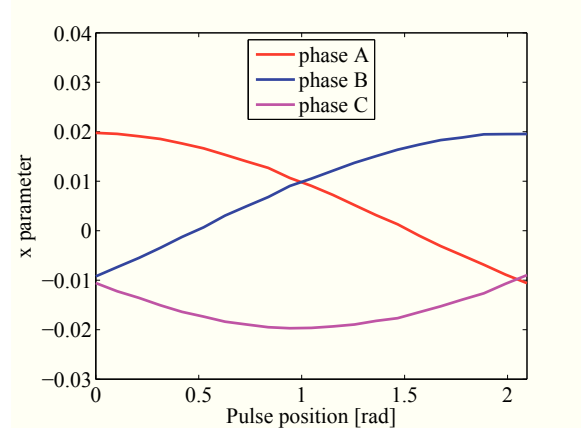


Fig. 14. Phase A, B and C x parameter values vs. the pulse position obtained by simulation.

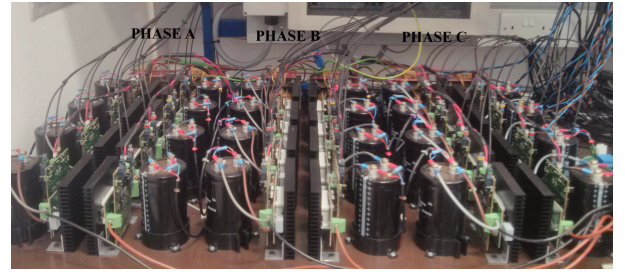


Fig. 15. Three phase MMC with 4 cells per arm.

TABLE III
EXPERIMENTAL CONVERTER AND LOAD PARAMETERS.

Description	value
Rated power	7 kW
DC voltage	400 V
AC voltage	225 V
Number of cells per arm	4
Nominal cell voltage	100 V
Phase inductance	3 mH
Arm inductance	1.5 mH
Cell capacitance	3.3 mF
DC link capacitance	8.5 mF
DC voltage droop	40 kV
Pulse frequency	50 Hz
Pulse duration	$\approx 150 \mu\text{s}$

The control algorithm is realised in a DSP-FPGA platform, including a Texas instruments 225MHz TMS320C6713 DSP and FPGA cards used for data acquisition and PWM signal generation. The DSP board is equipped with the DSK6XXHPI daughter card used for downloading the code and online monitoring of the control variables through the Matlab host interface. The waveforms captured through the host interface are sampled at 10 kHz, which is the DSP sampling frequency and thus they often have reduced switching ripple. Some of the results presented here are based on the host interface data. Other waveforms are captured with a 200MHz oscilloscope.

Fig. 17 presents the load characteristics, represented with

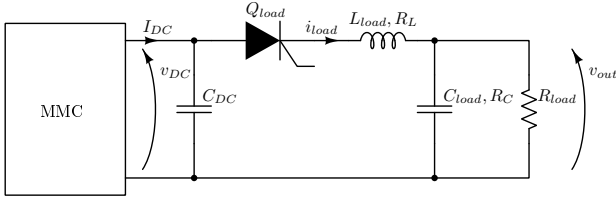


Fig. 16. Resonant Load circuit.

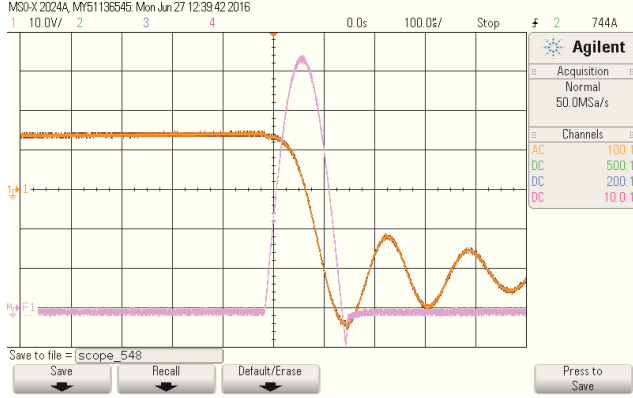


Fig. 17. Load current pulse (pink, 500 A/div) shaped with the resonant circuit and the DC voltage ripple (yellow, 10 V/div) vs. time (100 μs/div).

the current pulse and the droop of the DC voltage. The current pulse is nearly 3.2 kA while the voltage droop is about 45 V (around 10%) and the nominal DC voltage is 400 V.

Figures 18, 19 and 20 are captured for a pulse occurring 1.7 ms after the phase A grid voltage positive zero crossing, corresponding to a pulse position of 0.534 rad. Fig. 18 presents a converter waveforms under pulsed load conditions. Here the phase A converter voltage and current are presented together with the DC voltage and current. The DC voltage has about 10% voltage droop. Fig. 19 presents the converter/grid phase currents and the DC voltage with the pulsed DC load. As shown, there is no noticeable distortion in the AC currents, thus, as desired, the pulsed load effects are not propagated to the AC grid. Fig. 20 shows the effectiveness of the arm balancing algorithm based on the sum voltages of the upper and lower arm of phase A.

The AC and DC power fluctuations vs. the pulse position (computed on the basis of the host interface obtained AC voltages and currents and the DC voltage and current) are presented in Fig. 21. The values obtained are expected to be lower than the true values since the current switching ripple is rejected by the host interface sampling effect.

Similarly, the values of the $x_{A,B,C}$ parameter for phases A, B and C vs. the pulse position are presented in Fig. 22. Here, the dotted lines represent the internal imbalance present between the arms (in no load condition) which is dependent on the sensor calibration, temperature and imbalance between cells and arms. The imbalance is not significantly dependant on the rated power, meaning that its influence on the power imbalance and x parameter values is similar at full power,

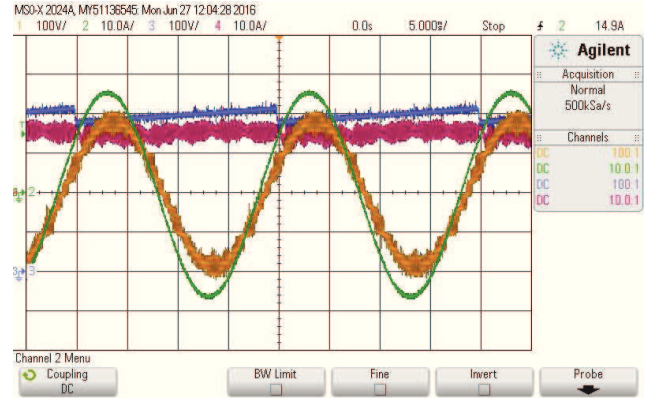


Fig. 18. Nine-level phase A converter voltage with respect to the grid neutral (yellow, 100 V/div), phase A converter/grid current (green, 10 A/div), converter DC voltage (blue, 100 V/div) and converter DC current (magenta, 10 A/div) vs. time (5 ms/div).

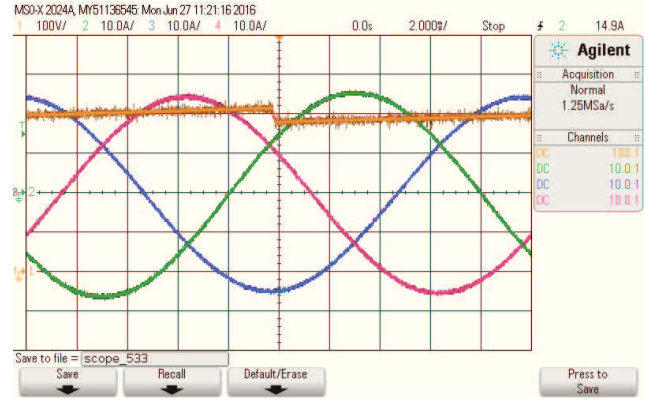


Fig. 19. Converter DC voltage (yellow, 100 V/div), converter/grid currents: phase A (green, 10 A/div), phase B (blue, 10 A/div) and phase C (magenta, 10 A/div) vs. time (2 ms/div).

but it is dependant on the temperature. The dashed lines represent the values of x parameter recorded during pulsed load conditions for different pulse positions. The full lines are the difference between the x parameters values during pulse and before pulse and they are associated with the pulsed-load effects. It can be seen that the experimental results are in agreement with the simulation results.

VII. CONCLUSION

The focus of the paper has been on the operation of a grid connected MMC under pulse discharge DC load conditions. A decoupled AC and DC side control has been adapted for the specific conditions and requirements of the application, while the modulation strategy is augmented in order to cope with the imbalances caused by the pulsed load. The change in modulation strategy is implemented to avoid overmodulation, which occurs as a consequence of the arm voltage imbalance. The proposed strategy achieves capacitor voltage balancing and AC power fluctuation below 0.3%, regardless the pulse position within the line voltage period. Simulation results demonstrate the effectiveness of the proposed modulation and control algorithm. The values of the x parameter, that

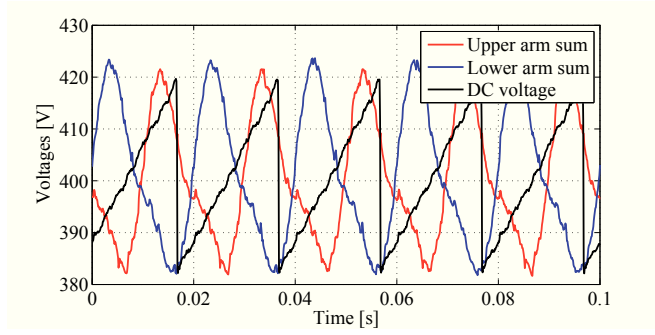


Fig. 20. Sum of the phase A upper and lower arm capacitors voltages and converter DC voltage vs time obtained by the host interface.

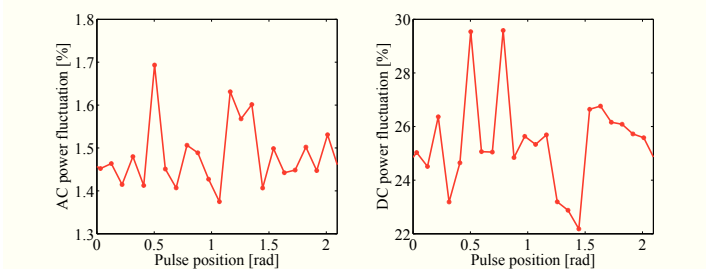


Fig. 21. AC and DC power fluctuation vs. the pulse position obtained by the host interface.

is a measure of redistribution of the AC reference between converter arms, is below 2 % for all pulse positions.

A small scale prototype was developed to experimentally prove the proposed approach. The arm balancing algorithm has proven successful, leading to undistorted grid currents. Experimentally, the AC and DC power fluctuations are higher when compared to the simulation results, but the MMC used has lower number of levels, and the emulated load does not draw flat-top pulses. The measured AC power fluctuation is below 2 %. The values of the x parameter have the same dependence on the pulse positions as those obtained by simulation.

Additionally a certain amount of imbalance between the arms was present in the no-load and resistive load operation. This is probably caused by the unsymmetrical (non-ideal) converter cells and arm inductances in the real converter, and also in the transducers that are used for sensing the capacitor voltages and arm currents. All those sources of imbalance are temperature dependent. The proposed method inherently copes with those imbalances in addition to those created by the pulsed load. Therefore, the proposed method could be used for different applications of the MMC other than that considered here.

The proposed algorithm does not explicitly impose a 50 Hz harmonic in the circulating current but this comes as a consequence of the AC reference redistribution and it has a phase shift with respect to the AC voltage reference of nearly 180° degrees in the case of a positive value of x (0° degrees in the case of a negative value of x). Therefore the method generates similar circulating currents to the method reported in [8], [9] but with decreased control complexity.

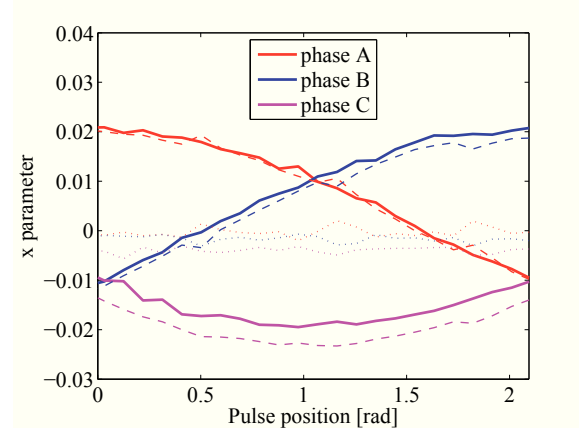


Fig. 22. Phase A, B and C x parameter values vs. the pulse position obtained by the host interface.

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