Influence of Design Parameters on the Short-Circuit Ruggedness of SiC Power MOSFETs

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***Abstract*— This work aims to present an investigation on short-circuit (SC) failure behaviour of SiC Power MOSFETs due to the onset of thermal runaway. As inferable from experimental outcomes, it is related to the formation of hotspot, whose exact location is mainly unpredictable and dictated by device structure and design parameters non-uniformities. TCAD simulations were performed to examine the impact of some parameters mismatch on hotspot formation and failure occurrence.**

Keywords*— *Silicon Carbide (SiC) Power MOSFET; Short-circuit failure; Short-Circuit ruggedness; Thermal Runaway; hot-spot; TCAD 2D simulation

I. INTRODUCTION

After the advent and the spread of Silicon Carbide (SiC) Power devices, especially Power MOSFETs [1], there has been an increasing interest in their failure mechanisms. Commercial devices should fulfil some robustness requirements, since in many applications stressful and out-of-SOA conditions might occur, even not rarely. Among all, short-circuit (SC) withstanding capability is a demanding feature for the design of reliable systems, and usually a device is required to survive a 10µs SC occurrence. A clear discernment on the failure origin could allow future devices to be more robust, increasing circuits reliability in case of undesired working conditions.

In recent years several works appeared, investigating and characterizing SiC Power MOSFETs. Many analyses reported SC devices behaviour, showing both single pulse and repetitive testing (e.g. [2]-[4]) highlighting maximum SC limits in different conditions, even spotting electro-thermal instability [5]. An analytical analysis of short-circuit capability has been proposed in [6] while two different failure modes have been identified and explained in [7]. Moreover, various physic-based compact models have been proposed, some including crucial electro-thermal effects (e.g. [8]-[9]).

In this paper, numerical simulations were the basis for the evaluation of design parameters impact on devices short-circuit capability, and their influence in creating weak spots. A TCAD structure was calibrated on measured transfer characteristics of a 1.2kV commercial Power MOSFET, nonetheless it does not reproduce the actual device geometry, and then it can be considered as a more general case study.

II. ANALYSIS

First, it is worth briefly recalling the results described in [7]. During single pulse test, temperature was suggested to be origin of two separate failure events. Moderate temperature increase (in case of relatively low power applied) could provoke a permanent damage on the top layers (resulting in gate/source terminals short). Consequently, it is impossible for the device to conduct anymore. The second case occurs for a large temperature increment. The amount of extra carriers thermally generated increases dramatically up to a value for which the leakage current is high enough to punch through the body/drift junction until it sets on thermal runaway phenomenon. If triggered, this positive feedback process makes the current focalize in a limited area. Fig.1 depicts the described situation observed experimentally, where the normalized temperature distribution at the turn-off (t_{PULSE}=8µs) is shown. It was obtained, being synchronized exactly at the turn-off instant, using a custom IR thermography system [10], that allowed to clearly catch the hot spot just before the failure event.

It has to be noted that, in this case, the failure occurs approximately 1µs after the turn-off (Fig.2). It is a failure mode usually observed in IGBTs [11], as well as current tails appearing at turn-off. This behaviour confirms that the failure cause could lie in a local increase of leakage current sustained by temperature.

During ON-state the current spreads nearly uniformly all over the device, but unavoidably some areas could have

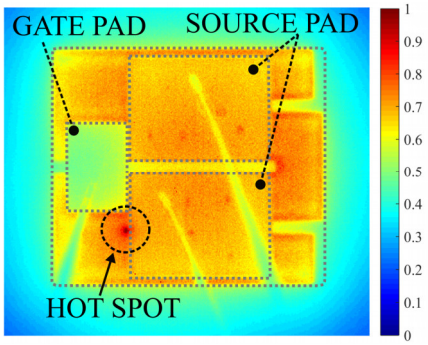


Fig. 1. Normalized temperature increase at t=8µs

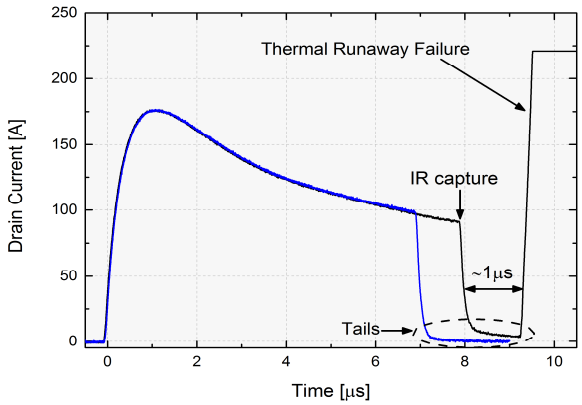


Fig. 2. Drain current short-circuit waveforms (V_{DS}=600V; V_{GS}=18V; T_{CASE}=27°C)

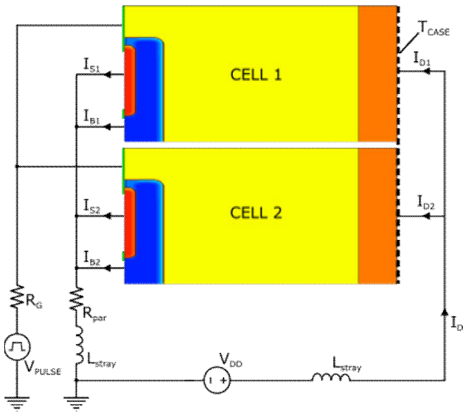


Fig. 3. Diagram of mixed-mode simulated circuit

slightly higher current density than other. As an example, the current is moderately more condensed beneath and around the bonded wires, while outer areas present smaller current density. Therefore, temperature distribution is uniform over a large area, with minor gradients defined by top device structure (pads, metallization, bond wires, etc.). Inside that area, a cluster of cells could be weaker due to inevitably differences created during manufacturing processes. They could be prone to drain more current and eventually almost the all short-circuit current when thermal runaway occurs. Unfortunately, location where hotspot appears is impossible to predict.

Described situation was analysed thanks to electro-thermal (ET) physical simulations. The device was modelled by two parallel cells and was included in a mixed-mode schematic as depicted in Fig.3. The ratio of area factors of two cells was chosen such that:

$$AF_1 + AF_2 = AF_{TOT}$$
$$\frac{AF_1}{AF_2} = 10^4 \quad (1)$$

CELL1 represents almost totally the device, while *CELL2* models the cluster of cells where hotspot might originate, therefore taking into account the filament dimension usually very modest compared to the total area. Moreover, mismatch in some structure parameters was introduced in *CELL2* to make it "weak". A cell can be considered weak if, for any reason, it carries even slightly more current than other cells, hence being more likely to give rise to thermal runaway. It is thus expected that the short-circuit failure current would entirely flow in *CELL2* if thermal runaway sets on. All the results are compared with a single cell structure calibrated on commercial device I_D-V_{GS} curves, used as reference design.

III. RESULTS

Channel peak doping mismatch was first analysed, and results are reported in Fig.4. As the leakage current reaches a critical value, the short-circuit current moves from *CELL1* to flow entirely through *CELL2*, until the device fails. It is visible from Fig.5 where current densities of both cells are reported. At the turn-off (Fig.5a), the current densities in both cells are almost balanced. Afterwards, the current in *CELL1* starts to decrease, while is higher in *CELL2* (Fig.5b). Finally, the weak cell carries all the failure current (Fig.5c) while *CELL1* is completing its turn-off phase. It has to be noted that, as expected, the leakage current is partially formed by hole flowing through the body terminal. The reference cell is able to sustain about 280ns longer SC pulse.

Channel peak doping fluctuation is extremely dependent on technology process, but in this case, a barely 0.75% difference is enough to create a weak cell reducing maximum time sustainable in short-circuit. Obviously, doping variation in real

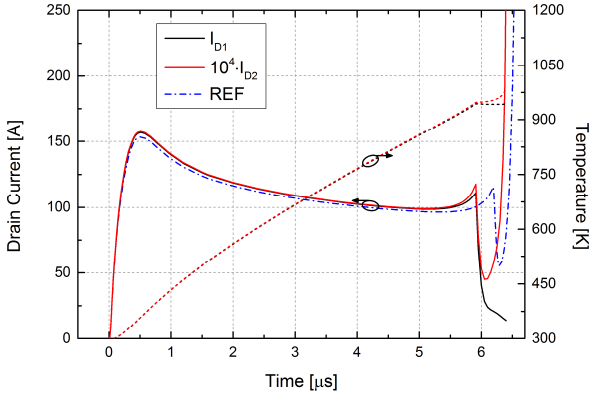


Fig.4. Simulated I_D SC waveforms – channel doping mismatch (V_{DS}=800V; V_{GS}=18V; T_{CASE}=27°C)

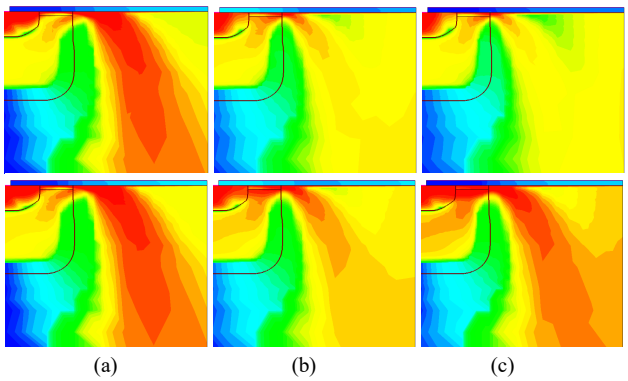


Fig. 5. Current density for *CELL1* (top) and *CELL2* (bottom)

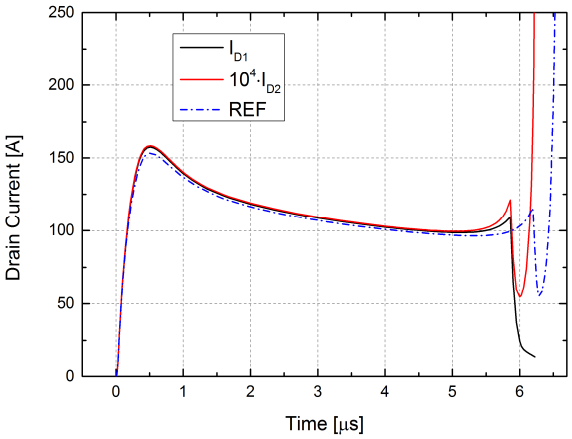


Fig. 6. Simulated I_D SC waveforms – channel length mismatch (V_{DS}=800V; V_{GS}=18V; T_{CASE}=27°C)

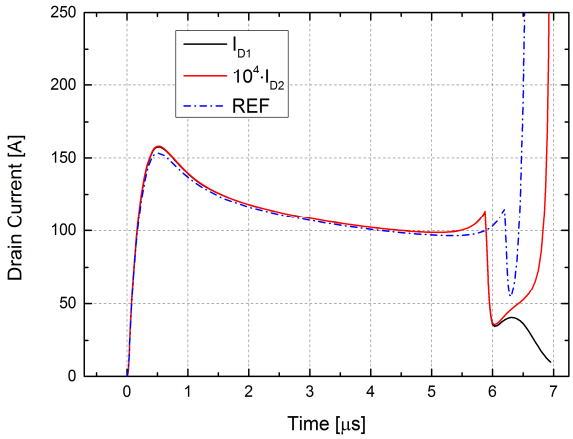


Fig. 7. Simulated I_D SC waveforms – interface traps mismatch (V_{DS}=800V; V_{GS}=18V; T_{CASE}=27°C)

processes are much higher than the value selected, it is therefore clear that areas prone to carry more current could always be present in any device.

Similar result was obtained when the mismatch is introduced in the channel length. Even in this case, an inhomogeneity of 1% leads to current crowding in a portion of the device (i.e. one of the simulated cells) and to a reduced capability of withstand short-circuit of about 300ns (Fig.6).

Finally, the case of different interface traps concentration was taken into account. Many works reported the significant role given by SiO_2/SiC interface defects on devices behaviour, due to their impact on mobility and threshold voltage. Importance lies in the correctly modelling their effect [8] and the development of process in order to reduce their density and produce devices with superior performances [12]. Traps concentration could vary within some orders of magnitude depending on the quality of technology process. In this analysis, a change of 2.5% triggers the failure mechanism about 315ns earlier. Current waveforms are depicted in Fig.7, where it is possible to note that traps also slightly modify the dynamics after the turn-off.

A further simulation was performed considering a structure formed by two full cells, where one of the four channels has a different doping (0.75% smaller peak). The reason is to include, in addition to parameter mismatch, the interaction and the electro-thermal feedback of adjacent cells. Obviously, as the leakage current rises, the weak cell sinks the total device current (I_{S2} in Fig.8). Fig.9 depicts device current density in different time instants. At turn-off edge (Fig.9a), all four cells have almost the same current value. Slight unbalance appears at the beginning of current tails (Fig.9b), but afterwards just *Cell2* exhibits the failure condition (Fig.9c). Moreover, the SC pulse reduction is about 345ns, which is greater than the previous case with two independent cells. This could be addressed because of the aforementioned electro-thermal interaction, which assists the formation of current filament.

Obtained results are summarised in Tab.1, which reports the mismatch percentage together with the reduction of maximum sustainable SC pulse Δt_{SC} (compared with the reference cell).

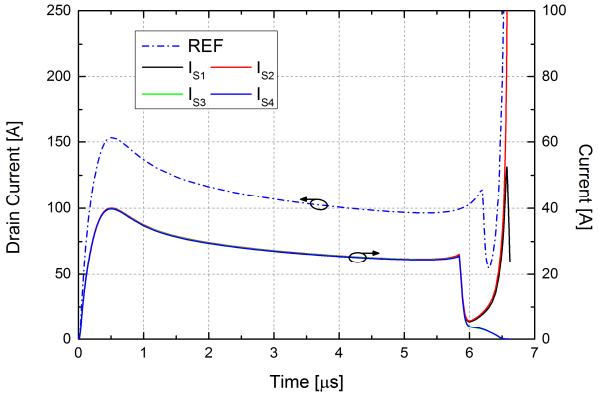


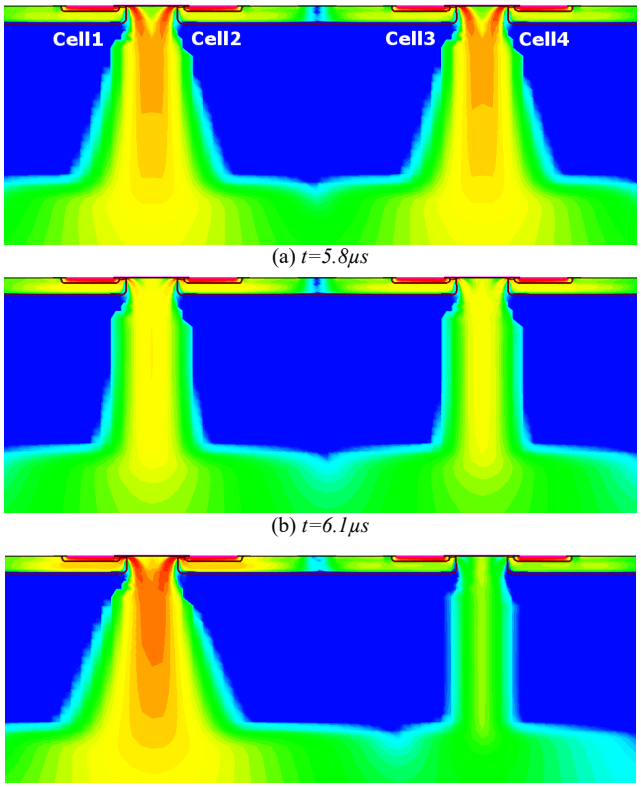
Fig. 8. Simulated current SC waveforms channel doping mismatch, four cells structure (V_{DS}=800V; V_{GS}=18V; T_{CASE}=27°C)

TABLE I.

Parameter	Variation	Δt_{SC}
Channel Doping	0.75%	280ns
Channel Length	1%	300ns
Interface Traps	2.5%	315ns
Channel Doping (four cells structure)	0.75%	345ns

IV. CONCLUSION

In this work, an analysis on possible design parameters mismatch affecting the short-circuit capability of SiC power MOSFETs has been proposed. The failure identified both experimentally and using TCAD simulation, corresponds to the formation of current filament with subsequent elevated energy density dissipated in a reduced area. Due to the mechanism regenerative nature, the current tends to be crowded where non-uniformity among cells creates a hotter (weak) area. Channel doping and length, amount of interface traps were the analysed parameters, which mostly affect SC



(a) *t=5.8µs*

(b) *t=6.1µs*

(c) *t=6.8µs*

Fig. 9. Current density four cells structure (V_{DS}=800V; V_{GS}=18V; T_{CASE}=27°C)

behaviour (since they directly act on V_{TH} and R_{CH}). As reported, even a minimum percentage difference in the aforementioned parameters (mostly unfeasible for current fabrication technology), leads to hot-spot type failure. Process improvements are of paramount importance to develop devices with better and better performances but an accurate choice of some design strategies should be investigated to increase devices short-circuit reliability.

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