Modulation strategies for an open-end winding induction machine fed by a two-output indirect matrix converter

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Abstract — **This paper presents a two-output indirect matrix converter feeding an open-ended winding induction machine. The modulation strategy for the converter input stage, which provides the DC voltage for the output stages, exploits the capability of the input rectifier to produce different DC voltage levels. Moreover, this paper includes a space vector modulation strategy for the converter output stages intended to eliminate the zero sequence load voltage. Furthermore, in order to decrease commutation losses, output stage commutation will take place at reduced voltage when load voltage requirements are low. Modulation strategies and overall system operation are verified via simulation in a PSim/Matlab platform with the machine operating under an open loop *V/f* control strategy. Experimental results are also presented to validate the control strategies.**

***Keywords*—Matrix converters; Space vector pulse width modulation; Variable speed drives; Open-ended winding.**

1. Introduction

In recent years, dual-inverter systems feeding open-ended winding induction motor drives have gained interest because they present several advantages when compared to a standard wye or delta connected induction machine drives. The main features of an open-winding induction machine drive can be summarized as [15]: each inverter is rated at half the machine power because power is supplied to the machine from both winding ends; each phase stator current can be controlled independently; possibility to have twice the effective switching frequency depending on the modulation strategy; extensibility to more phases [1],[3] leading to a phase current reduction; possibility of reducing common-mode voltage [5]; and certain degree of fault tolerance because of the voltage space vector redundancy.

However, an open-ended winding induction machine drive can have some drawbacks, such as [15]: possibility of zero sequence current flowing in the machine because of the occurrence of zero sequence voltage when a single DC supply is used [9]; increased conduction losses; higher complexity in the power converter, i.e. more power devices, circuit gate drives, etc.

Direct-link converters or matrix converters [14], have the distinctive advantages of bidirectional power flow capability, low distorted input currents with small passive input filter and do not require bulky energy storage elements. Moreover, when these converters are used to feed open-ended winding AC machines up to 1.5 times the input phase voltage can be produced across the machine phase windings [12]. In this paper an open-ended winding induction machine supplied by a two-output Indirect Matrix Converter (IMC) is presented. A Space Vector Modulation (SVM) strategy which eliminates the output zero sequence voltage is shown. Moreover, the capability of the input rectifier to produce different virtual DC voltages is exploited [8],[10]. If the virtual DC voltage is reduced, then commutations of the output Voltage Source Inverters (VSI's) can take place at lower voltages, thus reducing commutation losses. Therefore, input stage modulation is used to increase or decrease the DC voltage, depending on the machine operating conditions. Special care is paid in order

not to cause over modulation. The technical feasibility of the proposed topology, modulation strategy and control algorithms is thoroughly validated by means of PSim simulations, considering a *V/f* controlled induction machine. Experimental results are also presented using a 2 kW machine.

2. Power converter topology

The IMC, also known as a direct two-stage power converter, shows similar performance as the standard MC in terms of low distortion input currents, bidirectional power flow and number of devices (18 IGBTs and 18 diodes). The topology is similar to an AC/DC/AC conversion system using two back-to-back VSI converters but without including the bulky capacitors in the DC link. The scheme considers a 3-to-2 matrix converter, a current rectifier converter, at the converter input (the input stage) and a standard VSI at the converter output (the output stage). The IMC could be seen as an extension of early work carried out in the area of developing AC/DC/AC power converters without DC link capacitors [2],[4],[6], using either GTO thyristors or IGBT's to implement unidirectional switches. In those cases, the application of PWM strategies generates input current waveforms similar to the ones obtained in diode rectifier with smooth DC link current. Hence, the input current harmonic content is better than the scheme with a DC link capacitor and input diode converter, but low order harmonics, e.g. 5th and 7th order harmonics, are still present. These low order harmonics can be eliminated if fully bidirectional switches are used in the input rectifier, as it is the case of the IMC, see Fig. 1. In this topology the rectifier provides the DC voltage to the dual-inverter system outputs and is usually controlled to operate with unity displacement power factor at the input. The output of the IMC consists of two standard VSI's. Each inverter can produce eight space voltage vector locations independent of the other, resulting in a total of 64 voltage vector combinations, similar to a three level Neutral Point Clamped (NPC) inverter [13]. The open-end winding machine is connected between both VSI outputs.

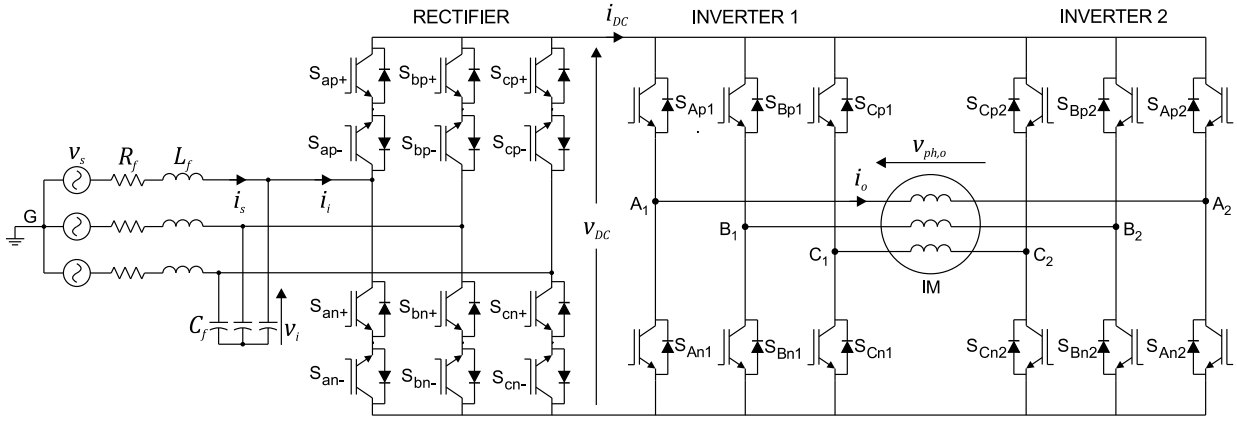


Fig. 1. IMC with one input and two output stages feeding an open-end winding induction machine.

The space vectors for inverter 1 are shown in Table 1; the same space vectors are valid for inverter 2 but with superscript 2.

Table 1. Switching states of the individual inverter

States of inverter 1 $[S_{A1}\ S_{B1}\ S_{C1}]$			
$V_1^1 = [1\ 0\ 0]$	$V_2^1 = [1\ 1\ 0]$	$V_3^1 = [0\ 1\ 0]$	$V_4^1 = [0\ 1\ 1]$
$V_5^1 = [0\ 0\ 1]$	$V_6^1 = [1\ 0\ 1]$	$V_7^1 = [1\ 1\ 1]$	$V_8^1 = [0\ 0\ 0]$

Let $V_{ij} = \left[V_i^1 V_j^2\right]$ with $i, j = 1 \ldots 8$, be the phase voltage vector combination of the dual-inverter output, hence a diagram of the vector locations is shown in Fig. 2 where the availability of redundant switching states for some voltage space vectors of the dual-inverter can be noted.

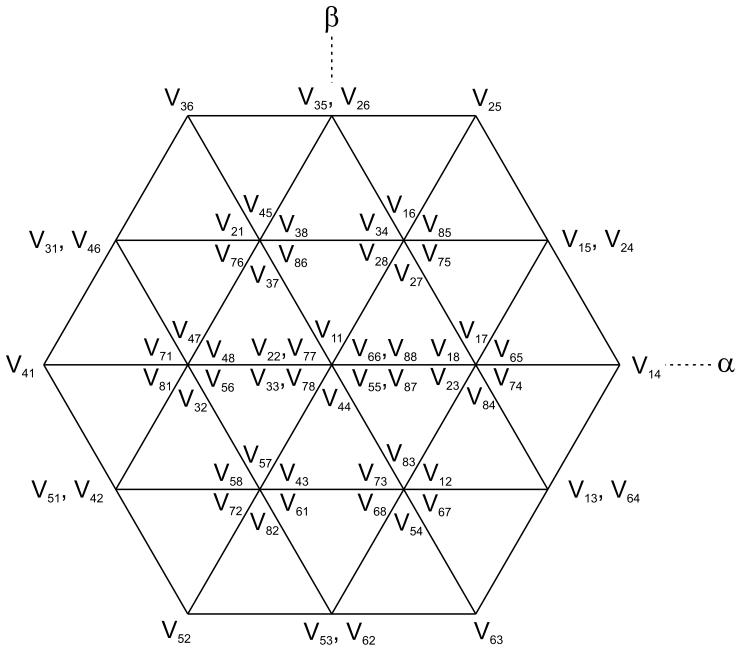


Fig. 2. Alpha-beta space vector locations of the dual-inverter scheme.

3. Modulation for the input stage of the IMC

The modulation for the input (rectifier) stage of the converter aims to obtain a positive DC link voltage in each sampling period and unity displacement factor at the input [7]. Moreover, the duty cycles used in the switching pattern should create sinusoidal currents at the converter input. Two different SVM strategies can be used in the rectifier [8]**Error! Reference source not found.** and the possible DC link voltage waveforms are shown in Fig. 3.

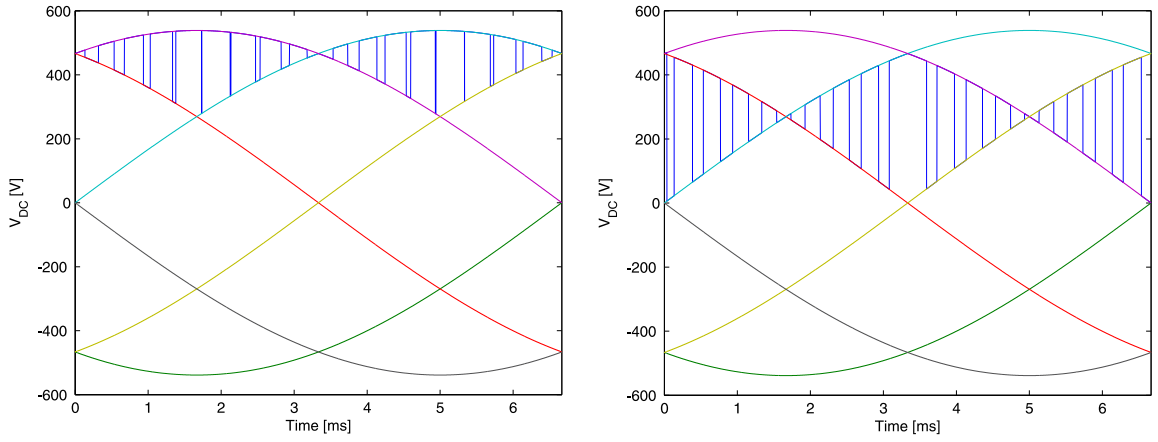
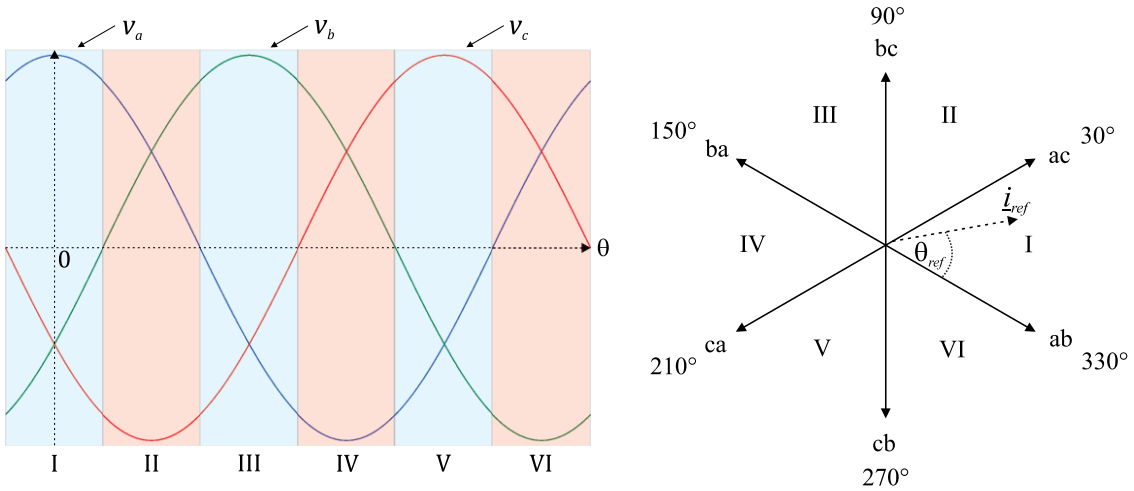


Fig. 3. a) Maximum DC voltage. b) Reduced DC voltage.

In order to obtain unity input displacement factor, the current reference vector is aligned with the vector corresponding to the converter input voltage. Hence three phase signals, corresponding to the converter input voltages, are used in the modulation strategies for the input rectifier.

3.1. Modulation strategy for maximum DC voltage

To maximize the DC link voltage, the sectors defined in Fig. 4 are considered, where $\underline{i}_{ref}$ is the current reference vector. It can be noted in Fig. 4a that in each sector there is one positive phase voltage and two negative phase voltages, or vice versa. The operation relies on keeping the upper (or lower) switch corresponding to the highest absolute value of the input phase voltages closed and the commutating the two lower (or upper) switches corresponding to the other input phase voltages; this results in a DC voltage composed of segments of the highest input line-to-line voltages in each sector (Fig. 3a).



a) b)

Fig. 4. a) Sectors defined by the input voltages and b) Locus of sectors and vectors for maximum DC voltage.

Defining the rectifier phase input currents i_{ia}, i_{ib} and i_{ic}, according to Fig. 4b, in Sector I the input phase currents in one switching interval are given by:

$$i_{ia} = (d_{ab} + d_{ac})i_{DC} \tag{1}$$

$$i_{ib} = -d_{ab} i_{DC} \tag{2}$$

$$i_{ic} = -d_{ac} i_{DC} \tag{3}$$

where i_{DC} is the DC link current and d_{ij} $(i, j = a, b, c)$ are the duty cycles for the input stage devices, with the first letter denoting the phase of the upper closed switch and the second letter the phase of the lower closed switch.

From (1)-(3) for Sector I the duty cycles are:

$$d_{ab} + d_{ac} = \frac{i_{ia}}{i_{DC}}; \quad d_{ab} = -\frac{i_{ib}}{i_{DC}}; \quad d_{ac} = -\frac{i_{ic}}{i_{DC}} \tag{4}$$

Because the zero current vectors are not used, the duty cycles need to satisfy the following relationship:

$$d_{ab} + d_{ac} = 1 \tag{5}$$

which implies, from eq. (4), that $i_{DC} = i_a$. Then the duty cycles are given by

$$d_{ab} = -\frac{i_{ib}}{i_{ia}}; \quad d_{ac} = -\frac{i_{ic}}{i_{ia}} \tag{6}$$

For unity displacement factor, the reference input currents are in phase with the phase input voltages, therefore the duty cycles of eq. (6) can be rewritten as:

$$d_{ab} = -\frac{i_{ib}}{i_{ia}} = -\frac{\cos(\theta - 120°)}{\cos(\theta)} \Longrightarrow d_{ab} = \frac{\sin(30° - \theta)}{\cos(\theta)} \tag{7}$$

$$d_{ac} = -\frac{i_{ic}}{i_{ia}} = -\frac{\cos(\theta + 120°)}{\cos(\theta)} \Longrightarrow d_{ac} = \frac{\sin(150° - \theta)}{\cos(\theta)} \tag{8}$$

with $\theta = 2\pi f$, where $f = 50\ Hz$ is the supply frequency. Considering the sector angle of the reference vector θ_{ref}, and defining $d_{ab} = d_{\gamma}^{R}$ and $d_{ac} = d_{\delta}^{R}$ then [10]**Error! Reference source not found.**:

$$d_{\gamma}^{R} = \frac{\sin(60° - \theta_{ref})}{\sin(60° - \theta_{ref}) + \sin(\theta_{ref})} \quad , \quad d_{\delta}^{R} = \frac{\sin(\theta_{ref})}{\sin(60° - \theta_{ref}) + \sin(\theta_{ref})} \tag{9}$$

and defining

$$d_\gamma = \sin(60° - \theta_{ref}) \quad , \quad d_\delta = \sin(\theta_{ref}) \tag{10}$$

eq. (9) can be rewritten as:

$$d_\gamma^R = \frac{d_\gamma}{d_\gamma + d_\delta} \quad , \quad d_\delta^R = \frac{d_\delta}{d_\gamma + d_\delta} \tag{11}$$

This result in a variable average DC voltage in each sampling time, given by:

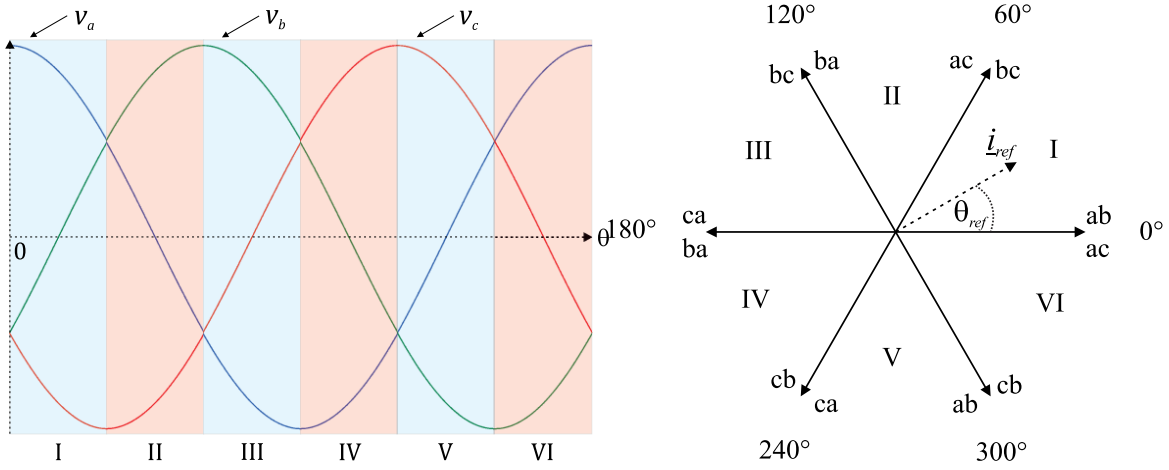
$$\bar{V}_{DC} = \frac{\sqrt{3}}{2} \frac{V_{line,in}}{d_\gamma + d_\delta} \tag{12}$$

where $V_{line,in}$ is the RMS line-to-line input voltage.

Further details about this modulation strategy can be found in [7], [10].

3.2. Modulation strategy for reduced DC voltage

If a reduced DC link voltage is required, the sectors defined in Fig. 5 should be considered. As can be seen in Fig. 5a, in each sector there is a positive voltage, a negative voltage and a voltage changing from positive to negative, or vice versa. In this case, in contrast to the modulation for maximum DC voltage, there are commutations in both the upper and lower switches of the converter in each sector. The result is a DC voltage composed of segments of the lower input line-to-line voltages (Fig. 3b).



a) b)

Fig. 5. a) Sectors defined by the input voltages and b) Locus of sectors and vectors for reduced DC voltage.

According to Fig. 5b, in Sector I the input phase currents in one switching interval are given by:

$$i_{ia} = d_{ab} i_{DC} \tag{13}$$

$$i_{ib} = (d_{bc} - d_{ab}) i_{DC} \tag{14}$$

$$i_{ic} = -d_{bc} i_{DC} \tag{15}$$

Considering (13)-(15), the duty cycles for Sector I are:

$$d_{bc} - d_{ab} = \frac{i_{ib}}{i_{DC}}; \quad d_{ab} = \frac{i_{ia}}{i_{DC}}; \quad d_{bc} = -\frac{i_{ic}}{i_{DC}} \tag{16}$$

Moreover, as the zero current vectors are again not used:

$$d_{ab} + d_{bc} = 1 \Longrightarrow d_{bc} = 1 - d_{ab} \Longrightarrow i_{ib} = (1 - 2d_{ab}) i_{DC} \tag{17}$$

and with (16) and (17), the DC current can be obtained:

$$i_{ib} = (1 - 2d_{ab}) i_{DC} \Longrightarrow i_b = i_{DC} - 2d_{ab} i_{DC} \tag{18}$$

$$i_{DC} = 2i_{ia} + i_{ib} = i_{ia} - i_{ic} = i_{iac} \tag{19}$$

Then, the duty cycles for Sector I are:

$$d_{ab} = \frac{i_{ia}}{i_{iac}}; \quad d_{bc} = -\frac{i_{ic}}{i_{iac}} \tag{20}$$

To obtain unity displacement factor at the converter input, (20) can be rewritten as:

$$d_{ab} = \frac{i_{ia}}{i_{iac}} \Longrightarrow d_{ab} = \frac{\cos(\theta)}{\cos(\theta) - \cos(\theta + 120°)} \tag{21}$$

$$d_{bc} = -\frac{i_{ic}}{i_{iac}} \Longrightarrow d_{bc} = -\frac{\cos(\theta + 120°)}{\cos(\theta) - \cos(\theta + 120°)} \tag{22}$$

Considering the reference vector angle θ_{ref}, then defining $d_{ab} = d_{\gamma}^{R}$ and $d_{bc} = d_{\delta}^{R}$ then:

$$d_{\gamma}^{R} = \frac{\cos(\theta_{ref})}{\cos(\theta_{ref}) + \cos(60° - \theta_{ref})} \quad , \quad d_{\delta}^{R} = \frac{\cos(60° - \theta_{ref})}{\cos(\theta_{ref}) + \cos(60° - \theta_{ref})} \tag{23}$$

and defining

$$d_{\gamma} = \cos(\theta_{ref}) \quad , \quad d_{\delta} = \cos(60° - \theta_{ref}) \tag{24}$$

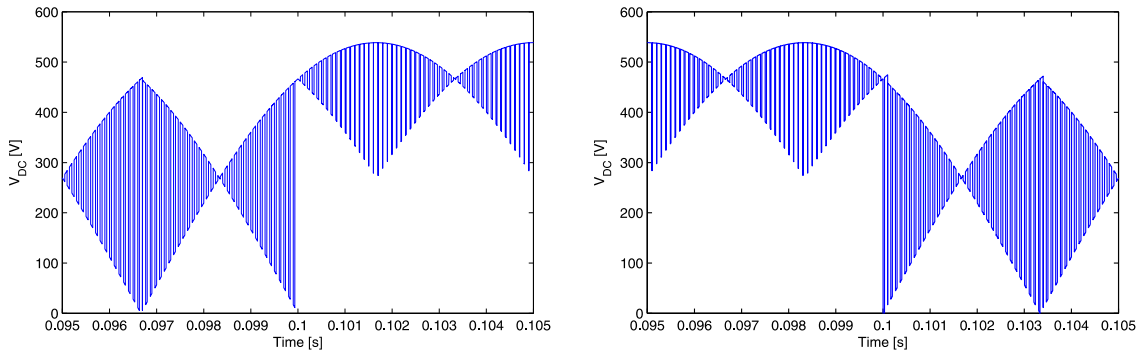
the duty cycles d_{γ}^{R} and d_{δ}^{R} are given by (11).

In this case the variable average DC voltage is given by [7], [10]:

$$\bar{V}_{DC} = \frac{1}{2}\frac{V_{line,in}}{d_\gamma + d_\delta} \tag{25}$$

Further information about this modulation strategy can be found in [7], [10].

Fig. 6a shows a transition from reduced DC voltage to maximum DC voltage and Fig. 6b shows the opposite situation.



a) b)

Fig. 6. Transition between both rectifier modulation strategies.

The rectifier SVM for reduced DC link voltage decreases the voltage gain by $\sqrt{3}$. Thus, the transition between reduced and maximum DC link voltage should take place when the output voltage reference is higher than $\frac{1.5}{\sqrt{3}} \cdot V_{ph,\,input} = 0.866 \cdot V_{ph,\,input}$, where $V_{ph,\,input}$ is the converter input phase voltage. Further details about the modulations for the input stage can be found in [7], [10].

4. Modulation for the output stages of the IMC

In an open-ended winding machine fed by two independent and isolated voltage sources there will be no zero sequence current circulation; however, further hardware is needed which increases the cost and volume of the drive. On the other hand, the topology proposed in this paper could produce the circulation of zero sequence currents because of zero sequence voltages applied to the machine phase winding. However, zero sequence voltages can be eliminated or reduced by using a suitable modulation strategy.

In general, the zero sequence voltage at the machine terminals can be defined as:

$$v_{zs} = \frac{v_{A1A2} + v_{B1B2} + v_{C1C2}}{3} \tag{26}$$

where v_{A1A2}, v_{B1B2} and v_{C1C2} are the instantaneous machine phase voltages. Since the output phase voltage $v_{ph,o}$ can be obtained as:

$$v_{ph,ok} = v_{DC}(S_{k1} - S_{k2}) \text{ with } k = A, B, C \tag{27}$$

where S_{k1} and S_{k2} $(k = A, B, C)$ are the phase switching functions of inverter 1 and inverter 2, respectively, and v_{DC} is the DC link voltage, the output zero sequence voltage can be expressed as:

$$v_{zs} = \frac{1}{3}\sum_{k=A,B,C} v_{ph,ok} = \frac{v_{DC}}{3}\sum_{k=A,B,C}(S_{k1} - S_{k2}) \tag{28}$$

Thus, in order to make $v_{zs} = 0$, the following relationship must be satisfied:

$$\sum_{k=A,B,C} S_{k1} = \sum_{k=A,B,C} S_{k2} \tag{29}$$

Therefore, in order to eliminate the instantaneous zero sequence voltage in the load is necessary and sufficient to have the same number of upper (or lower) switches closed on both output inverters at every switching period.

The dual-inverter topology can produce 64 space voltage vectors locations. It can be found that there are two different but totally equivalent sets of active vectors which do not produce zero sequence voltages [11]; these sets are given in Table 2 where $V_{ij} = [S_{Ap1}\ S_{Bp1}\ S_{Cp1}\ S_{Ap2}\ S_{Bp2}\ S_{Cp2}]$ with $i, j = 1 \ldots 8$, is a space vector combination of the dual inverter.

Table 2. Sets of active vectors which do not produce zero sequence voltage

Set 1		Set 2	
$V_{15} = [1\ 0\ 0\ 0\ 0\ 1]$	$V_{51} = [0\ 0\ 1\ 1\ 0\ 0]$	$V_{24} = [1\ 1\ 0\ 0\ 1\ 1]$	$V_{42} = [0\ 1\ 1\ 1\ 1\ 0]$

$V_{35} = [0\ 1\ 0\ 0\ 0\ 1]$	$V_{53} = [0\ 0\ 1\ 0\ 1\ 0]$	$V_{26} = [1\ 1\ 0\ 1\ 0\ 1]$	$V_{62} = [1\ 0\ 1\ 1\ 1\ 0]$
$V_{31} = [0\ 1\ 0\ 1\ 0\ 0]$	$V_{13} = [1\ 0\ 0\ 0\ 1\ 0]$	$V_{46} = [0\ 1\ 1\ 1\ 0\ 1]$	$V_{64} = [1\ 0\ 1\ 0\ 1\ 1]$

A representation of the locus formed by the space vectors producing null v_{zs} is shown in Fig. 7 where it can be seen that the hexagon is divided into six sectors and among the eight null vectors available, only six are finally used (three null vectors per set) in order to reduce the commutations in a period [12]. Moreover the null vectors should be mapped depending on the sector information [12]; the mapping is shown in Table 3.

Table 3. Mapping of zero vectors

Sector	I	II	III	IV	V	VI
Set 1 zero vectors	V_{11}	V_{55}	V_{33}	V_{11}	V_{55}	V_{33}
Set 2 zero vectors	V_{44}	V_{22}	V_{66}	V_{44}	V_{22}	V_{66}

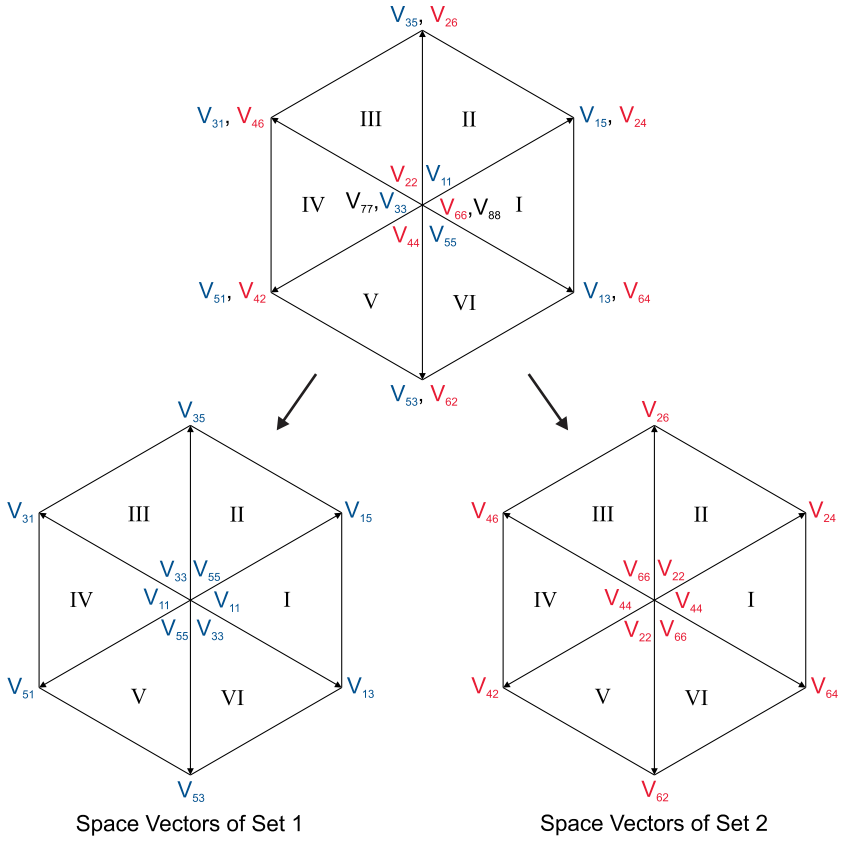


Fig. 7. Locus of vectors producing null zero sequence voltage.

The duty cycles for the output stages are calculated using standard SVM as [7], [10]:

$$d_\alpha = m(t)\sin\left(\pi/3 - \theta_{ref,o}\right),\ d_\beta = m(t)\sin\left(\theta_{ref,o}\right) \text{ and } d_0 = 1 - d_\alpha - d_\beta \tag{30}$$

where $\theta_{ref,o}$ is the angle of the output reference voltage space vector and $m(t)$ is a variable modulation index, because of the variable average DC voltage, given by:

$$m(t) = \frac{\hat{V}_o}{\bar{V}_{DC}} \tag{31}$$

with $\hat{V}_o$ the peak value of the output reference voltage and $\bar{V}_{DC}$ the average value of the DC link voltage (see (12) and (25)). Therefore, the eq. (31) can be rewritten as:

$$m(t) = \frac{\hat{V}_o}{kV_{line,in}}\left(d_\gamma + d_\delta\right) \tag{32}$$

where k is $\sqrt{3}/2$ or $1/2$ depending on the modulation used for the input rectifier. Defining a constant modulation index m_o as:

$$m_o = \frac{\hat{V}_o}{kV_{line,in}} \qquad 0 \le m_o \le 1 \tag{33}$$

The duty cycles for the output stages result in:

$$d_\alpha = m_o\left(d_\gamma + d_\delta\right)\sin\left(\pi/3 - \theta_{ref,o}\right) \tag{34}$$

$$d_\beta = m_o\left(d_\gamma + d_\delta\right)\sin\left(\theta_{ref,o}\right) \tag{35}$$

$$d_0 = 1 - d_\alpha - d_\beta \tag{36}$$

To obtain a correct balance of the input currents and the output voltages in a switching period, the modulation pattern should produce all combinations of the rectification and the inversion switching states [7], resulting in the following duty cycles for the active vectors:

$$d_{\alpha\gamma} = d_\alpha d_\gamma^R\ ,\ d_{\beta\gamma} = d_\beta d_\gamma^R\ , d_{\alpha\delta} = d_\alpha d_\delta^R\ ,\ d_{\beta\delta} = d_\beta d_\delta^R \tag{37}$$

The total zero vector duty cycle is:

$$d_0 = 1 - d_\alpha - d_\beta \tag{38}$$

and the combined zero vector duty cycles:

$$d_{0\gamma} = d_0 d_\gamma^R\ ,\ d_{0\delta} = d_0 d_\delta^R \tag{39}$$

The duty cycles are the same for both output stages of the power converter and considering the vectors of Set 1 (see Tables 2 and 3), the switching sequence of each sector is given by Table 4.

Table 4. Mapping of zero vectors

	Sector I								**Sector II**							
	d_γ^R				d_δ^R				d_γ^R				d_δ^R			
	$\frac{d_{0\gamma}}{2}$	$d_{\alpha\gamma}$	$d_{\beta\gamma}$	$\frac{d_{0\gamma}}{2}$	$\frac{d_{0\delta}}{2}$	$d_{\beta\delta}$	$d_{\alpha\delta}$	$\frac{d_{0\delta}}{2}$	$\frac{d_{0\gamma}}{2}$	$d_{\alpha\gamma}$	$d_{\beta\gamma}$	$\frac{d_{0\gamma}}{2}$	$\frac{d_{0\delta}}{2}$	$d_{\beta\delta}$	$d_{\alpha\delta}$	$\frac{d_{0\delta}}{2}$
INV 1	V_1^1	V_1^1	V_1^1	V_1^1	V_1^1	V_1^1	V_1^1	V_1^1	V_5^1	V_1^1	V_3^1	V_5^1	V_5^1	V_3^1	V_1^1	V_5^1
INV 2	V_1^2	V_3^2	V_5^2	V_1^2	V_1^2	V_5^2	V_3^2	V_1^2	V_5^2	V_5^2	V_5^2	V_5^2	V_5^2	V_5^2	V_5^2	V_5^2
	Sector III								**Sector IV**							
	d_γ^R				d_δ^R				d_γ^R				d_δ^R			
	$\frac{d_{0\gamma}}{2}$	$d_{\alpha\gamma}$	$d_{\beta\gamma}$	$\frac{d_{0\gamma}}{2}$	$\frac{d_{0\delta}}{2}$	$d_{\beta\delta}$	$d_{\alpha\delta}$	$\frac{d_{0\delta}}{2}$	$\frac{d_{0\gamma}}{2}$	$d_{\alpha\gamma}$	$d_{\beta\gamma}$	$\frac{d_{0\gamma}}{2}$	$\frac{d_{0\delta}}{2}$	$d_{\beta\delta}$	$d_{\alpha\delta}$	$\frac{d_{0\delta}}{2}$
INV 1	V_3^1	V_3^1	V_3^1	V_3^1	V_3^1	V_3^1	V_3^1	V_3^1	V_1^1	V_3^1	V_5^1	V_1^1	V_1^1	V_5^1	V_3^1	V_1^1
INV 2	V_3^2	V_5^2	V_1^2	V_3^2	V_3^2	V_1^2	V_5^2	V_3^2	V_1^2	V_1^2	V_1^2	V_1^2	V_1^2	V_1^2	V_1^2	V_1^2
	Sector V								**Sector VI**							
	d_γ^R				d_δ^R				d_γ^R				d_δ^R			
	$\frac{d_{0\gamma}}{2}$	$d_{\alpha\gamma}$	$d_{\beta\gamma}$	$\frac{d_{0\gamma}}{2}$	$\frac{d_{0\delta}}{2}$	$d_{\beta\delta}$	$d_{\alpha\delta}$	$\frac{d_{0\delta}}{2}$	$\frac{d_{0\gamma}}{2}$	$d_{\alpha\gamma}$	$d_{\beta\gamma}$	$\frac{d_{0\gamma}}{2}$	$\frac{d_{0\delta}}{2}$	$d_{\beta\delta}$	$d_{\alpha\delta}$	$\frac{d_{0\delta}}{2}$
INV 1	V_5^1	V_5^1	V_5^1	V_5^1	V_5^1	V_5^1	V_5^1	V_5^1	V_3^1	V_5^1	V_1^1	V_3^1	V_3^1	V_1^1	V_5^1	V_3^1
INV 2	V_5^2	V_1^2	V_3^2	V_5^2	V_5^2	V_3^2	V_1^2	V_5^2	V_3^2	V_3^2	V_3^2	V_3^2	V_3^2	V_3^2	V_3^2	V_3^2

It can be noted in Table 4 that in each sector one inverter keeps clamped in a switching state while the other inverter commutates. This allows reducing the switching losses of the IMC output stages. On the other hand it is worth stressing that the input stage has zero current soft switching for almost negligible input stage switching losses.

5. Simulation results

The modulation strategies proposed have been simulated using PSim/Matlab. The simulation has been performed for an open-end winding induction machine fed by a two-output IMC with open loop V/f control strategy. Table 5 shows the simulation parameters and Fig. 8 shows the modulation and control system.

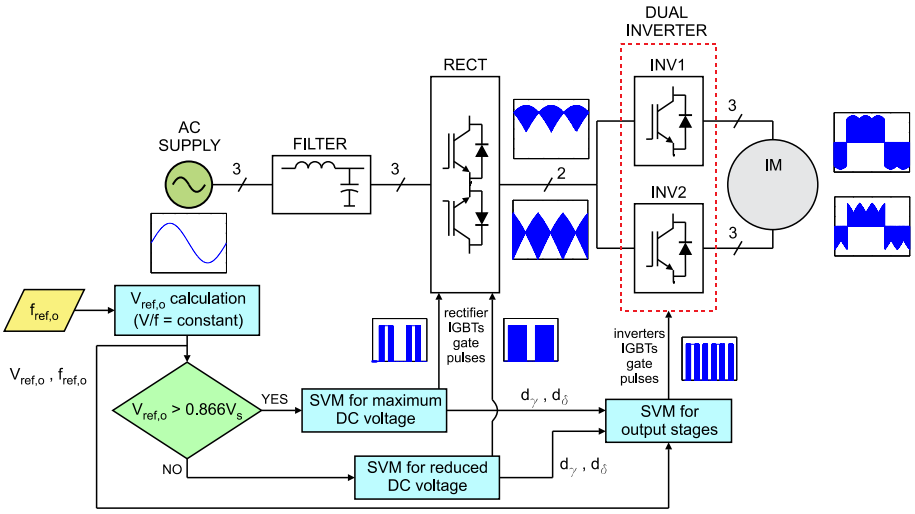


Fig. 8. Modulation and control system.

The modulation index m_o is limited to avoid going into overmodulation in the output stages. In this condition the output phase voltage achieved across the windings can be at most 1.5 times the supply phase voltage (220 V RMS). A flow diagram of the simulation scheme is shown in Fig. 9.

Table 5. Simulation Parameters

Variables	Description	Value	Variables	Description	Value
V_s	Phase source voltage	220 V	R_s	Stator resistance	0.8 Ω
f	Source frequency	50 Hz	R_r	Rotor resistance	1.0 Ω
C_f	Input filter capacitance	12 µF	L_s	Stator self inductance	0.100 H
L_f	Input filter inductance	0.5 mH	L_r	Rotor self inductance	0.100 H
f_s	Switching frequency	10 kHz	L_m	Magnetizing inductance	0.075 H
P_m	Machine power	5 kW			

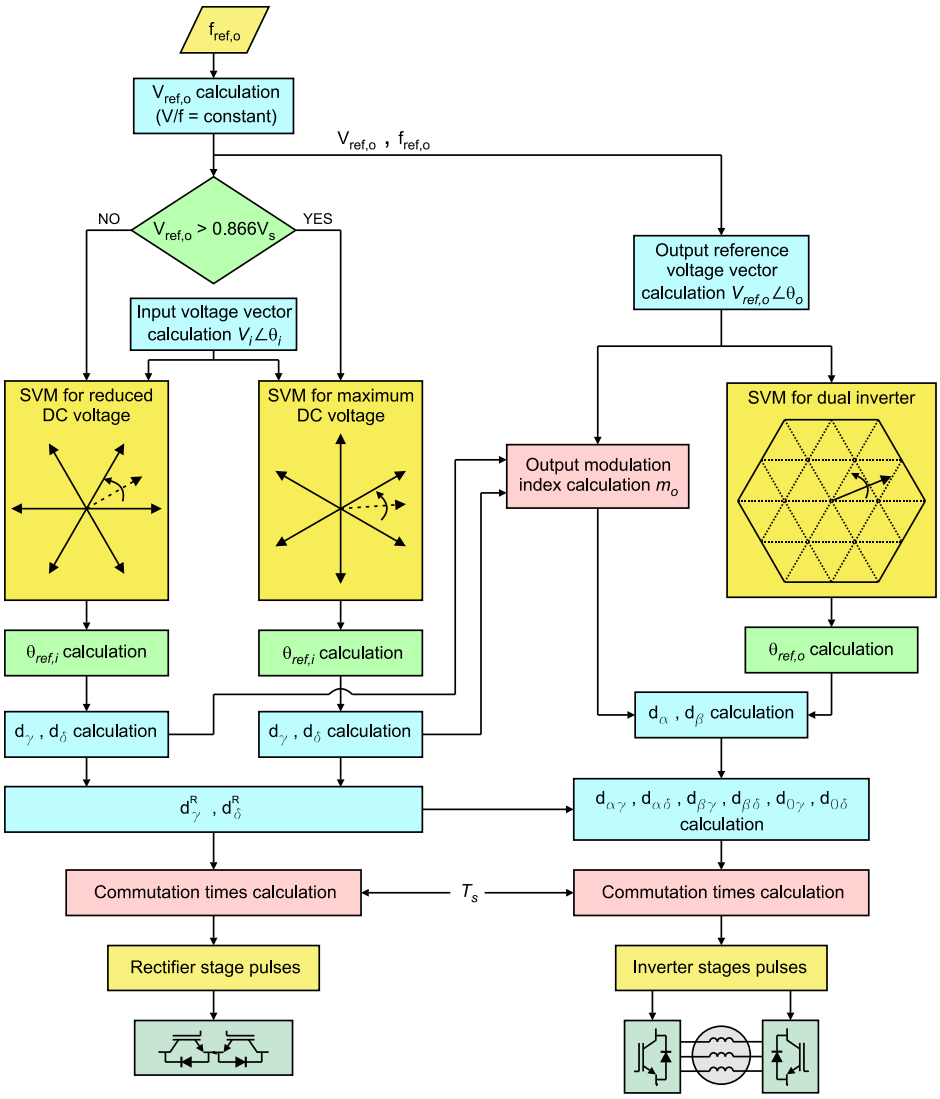


Fig. 9. Flow diagram of the simulation scheme.

The performance of the system is verified for reference output frequencies of 25 Hz (Figs. 10 - 12) and 50 Hz (Figs. 13 - 15); the corresponding voltage references are 165 V and 330 V. Fig. 10 shows the phase-*a* voltage (top) and machine currents (bottom).

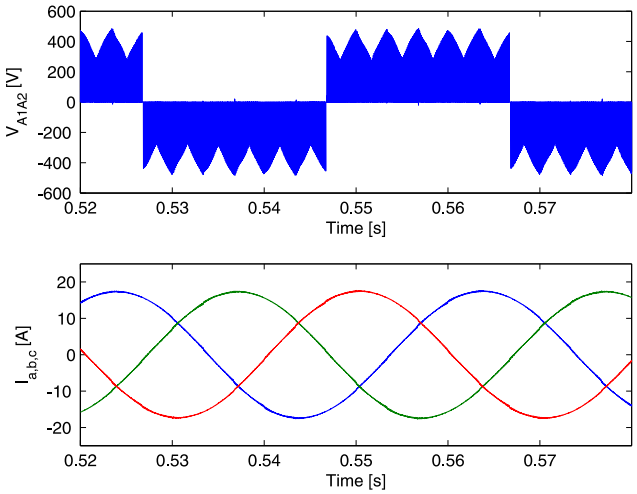


Fig. 10. Machine phase voltage (top) and currents (bottom) for reduced DC voltage.

The reduced DC link voltage and its frequency spectrum are shown in Fig. 11 top and bottom, respectively.

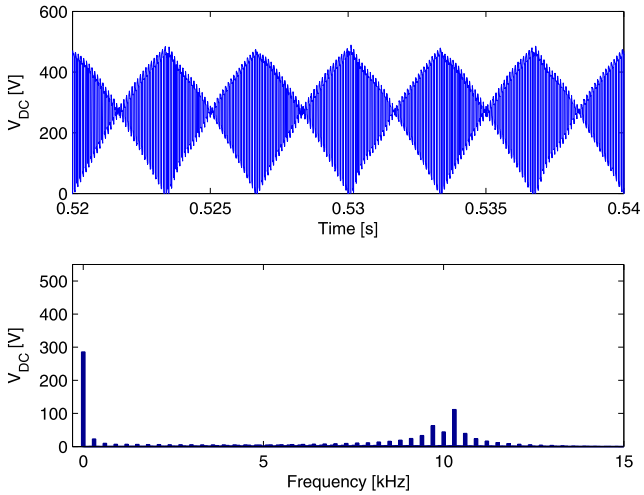


Fig. 11. Reduced DC voltage (top) and its frequency spectrum (bottom).

Fig. 12 (top) shows the input source currents. A distortion occurring every 60° (when a rectifier sector change takes place) can be appreciated; this distortion can be reduced by increasing the input filter damping. Fig. 12 (bottom) shows the input phase voltage and current where the unity displacement factor operation can be noted.

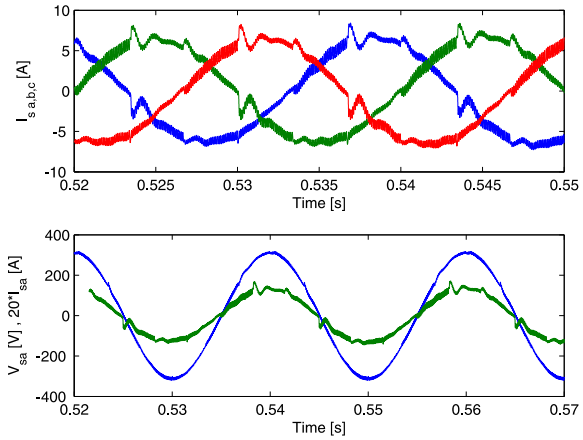


Fig. 12. Input currents (top) and input phase voltage and current (bottom) for reduced DC voltage.

The phase-a voltage (top) and machine currents (bottom) for the rectifier producing maximum DC voltage are shown in Fig. 13 (top).

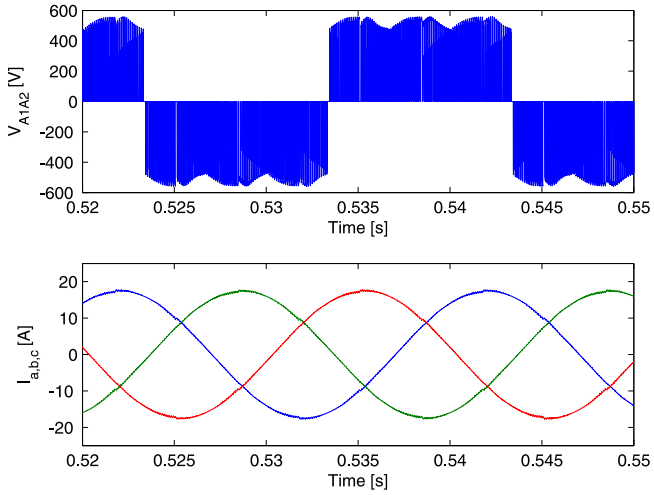


Fig. 13. Machine phase voltage (top) and currents (bottom) for maximum DC voltage.

The maximum DC voltage is shown in Fig. 14 along with its frequency spectrum. A lower harmonic distortion can be appreciated in comparison with the spectrum shown in Fig. 11 (bottom) for reduced DC voltage.

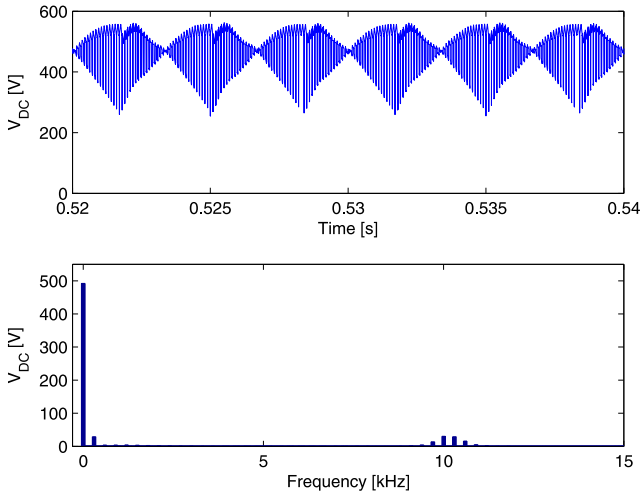


Fig. 14. Maximum DC voltage (top) and its frequency spectrum (bottom).

The input currents are shown in Fig. 15 (top). The distortion occurring every 60° is lower than when operating with reduced DC voltage. The input displacement factor is unity as can be seen in Fig. 15 (bottom).

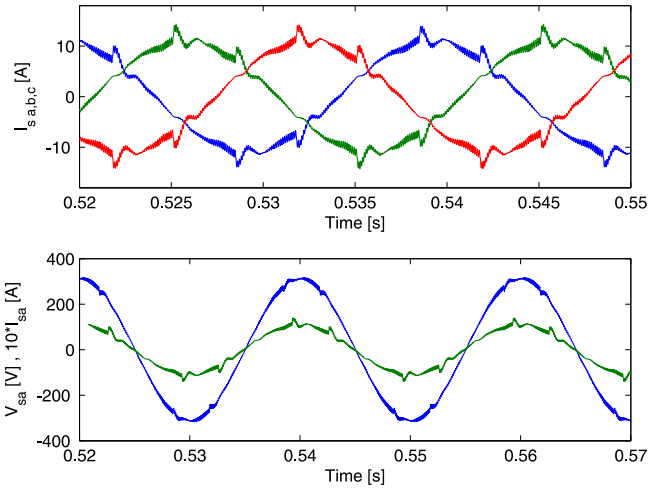


Fig. 15. Input currents (top) and input phase voltage and current (bottom) for maximum DC voltage.

Regarding the input filter of the power converter and the $L_f - C_f$ parameters given in Table 5, the cut-off frequency is given by:

$$f_c = \frac{1}{2\pi\sqrt{L_f C_f}} = \frac{1}{2\pi\sqrt{0.5 \cdot 10^{-3} \cdot 12 \cdot 10^{-6}}} = 2055\ Hz \tag{40}$$

Therefore, as the switching frequency of the power converter is 10 kHz, the high order harmonics of the rectifier input current shown in Fig. 16 (top - green waveform) are appropriately filtered out, as can be noted from the supply current shown in Fig. 16 (bottom). The filter capacitor voltage is also shown in Fig. 16 (top – blue waveform).

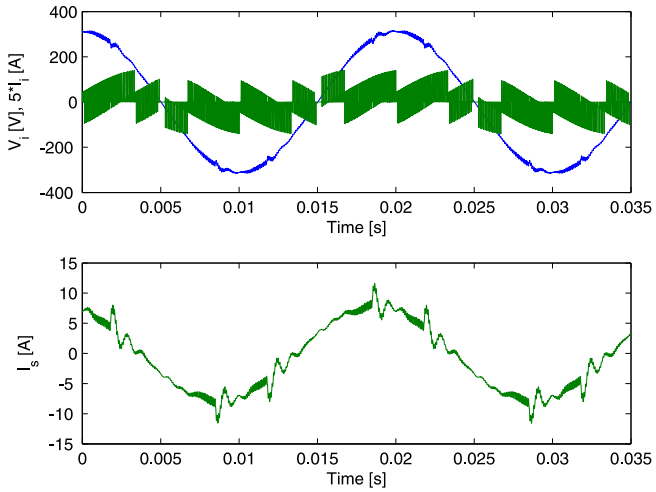


Fig. 16. Rectifier input current and filter capacitor voltage (top). Source current (bottom).

Finally, Fig. 17 shows the zero sequence voltage which is eliminated for both rectifier modulation strategies, because it depends only on the modulation for the output inverters (see section 4).

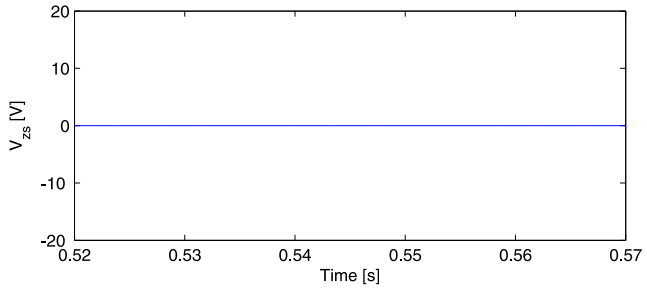


Fig. 17. Zero sequence voltage.

6. Experimental results

Preliminary experimental results for open-loop operation have been obtained using the system shown

in Fig. 18. A six-pole induction machine rated at 2 kW is used. A DSP board, based on the TMS320C6713 processor, is used as the control platform. The calculation of duty cycles is carried out on the DSP among several other tasks. An interface board, based on an FPGA, is used to implement the modulation strategies and data acquisition. Communication between the DSP and a PC is achieved using a DSK6713HPI (Host Port Interface) daughter card. The converter input stage uses SK60GM123 modules and the output stages use SK35GD126 modules. The switching frequency and the sampling frequency of input voltages, is 10 kHz. Voltages and currents have been measured using a Yokowaga DL850 ScopeCorder, using four two channel, 12 bit, high speed 100Ms/s modules for voltage measurements and two 12 bit, two channel, 10Ms/s modules for current measurements. The experimental setup parameters are shown in Table 6.

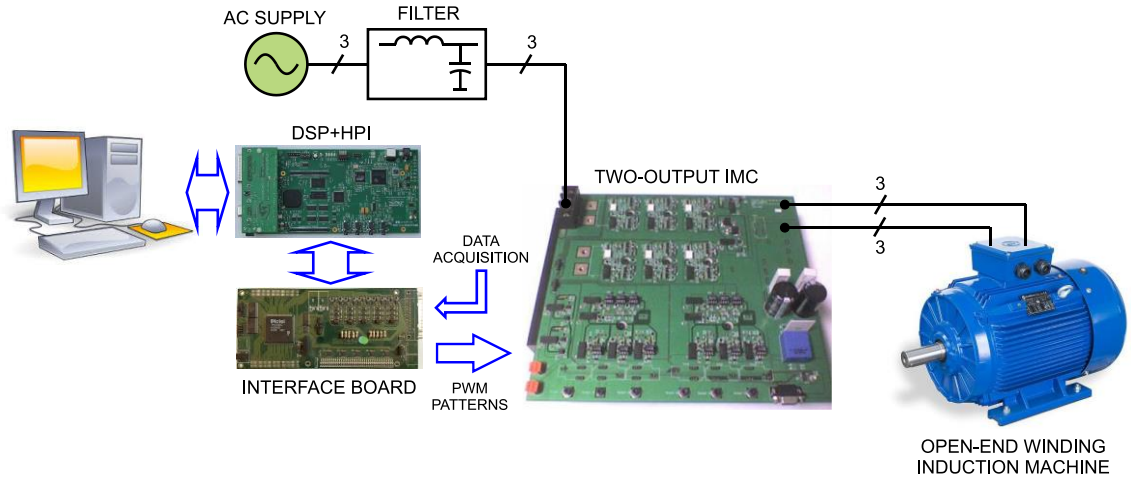


Fig. 18. Experimental system.

Table 6. Experimental Parameters

Variables	Description	Value
V_s	Phase source voltage	90 V
f	Source frequency	50 Hz
C_f	Input filter capacitance	6 µF
L_f	Input filter inductance	0.5 mH
f_s	Switching frequency	10 kHz
P_m	Machine power	2 kW

A transition between reduced and maximum DC link voltage is shown in Fig. 19 (top). The corresponding output phase voltage is shown in Fig. 19 (bottom).

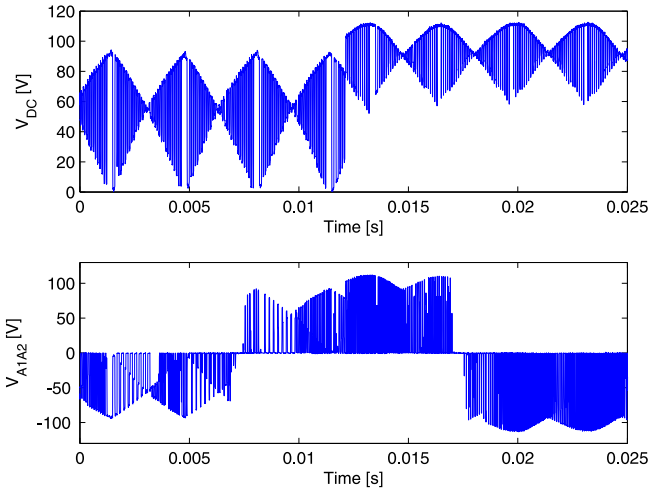


Fig. 19. DC link voltage (top) and output phase voltage (bottom) for a transition between both rectifier modulation strategies.

For 50 Hz operation, the rectifier is modulated to obtain maximum DC voltage. In this case the voltages of the three machine windings are shown in Fig. 20 while Fig. 21 shows the zero sequence voltage produced (calculated by (26)). As can be noted, the zero sequence voltage is not exactly zero but this is probably due to the measurement procedure because not all of the channels are sampled at the same time and because in the simulation system the switches are considered ideal.

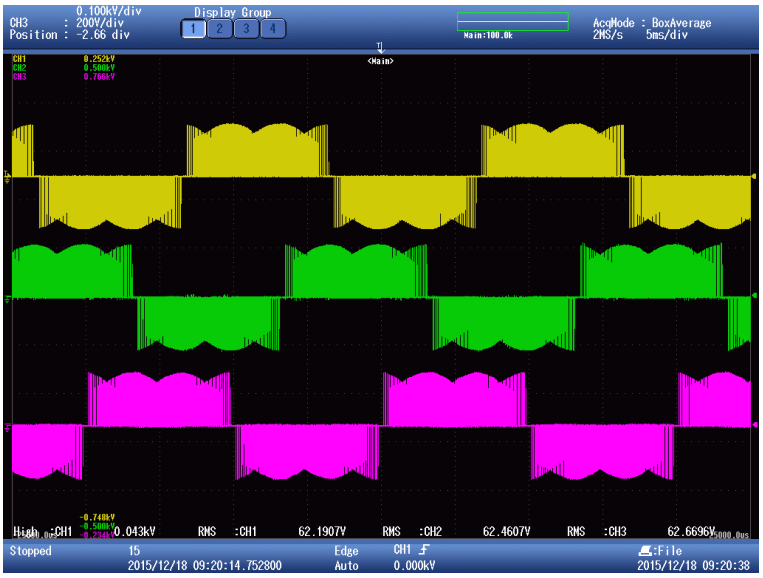


Fig. 20. Machine phase voltages. Scales: 200 V/div, 5 ms/div.

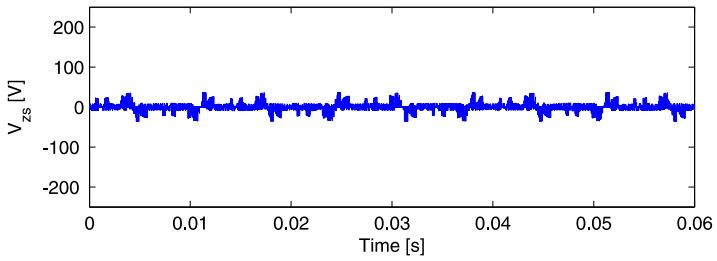


Fig. 21. Zero sequence voltage.

The converter output currents (machine phase currents) are shown in Fig. 22 resulting in similar waveforms compared to the simulation results (see Fig. 13).

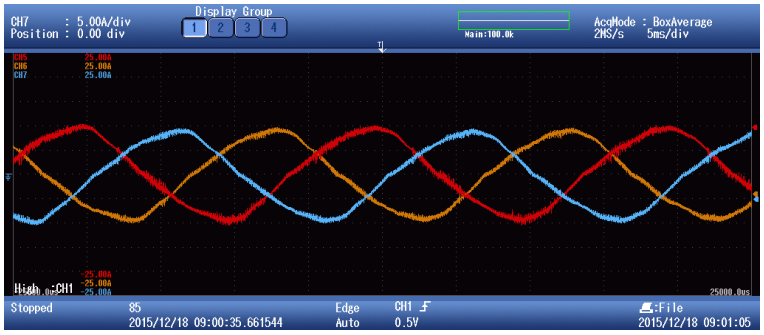


Fig. 22. Machine currents. Scales: 5 A/div, 5 ms/div.

The input phase voltage and current are shown in Fig. 23 where the unity displacement factor can be noted. In general, these preliminary experimental results are very similar to those obtained via simulations.

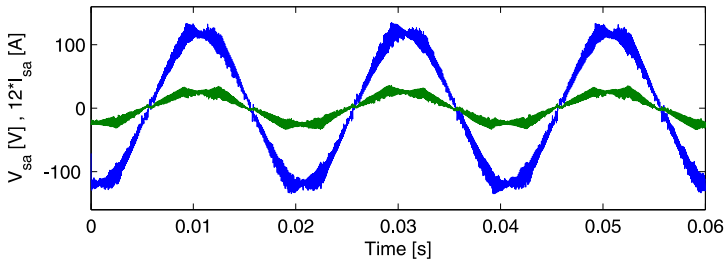


Fig. 23. Input rectifier voltage and current.

7. Conclusion

A topology based on indirect matrix converter to drive open-ended winding AC machines have been presented. Two modulation strategies have been used for the input rectifier, depending on the output voltage requirement. One modulation strategy aims for a maximum positive DC voltage and the other modulation strategy aims for a reduced positive DC voltage. Regardless of the modulation strategy used for the rectifier, unity displacement power factor operation is achieved at the converter input. On the other hand, the output stages are modulated via a space vector modulation strategy which eliminates the zero sequence voltage in the load by using only certain voltage vectors. Simulation and experimental results have been shown verifying the feasibility of the proposed drive.

8. Acknowledgements

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