Novel Current-Limiting Strategy for Solid-State Circuit Breakers (SSCB) Without Additional Impedance

Chunyang Gu[1], Francis Effah[2], Alberto Castellazzi[1], Alan J. Waston[1], Pat Wheeler[1]

[1]The University of Nottingham
Tower Building, University Park,
Nottingham, UK, NG7 2RD
E-Mail: chunyang.gu@nottingham.ac.uk

[2]The University of Mines and Technology
Dept. Electrical & Electronic Engineering,
P. O. Box 237, Tarkwa, Ghana
E-Mail: fbeffah@umat.edu.gh

Keywords

«Current limiter», «Protection device», «linear region of MOSFET», «Solid-state circuit breakers», «phase shifting control»

Abstract

Current-limiting strategies for solid-state circuit breaker (SSCB) without adding impedance is introduced in this paper. With the current limitation of novel phase-shifting method, the advantages are simple hardware structure, relatively low cost, no heat generation, low weight and small size. Current-limiting capability is exploited with qualities of good control accuracy and robustness. The principle and theoretical analysis of phase-shifting current-limiting method are detailed introduced together with simulation/experimental verifications.

Introduction

Traditional mechanical circuit breaker (MCB) is with a limited operating speed and reduced lifetime because of its electromagnetic contacts. In recent times, power semiconductors have been used to substitute MCBs. These kinds of configurations are called solid-state circuit breaker (SSCB) [1-4]. There is no arcing, no contact erosion, so that the lifetime of an SSCB is high than an MCB. Due to the absence of mechanical part, the reaction speed of SSCB is high. SSCB is suitable for both AC and DC. With digital control, SSCB is accurate and flexible for multi-functional control and monitoring. With the use of wide bandgap devices (SiC or GaN), SSCBs are suitable for where fast switching is the precedence and losses are acceptable.

The basic configuration of a solid-state circuit breaker (SSCB) is a bi-directional semiconductor switch paralleled with MOV arrester, as shown in Fig. 1. With proper control of semiconductor switches, current-limiting function may be achieved [5]. In that way, no additional elements is needed, this may reduce the circuit breaker system dimension and cost.

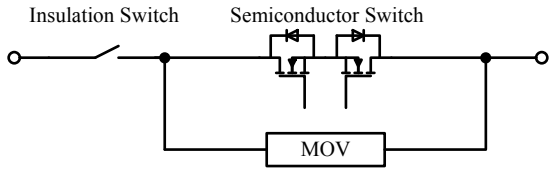


Fig. 1: Basic configuration of an SSCB without additional components.

For both AC/DC applications, PWM control (pulsed gate signal) and linear region control (variable gate signal) of the main semiconductor devices are appropriate. For AC applications, phase-shifting control is suitable for current limitation without additional impedance. The advantages of the proposed phase-shifting current-limiting control method are: a) Simple hardware structure; b) relatively low cost; c) high control accuracy; d) low weight and small size.

In this paper, current-limiting control strategies are applied to circuit breaker configurations with SiC/Si power devices in which no additional current-limiting passive components are needed e.g. inductors [6], PTC resistors [7] or superconductors [8]. The principle and further theoretical analysis is shown. Further simulation results are put forward to validate the control scheme. Current-limiting

circuit breaker prototype with 400V/500A breaking capability is designed and tested with experiments.

Theoretical Analysis and Control Strategies of CL-SSCB

SSCB consists of WBG switches with RCD snubber circuits and a metal oxide varistor (MOV). WBG switches to break the main current and MOV to absorb the reactor energy. For the three current-limiting methods, SSCB in Fig. 1 works in different conditions.

PWM Control Current-Limiting Method (Pulsed Gate Signal)

The current limitation for DC solid-state circuit breakers could be done by PWM control of the semiconductor devices. Therefore, main semiconductor devices are with pulsed gate driving signal. Fast WBG semiconductor devices such as SiC are highly recommended for maintaining limited currents.

Linear-Region Control Current-Limiting Method (Variable Gate Signal)

The current-limiting capability may be realized by using the linear region of the semiconductor devices. Therefore, the common-emitter semiconductor devices are working as a resistor to limit the current. With different gate voltage control of IGBTs or MOSFETs, the injected resistance to the system is different, so that the fault current could be limited.

Novel Phase-Shifting Current-Limiting Method

The basic principle of the phase-shifting current-limiting method is to make natural zero crossing of line current with the help of AC grid voltage, therefore limit the current without extra energy absorption, as shown in Fig. 2. With pure inductive load or with short-circuit fault, no active power is injected into the system. With resistive-inductive load or with overload fault, both active power and reactive power are injected into the system. The duty ratio and phase shift of the gate signal are determined by the condition of load (impedance and power factor) and the specific current-limiting requirement (RMS value or peak value). Zero current switching (ZCS) is necessarily achieved to eliminate extra power loss on the switches. And this behavior ensures that all of the semiconductor devices could be used including thyristors.

As the current harmonics are much higher than other type of current limiting circuit breakers, for the purposes of ER G5/4-1, semiconductor motor controllers (soft starters) and load controllers, which comply with IEC 60947-4-2 and IEC 60947-4-3, can be considered as AC regulators and the limits for these devices given in ER G5/4-1 will apply [9]. As the current waveform using the proposed phase-shifting control method is similar to a soft starter of motor and is less than three seconds in most cases, the installations of this type of current limiter can be accepted.

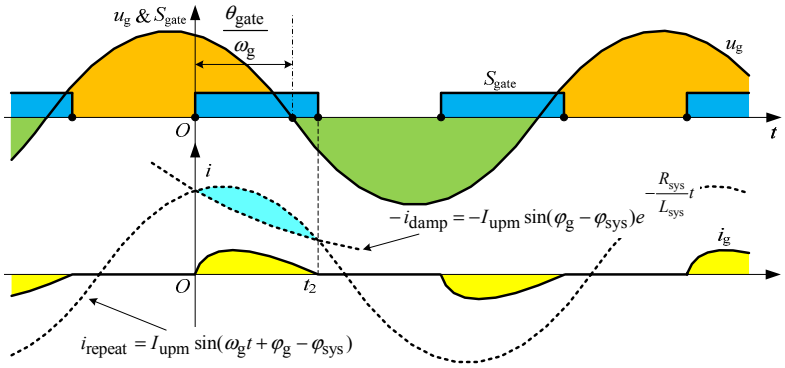
Mathematical Analysis of Phase-Shifting Characteristics

When grid voltage is $u_{\mathrm{g}} = U_{\mathrm{gm}}\sin(\omega_{\mathrm{g}}\mathrm{t} + \varphi_{\mathrm{g}})$, line impedance is $Z_{\mathrm{line}} = R_{\mathrm{line}} + \mathrm{j}\omega_{\mathrm{g}}L_{\mathrm{line}}$, the load impedance is $Z_{\mathrm{load}} = R_{\mathrm{load}} + \mathrm{j}\omega_{\mathrm{g}}L_{\mathrm{load}}$. The unlimited prospective current with the given system parameters might reach a high value: $i_{\mathrm{up}} = \frac{u_{\mathrm{g}}}{Z_{\mathrm{load}}+Z_{\mathrm{line}}} = \frac{U_{\mathrm{gm}}\sin(\omega_{\mathrm{g}}\mathrm{t}+\varphi_{\mathrm{g}})}{R_{\mathrm{sys}}+\mathrm{j}\omega_{\mathrm{g}}L_{\mathrm{sys}}} = I_{\mathrm{upm}}\sin(\omega_{\mathrm{g}}\mathrm{t} + \varphi_{\mathrm{up}})$, where $R_{\mathrm{sys}} = R_{\mathrm{load}} + R_{\mathrm{line}}$, $L_{\mathrm{sys}} = L_{\mathrm{load}} + L_{\mathrm{line}}$; $I_{\mathrm{upm}} = \frac{U_{\mathrm{gm}}}{\sqrt{{R_{\mathrm{sys}}}^2+\omega_{\mathrm{g}}{}^2{L_{\mathrm{sys}}}^2}}$ is the amplitude of the unlimited prospective sinusoidal current; and $\varphi_{\mathrm{up}} = \varphi_{\mathrm{g}} - \varphi_{\mathrm{sys}} = \varphi_{\mathrm{g}} - \arctan(\frac{\omega_{\mathrm{g}}L_{\mathrm{sys}}}{R_{\mathrm{sys}}})$ is the phase angle of that current. There are two control variables for phase-shifting control current limiting: duty ratio of gate signal (D_{gate}) is the ratio of on-state time to the period time of gate signal; and phase angle of gate signal (θ_{gate}) is the phase angle of the turn-on point of gate signal leading the zero crossing point of grid voltage. The phase angle of gate signal $\theta_{\mathrm{gate}} \geq 0$ is established for combined resistive-inductive loads.

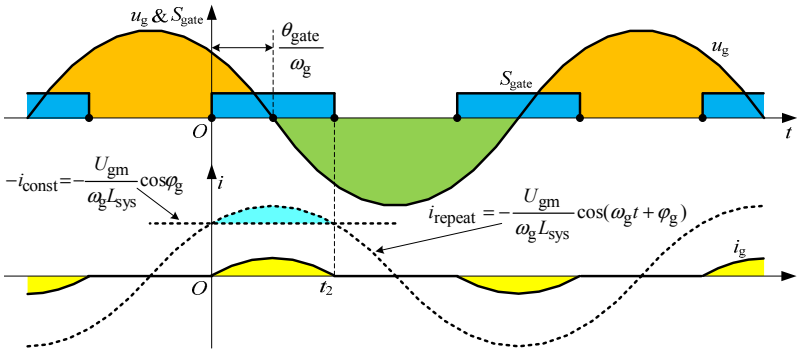
Suppose the gate signal turns on at t_1 and turns off at t_2 during one cycle time, and $t_1 = 0$ as a reference mark. When $t \in [t_1, t_2]$, and the system resistance is not zero (e.g. overload condition or larger line resistance), the limited current is

$$i_g(t) = I_{upm}\left[\sin(\omega_g t + \pi - \theta_{gate} - \varphi_{sys}) - \sin(\pi - \theta_{gate} - \varphi_{sys})\, e^{-\frac{t}{\tau_{sys}}}\right] \quad (1)$$

where $\tau_{sys} = \frac{L_{sys}}{R_{sys}} = \frac{\tan(\varphi_{sys})}{\omega_g}$ is the time constant of the system impedance. t_2 is solved by $i_g(t_2) = 0$. The line current is made up of two components: the damping component i_{damp} and the repeating component i_{repeat}, as shown in Fig. 2. It is apparent that φ_{sys}, τ_{sys} and I_{upm} are the system parameters related to ω_g, U_{gm}, R_{sys} and L_{sys}. And θ_{gate} is the main control variable. Fig. 3 shows the controlled line current waveforms (p.u. value) with different system impedances with constant $\omega_g = 100\pi$ rad/s. The D_{gate} type solution of (16) is actually the cross-zero point of the waveforms in Fig. 3. For peak line current, the control domain is $\theta_{gate} \in [0, \pi - \varphi_{sys}]$, and the range of value is $I_{g,peak} \in [0, I_{upm}]$. If the control phase angle θ_{gate} goes up from 0 to $\pi - \varphi_{sys}$, the peak current $I_{g,peak}$ goes up from 0 to I_{upm}, and D_{gate} goes up from 0 to 1 at the same time.



(a) $R_{sys} \neq 0$

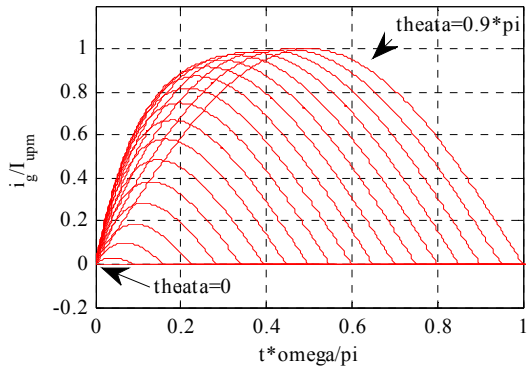


(b) $R_{sys} = 0$

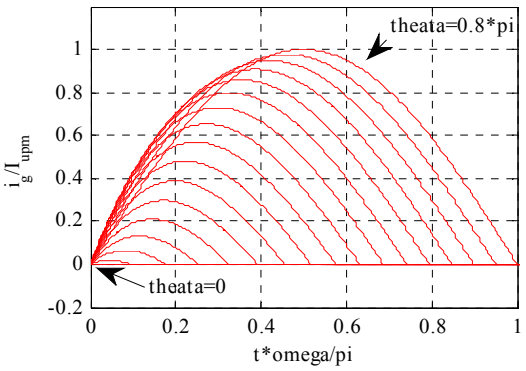
Fig. 2: The principle of the phase-shifting current-limiting method.

When ω_g is considered as a constant, the duty ratio D_{gate}, p.u. peak current $I_{g,peak}$ and p.u. RMS current $I_{g,RMS}$ are actually the functions of phase angle of the system impedance φ_{sys} and gate phase angle $\theta_{gate} \in [0, \pi - \varphi_{sys}]$, that is: $D_{gate} = \frac{\omega_g t_2}{\pi} = f_{D_{gate}}(\theta_{gate}, \varphi_{sys})$, $I_{g,peak,pu} = \frac{I_{g,peak}}{I_{upm}} = f_{I_{peak,pu}}(\theta_{gate}, \varphi_{sys})$ and $I_{g,RMS,pu} = \frac{I_{g,RMS}}{I_{upm}} = f_{I_{RMS,pu}}(\theta_{gate}, \varphi_{sys})$. Fig. 4 shows the surfaces of D_{gate}, $I_{g,peak,pu}$ and $I_{g,RMS,pu}$ related to θ_{gate} and φ_{sys}, respectively.

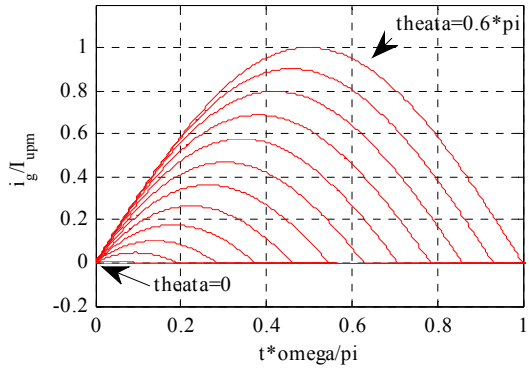
It is reasonable that if the R-L parameters φ_{sys} are given or observed, we can get θ_{gate} with the reference requirements of $I_{\text{g,peak,pu}}$ or $I_{\text{g,RMS,pu}}$; then with certain φ_{sys} and θ_{gate}, D_{gate} is found out. However if the system parameters are not accurately given, or the parameters are changing and difficult to be observed, it is practical to use a close-loop method to control the line current and to achieve ZCS off as well.



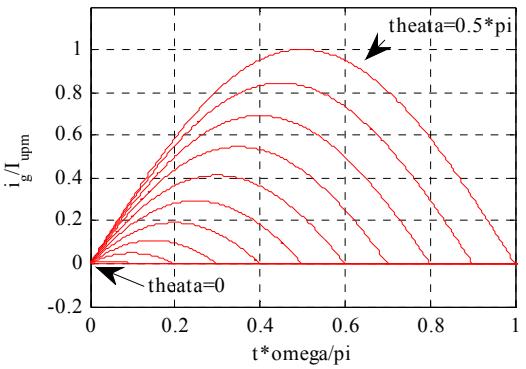
(a) $\varphi_{\text{sys}} = 0.1\pi$, $\theta_{\text{gate}} \in [0{:}\ 0.05\pi{:}\ 0.9\pi]$.



(2) $\varphi_{\text{sys}} = 0.2\pi$, $\theta_{\text{gate}} \in [0{:}\ 0.05\pi{:}\ 0.8\pi]$.

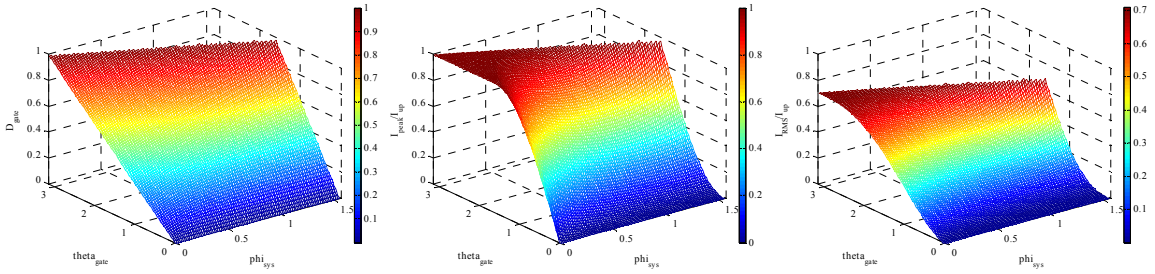


(c) $\varphi_{\text{sys}} = 0.4\pi$, $\theta_{\text{gate}} \in [0{:}\ 0.05\pi{:}\ 0.6\pi]$.



(d) $\varphi_{\text{sys}} = 0.5\pi$, $\theta_{\text{gate}} \in [0{:}\ 0.05\pi{:}\ 0.5\pi]$.

Fig. 3: Time-current waveforms of a half cycle with different system impedance ($\omega_{\text{g}} = 100\pi$ rad/s).



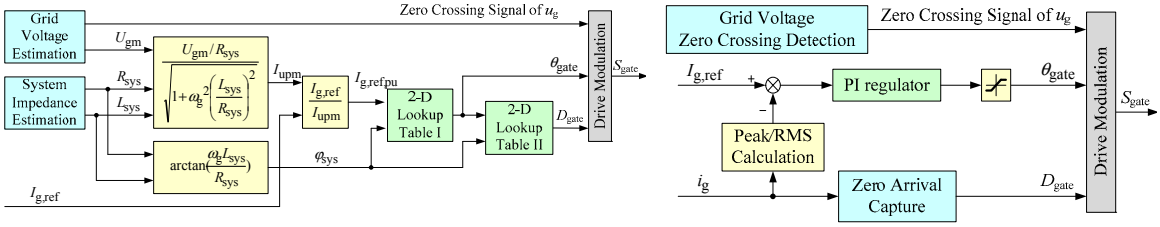
(a) Surface D_{gate}, θ_{gate} and φ_{sys}. (b) Surface $I_{\text{g,peak,pu}}$, θ_{gate} and φ_{sys}. (c) Surface $I_{\text{g,RMS,pu}}$, θ_{gate} and φ_{sys}.

Fig. 4: Control characteristics of D_{gate}, θ_{gate}, φ_{sys}, $I_{\text{g,peak,pu}}$ or $I_{\text{g,RMS,pu}}$ ($\omega_{\text{g}} = 100\pi$ rad/s).

Detailed Practical Control Description

The general control diagrams are proposed as in Fig. 5. In Fig. 5(a), $I_{\text{g,ref}}$ is the current-limiting command (reference current) value, which could be either $I_{\text{g,peak}}$ or $I_{\text{g,RMS}}$, depending on requirements. The 2-D lookup table I is related to Fig. 4(b) and Fig. 4(c), which is calculation offline and pre-written in the controller's memory. The 2-D lookup table II is related to Fig. 4(a), which is also pre-written in the controller's memory. If the zero crossing point of grid voltage is captured, the system could be controlled with simplified close-loop control method, as shown in Fig. 5(b). Compared with Fig. 5(a), neither complex calculation module nor huge 2-D lookup table is needed.

However, the dynamic response is not as good as with Fig. 5(a). The grid voltage zero crossing detection could be done by using voltage sensor, the estimation method or using other detection tools such as a diode.



(a) Open-loop method. (b) Close-loop method.

Fig. 5: General open-close control diagram of current limitation.

Semiconductor Device Selection of of CL-SSCB

When For a 400V/500A AC electrical system, the device selection was based on the following criteria:

(a) Voltage rating: at least 1.5 times the peak phase voltage. Typical ratings at single device level of 1.2kV;

(b) On-state losses: the lower the better, for optimised system efficiency and to contain the design of the thermal management. As a hybrid circuit breaker is designed, On-state loss is not a big issue of on-state loss.

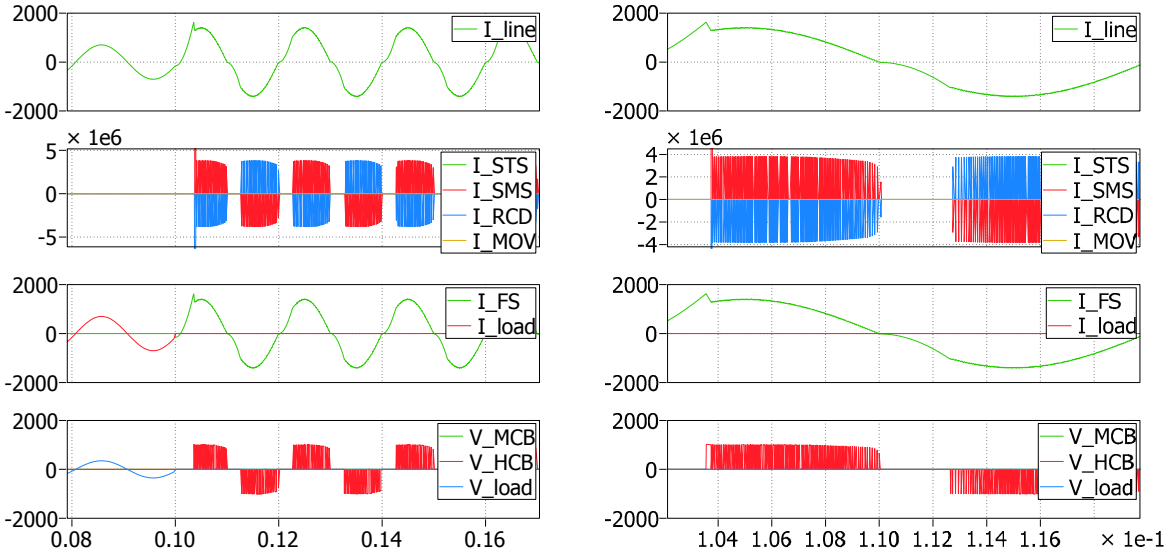
Several 1200V semiconductor devices which can be realistically taken into consideration for this kind of application are Silicon Insulated Gate Bipolar Transistor (Si IGBT), Silicon Metal Oxide Semiconductor Field Effect Transistor (Si MOSFET), Silicon Carbide Metal Oxide Semiconductor Field Effect Transistor (SiC MOSFET), Silicon Carbide Junction Field Effect Transistor (SiC JFET) and Silicon Carbide Bipolar Junction Transistor (SiC BJT).

It is obvious that wide-bandgap SiC devices are excellent with higher frequency, lower losses and higher reliability to replace Si IGBT and Si MOSFET. SiC MOSFET C2M0025120D may be a good choice as it contains anti-parallel diode and with better performance than the others. However, for practical applications in hybrid circuit breaker products, Si IGBT devices might be alternative choices because their lower price and acceptable performances.

Table I: Semiconductor devices types in detail.

Devices / Parameters	Si IGBT	Si MOSFET	SiC BJT	SiC JFET	SiC MOSFET
	FGH40T120SMD	IXFB30N120P	GA50JT12-247	UJN1205K	C2M0025120D
I_D with specific T_{Case}	40A @ 100°C	23A @ 100°C	80A @ 100°C	23A @ 125°C	60A @ 100°C
$R_{th,j-c}$	0.27K/W	0.1K/W	0.26K/W	0.65K/W	0.27K/W
Max Junction temperature	175°C	150°C	175°C	175°C	150°C
Max P_D @ T_{Case}=25°C	555W	1250W	583W	230W	463W
P_D @ T_{Case}=100°C	277W	500W	288W	115W	185W
On-state characteristics	$V_{CE(sat)}$=1.8V	$R_{DS(on)}$=350mΩ	$R_{DS(on)}$=20mΩ	$R_{DS(on)}$=45mΩ	$R_{DS(on)}$=25mΩ
Anti-parallel diode	Integrated 0.89K/W 3.8V	Intrinsic 0.1K/W 1.5V	Additional GA50JT12-247 0.242K/W 1.5V	Additional UJ2D1230K 0.4K/W 1.5V	Intrinsic 0.24K/W 3.3V

Simulation and Experimental Verifications



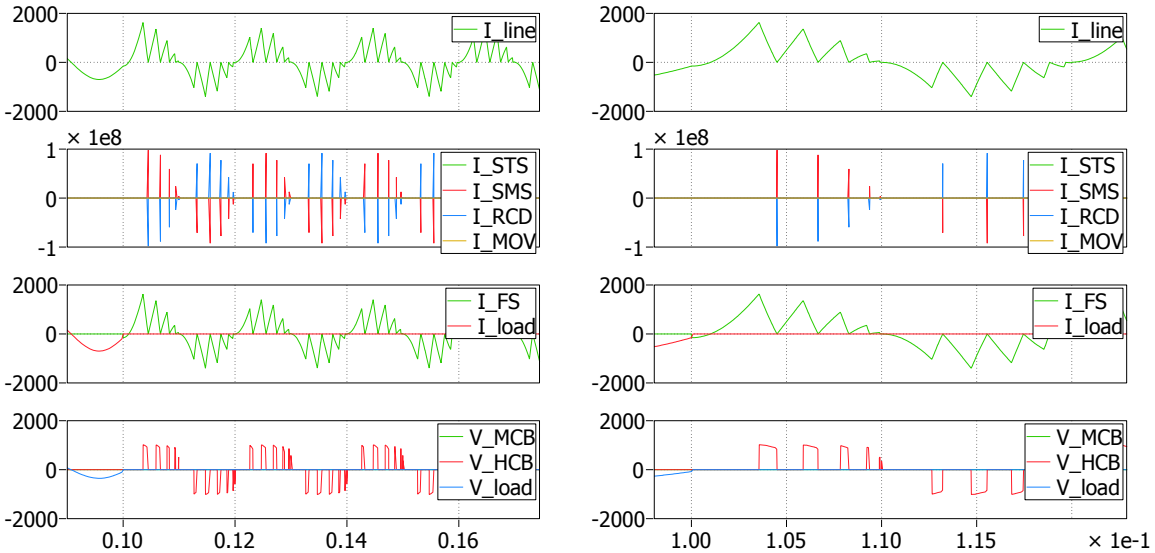
(a) Whole breaking process (current: A, voltage: V). (b) Details of breaking process (current: A, voltage: V).

Fig. 6: Simulation results of PWM method with continuous current.

Simulation Results of PWM Control

Fig. 6 shows the simulation results of PWM method with continuous current, the breaking current is set to be 1400A. The power loss on MOV resistor, which is an very big value. The reason why large power dissipation is added to MOV when limiting the current, is that no matter what the control method is, the switched MOV is equivalent to a variable resistor. When the rated source voltage is associated with 2~3 times of rated current and nearly unity power factor, the 2~3 times of rated active power must be absorbed by MOV component.

Fig. 7 shows the functional simulation results of PWM method with discontinuous current. The power loss of MOV will be smaller than that of PWM method with continuous current.

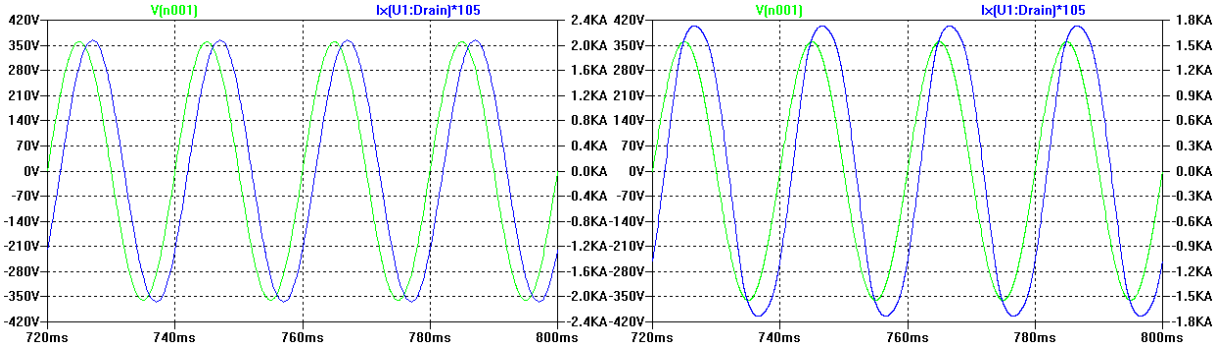


(a) Whole breaking process (current: A, voltage: V). (b) Details of breaking process (current: A, voltage: V).

Fig. 7: Simulation results of PWM method with discontinuous current.

Simulation Results of Linear Region Control

Fig. 8 and Fig. 9 show the SPICE simulation results of linear region control current limiting. A detailed Cree SiC MOSFET SPICE model is used in this simulation for the variable gate voltage control for different resistance injection. This simulation uses the minimum number of devices and the case is connected to 25°C constant temperature for power dissipation (ideal heat dissipation which is not realizable). The paralleled semiconductor devices are assumed to be equal in current.



(a) Unlimited current waveform ($I_{g,peak} = 3 \times I_n$). (b) Limited current waveform ($I_{g,peak} = 2.5 \times I_n$).

Fig. 8: Simulation results of linear region control of current limitation (voltage and current).

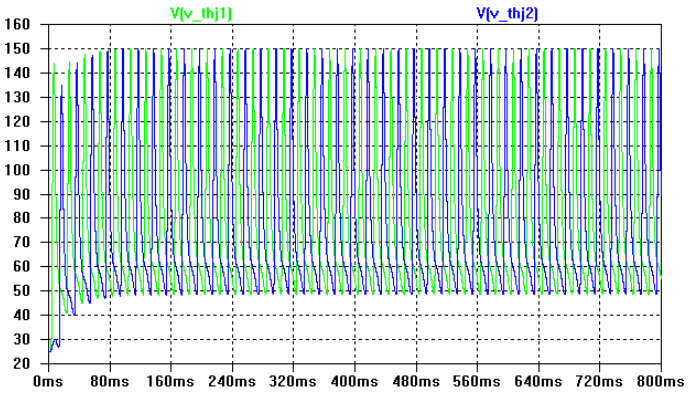
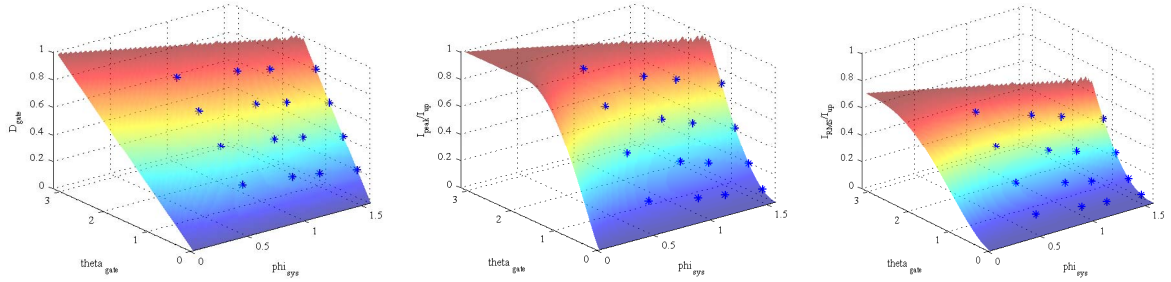


Fig. 9: Simulation results of linear region control of current limitation (junction temperature in °C).

Simulation Results of Phase-Shifting Control

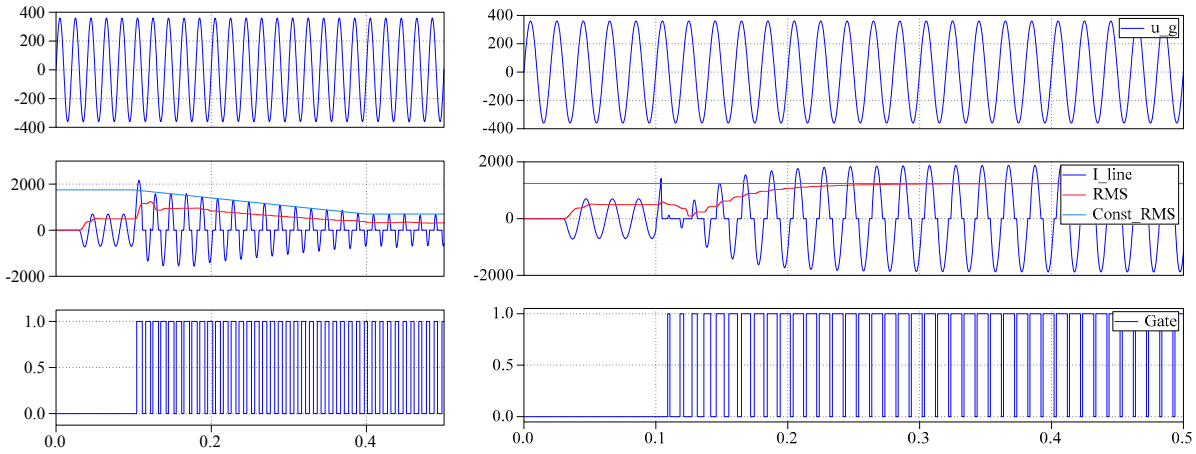
The corresponding surface of D_{gate}-θ_{gate} with 16 check point compared with theoretical solutions in Fig. 4 is shown in Fig. 10. The simulation results and theoretical solutions meet closely. The correctness of analysis is verified. The correctness of characteristics analysis is verified which lays the foundation of further open-loop control method and close-loop control method.

The system parameter estimation results are good enough for open-loop control even with short circuit conditions. As shown in Fig. 11(a). The correctness of open-loop control as well as the estimation methods is verified. The close-loop simulation results are shown from Fig. 11(b). Both the briefness and data amount of close-loop method is better than open-loop method, but the response speed is slower with potential control oscillation.



(a) Surface D_{gate}, θ_{gate} and φ_{sys}. (b) Surface $I_{g,peak,pu}$, θ_{gate} and φ_{sys}. (c) Surface $I_{g,RMS,pu}$, θ_{gate} and φ_{sys}.

Fig. 10: Characteristics surfaces with 16 simulations check points.



(a) Open-loop, ramp command. (b) Close-loop, constant command. ($I_{\mathrm{g,peak}} = (2.5\sim1) \times I_{\mathrm{n}}$)

Fig. 11: Type Z ($I_{\mathrm{upm}} = 3I_{\mathrm{n}}$) simulation waveforms: voltage (V), instant/reference/RMS currents (A) and gate signals.

Experimental Verifications

Fig. 12 shows the schematic diagram and photograph of designed SSCB with SiC power MOSFETs and SiC IGBTs. Table II gives the details of the two SSCB prototypes. With certain MOV, the total clear time of SSCB at 150A is less than 1ms, with peak current of about 160A. Although the turn-off speed of SiC MOSFET is faster than that of Si IGBT, the trip time of SiC MOSFET is a little larger than that of Si IGBT because its switch-off time is delayed by snubber circuit.

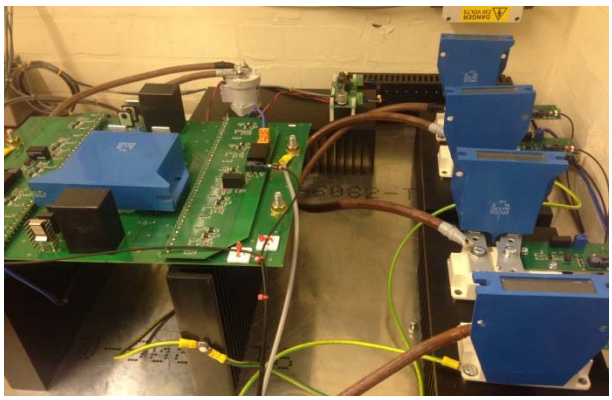
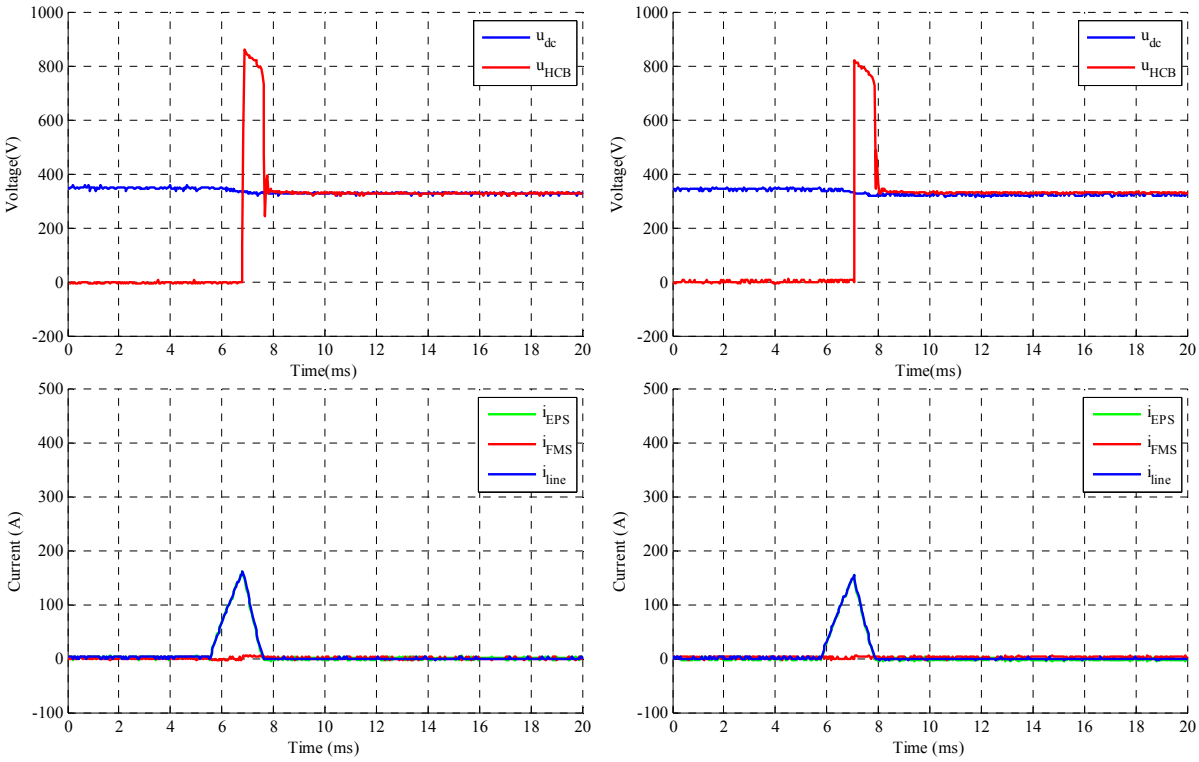


Fig. 12: Photograph of designed SSCB with SiC power MOSFETs or Si IGBTs.

Table II: Details of two SSCB prototypes.

Parameters	Details of prototype 1	Details of prototype 2
Device type	SiC MOSFET	Si IGBT
Part number	C2M0025120D 15 in parallel	FZ600R17KE3
Rated current	900A	600A
MOV arrestor	B80K385	B60K385
Resistor of snubber	50Ω	N/A
Diode of snubber	DH60-18A	N/A
Capacitor of snubber	15μF/1100V	N/A

Fig. 13 gives the primary experimental results of SSCB testing.



(a) With SiC MSOFETs. (b) With Si IGBTs.

Fig. 13: Preliminary experimental results of SSCB (360A, breaking at 150A).

Fig. 14 show the comparison of SSCB operation performance using SiC MOSFET and Si IGBT, i.e. the comparison of total clear time (from a fault occurs to main current reduces to zero) and EPS trip time (from EPS contacts to EPS branch current reduces to zero). Although the turn-off speed of SiC MOSFET (57ns typical) is faster than that of Si IGBT (200ns typical), the trip time of SiC MOSFET is a little larger than that of Si IGBT because its switch-off time is delayed by RCD snubber circuit with time constant of 0.75ms.

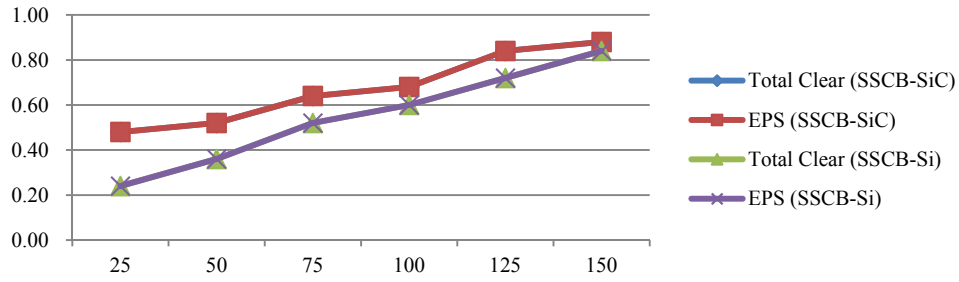


Fig. 14: Comparison of total clear time and EPS trip time (ms) with SiC MOSFET and Si IGBT.

Conclusions and Future Works

In this paper, current-limiting control strategies of PWM control, linear region control as well as phase-shifting control are applied to basic solid-state circuit breaker configurations with Si or SiC power devices without additional impedance. The principle and further theoretical analysis is proposed with analysis.

When limiting the current with PWM of semiconductor devices, the semiconductor with MOV works as a resistor to absorb the energy. All of the resistive power is absorbed by MOV arrestor, which makes the MOV to be bigger than other methods. When limiting the current with linear region of semiconductor devices, current-limiting may be good only for short period of time depending on SOA of semiconductor devices and cooling conditions.

When limiting the current with phase-shifting method, the advantages are simple hardware structure, relatively low cost, control with parameter robustness, high control accuracy, no heat generation, low weight and small size. The disadvantage would be only AC operation, relatively complex control and high current harmonics.

PLECS and SPICE simulation results are given to validate the control strategies. Current-limiting circuit breaker prototype with 400V/500A breaking capability is designed and tested with experiments. Future work of current-limiting methods will be the detailed assessments of phase-shifting method with further experiment verifications.

References

[1] S. Schroder, C. Meyer, and R. W. De Doncker, "Solid-state circuit breakers and current-limiting devices for medium-voltage systems," in Power Electronics Congress, 2002. Technical Proceedings. CIEP 2002. VIII IEEE International, 2002, pp. 91-95.

[2] M. M. R. Ahmed, G. Putrus, R. Li, and R. Penlington, "Development of a prototype solid-state fault-current limiting and interrupting device for low-voltage distribution networks," Power Delivery, IEEE Transactions on, vol. 21, pp. 1997-2005, 2006.

[3] R. Nasereddine, I. Amor, A. Massoud, and L. Ben Brahim, "AC solid state circuit breakers for fault current limitation in distributed generation," in GCC Conference and Exhibition (GCC), 2013 7th IEEE, 2013, pp. 446-449.

[4] H. Radmanesh, S. H. Fathi, G. B. Gharehpetian, and A. Heidary, "A Novel Solid-State Fault Current-Limiting Circuit Breaker for Medium-Voltage Network Applications," Power Delivery, IEEE Transactions on, vol. PP, pp. 1-1, 2015.

[5] C. W. Brice, R. A. Dougal, and J. L. Hudgins, "Review of technologies for current-limiting low-voltage circuit breakers," Industry Applications, IEEE Transactions on, vol. 32, pp. 1005-1010, 1996.

[6] D. F. Peelo, G. S. Polovick, J. H. Sawada, P. Diamanti, R. Presta, A. Sarshar, et al., "Mitigation of circuit breaker transient recovery voltages associated with current limiting reactors," Power Delivery, IEEE Transactions on, vol. 11, pp. 865-871, 1996.

[7] M. Steurer, K. Frohlich, W. Holaus, and K. Kaltenegger, "A novel hybrid current-limiting circuit breaker for medium voltage: principle and test results," Power Delivery, IEEE Transactions on, vol. 18, pp. 460-467, 2003.

[8] W. Paul, J. Rhyner, and F. Platter, "Superconducting fault current limiters based on high Tc superconductors," in Fault Current Limiters - A Look at Tomorrow, IEE Colloquium on, 1995, pp. 4/1-4/4.

[9] M. Harmonics, "A Guide to ENA Engineering Recommendation G5/4-1," online http://documents.mx/documents/managing- harmonics- a- guide- to- ena- engineering- recommendation-g54-1.html.