THE STAR-SWITCHED MMC (SSMMC) - A HYBRID VSC FOR HVDC APPLICATIONS

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Abstract

This paper presents a new hybrid VSC topology (the Star-Switched MMC) – suitable for HVDC applications. The basic structure and operating principles of the topology are described. Control strategies that regulate the power exchanged between the VSC, the AC network and the DC network are presented. A modulation strategy ensuring appropriate switching of the individual chain-link sub-modules and a capacitor voltage balancing algorithm that ensures the capacitor voltages are maintained within the required tolerance are discussed. Results from a simulation model are presented to validate the expected performance of the converter and the proposed control schemes.

1 Introduction

The generation of power from renewable energy sources is growing rapidly. However, the new mega-generation sites are often hundreds of kilometers away from consumers and vast amounts of power have to be transported over long distances. Traditionally, due to the relative simplicity of AC transformers and lower losses, High Voltage AC (HVAC) systems have been deployed[1]. As high voltage electronic converters became more efficient and economical, High Voltage DC (HVDC) transmission became an attractive option for long distance high power transmission because of the following advantages over the counterpart HVAC system[2-4]

- Overhead line clearances are smaller for DC systems contributing to a reduced cost of transmission installation.
- DC power can be controlled far more quickly than AC power to respond to power transients or faults. This provides improved network stability against disturbances.
- DC power can be transmitted economically to far greater distance than AC power. Theoretically, there is no distance limit for HVDC transmission.
- DC power can be used to interconnect two systems of different frequency or phase as the power flow through an HVDC link can be controlled independently of the phase angle between the source and load.

HVDC systems do however have some disadvantages especially when considered for short distance power transmission. They are less reliable and have less availability than AC systems mainly because of the extra converter stations [2]. The cost of losses in the converter station and the system cost may be more than that of an AC system for short distance transmission.

Considerable research and industrial development on HVDC converter technology has been carried out over many years to improve the power transfer capability and to reduce the power loss and the cost of transmission. Various HVDC converter topologies and control techniques were introduced in this effort [1, 5, 6] . Although current source converters (line commutated thyristor converters) are well known and are more efficient than alternatives, they have fundamental drawbacks that hamper the advancement of CSC based HVDC in some applications [2-4]. They have higher converter foot-print and limited active and reactive power control capability. They also lack black start capability and cannot support an AC network containing only passive loads. Since the DC current cannot be reversed, power reversal is not possible without reversing the polarity of the DC voltage. This limits CSC HVDC projects to use certain types of (more expensive) cables and gives these converters very limited scope for multi-terminal DC (MTDC) operations, a key aspect for future HVDC applications.

VSCs overcome some of the key drawbacks of CSC and are therefore becoming increasingly popular for HVDC applications. However, compared to CSCs they have lower overall converter efficiency and currently the feasible maximum power rating is lower. Various VSC topologies have been considered for HVDC applications in the effort to improve converter efficiency and explore the advantages of VSC systems in HVDC networks.

VSC topologies that have been considered include the Two-Level VSC [2, 3], Three-Level Neutral-Point-Clamped (NPC) VSC [7], the capacitor clamped VSC (Flying Capacitor (FC) [8]) and the Cascaded H-Bridge VSC[9]. The conventional multilevel VSCs: - NPC and FC are known to have limitations for implementation with a large numbers of levels (3 in the case of the NPC) [10]. The cascaded H-Bridge can be implemented with several voltage levels but requires isolated DC sources for each bridge unless it is operated as a STACOM with no real power flow. This is a fundamental drawback that makes it less attractive for HVDC applications.

Recently, the Modular Multi-Level Converter (MMC) [1, 3, 11, 12] has been proposed and is being extensively investigated for HVDC applications. It offers some interesting

characteristics including, high modularity, scalability, high converter efficiency, low device stress, low loss, and reduced harmonic content in the synthesised waveform.

Modular multi-Level converters however have some drawbacks. They require complex control strategies to ensure that the floating capacitor voltages are maintained within a tight tolerance band for sustainable operation of the converter [13]. The sub-module capacitors are also large and bulky. When half-bridge sub-modules are used, the converter is not able to block DC fault [14] which is a desirable feature for VSC-HVDC converters as DC circuit breakers for high power applications are still under development and are extremely costly [15, 16]. An MMC with full-bridge submodules can operate in the presence of a DC fault, but the conduction loss is considerably higher as the number of semiconductor devices in conduction is doubled.

Recently, hybrid voltage source converters such as the parallel hybrid VSC [5, 17] and the Alternate Arm Converter (AAC) [6, 18], combining features of two-level and modular multi-Level converters have been proposed to achieve high waveform fidelity, lower loss and/or DC fault blocking capability.

Despite the fact that many VSC topologies, each with their own advantages have been introduced so far, there is still considerable scope for further innovation to devise converter topologies with the optimum desired performance for many applications.

This paper investigates a hybrid voltage source converter topology, the star-switched modular multilevel converter (SSMMC) [19] being considered for HVDC applications. It describes the basic topology structure, operating principles and converter control strategies required to regulate the power exchange between the AC network, the converter and the DC network. The PLECS simulation package is used to model the converter, to study and verify its working principles and to validate the proposed control schemes.

2 Converter Topology

The topology as shown in Figure 1 consists of two arms in each phase. One arm is a switching block (S) and the other arm is a cascaded connection of half-bridge sub-modules termed the Chain-link (CL). The position of the two arms in a phase could be interchanged – with no difference to the basic operation. The CL arms are connected in a star configuration at one pole of the DC network while the S arms are connected in a star configuration at the other pole of the DC network. In this paper, the circuit is analysed considering the upper arm in each phase as the S block and the lower arm as the CL block. The configuration of the switches required in the S block depends on the intended application of the converter. For bidirectional operation, active switches are required. However, for ease of illustration the performance of the converter is investigated considering mainly operation as a rectifier with diodes in the S block. Though, the converter efficiency is discussed as a bidirectional converter to facilitate comparison with other HVDC VSCs. In the loss analysis, active switches are considered for use in the S blocks.

The cascade of half-bridge chain-link sub-modules in the lower arm are the same basic building blocks used in the MMC. Each individual sub-module is identical comprising two IGBTs with anti-parallel diodes and a storage capacitor as shown in Figure 2.

The output voltage of a sub-module is controlled by operating the two switches (S_a and S_b) in a complementary fashion (assuming ideal switching). When the upper switch (S_a) is ON and the bottom switch (S_b) is OFF, the sub-module capacitor is inserted into the external circuit and the sub-module output voltage (V_{cell}) is equal to the capacitor voltage (V_c). When the bottom switch (S_b) is ON and the upper switch (S_a) is OFF, the sub-module is bypassed and its output voltage will be zero.

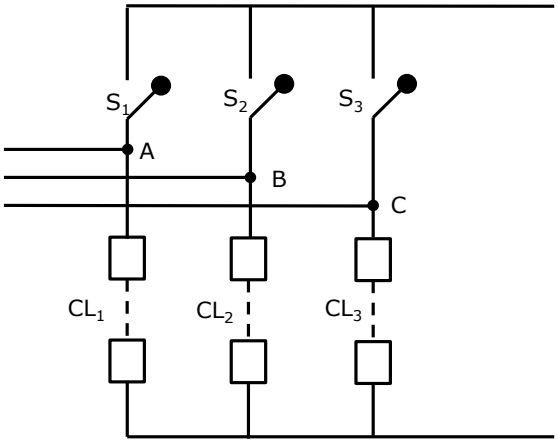


Figure 1: Basic Structure of the SSMMC Hybrid Converter

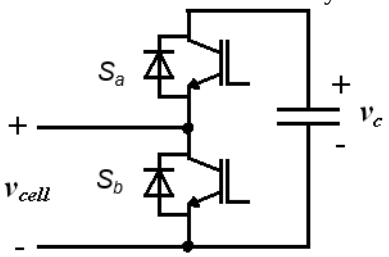


Figure 2: Structure of a Chain-Link submodule

It is therefore possible to control the output voltage of the converter by controlling the outputs of the individual sub-modules either to be 0 or V_c. With a suitable (large) number of chain-link sub-modules connected in series, the converter can produce a stepped voltage very close to a pure sinusoid

3 Operating Principle of the Converter

For convenience of analysing the general operation of this converter, the chain-links can be represented as controlled voltage sources and the converter can be considered to be connected to a bipolar DC network as shown in Figure 3.

The upper arm diode switches are naturally-commutated devices and hence their switching state is controlled by the polarity of the voltages applied to their terminals. For this converter topology, the voltage across each diode is equal to

the difference between two adjacent phase to phase output voltages at the converter terminals.

Considering the case where three balanced sinusoidal voltages (1) are created at the AC terminals of the converter, it can be observed from the phase voltages in Figure 4 that each of the phase voltages is greater than the other two for 1/3 of the complete cycle (120 degrees).

$$V_x = \hat{V}\sin\left(\omega t - k\frac{2\pi}{3}\right) \quad k \in \{0,1,2\}, x \in \{a,b,c\} \qquad (1)$$

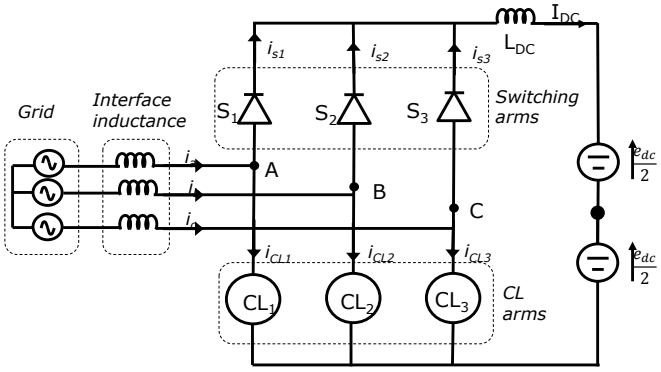


Figure 3: Simplified representation of the hybrid converter

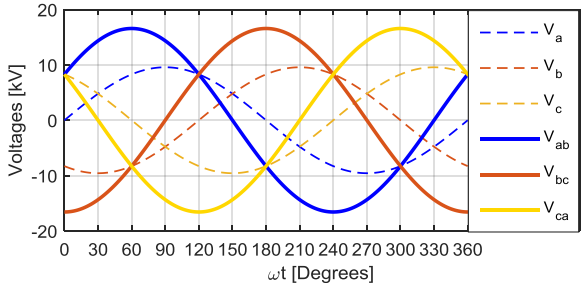


Figure 4: Ideal converter AC voltages for an 11kV system (Dashed lines are phase voltages, and continuous lines are line voltages)

For the SSMMC topology, the diodes in the upper arms conduct when their respective phase voltage is greater than the other two. Hence, from Figure 4, the conduction states of the switches can be deduced to be as presented in Figure 5. Clearly, for the converter to operate successfully, the diodes in the upper arm should alternately conduct exactly for one-third of the fundamental cycle for the balanced conditions defined in (1). The three intervals where S_1, S_2 and S_3 conduct are termed Mode1, Mode2 and Mode 3 respectively.

The relationships between the chain-link voltages, the AC terminal voltages and the DC side voltages for the three conduction intervals are summarised in Table 1. In each mode, the voltage produced by the chain-link associated with the conducting switch is defined as V_{m1}, V_{m2} and V_{m3} respectively for the 3 modes. The DC output voltage of the converter for one full cycle is the average of the output DC voltage over the three modes. Ignoring the effect of resistance in the DC side inductor, the converter synthesises a DC voltage to support the DC bus voltage in each interval. Hence in the balanced steady state condition V_{m1}, V_{m2} and V_{m3} are all equal to the DC bus voltage.

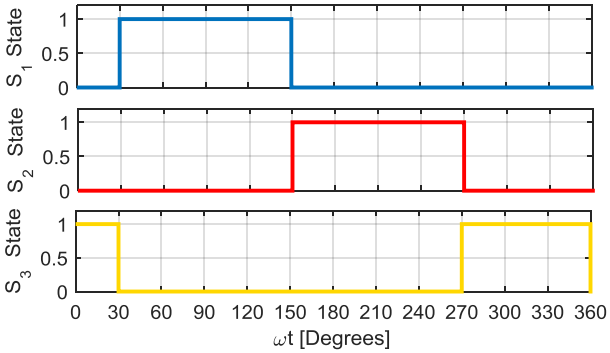


Figure 5: Switching arm conduction intervals

In Table 1, the voltages to be synthesised by the converter chain-links are summarised and are illustrated in Figure 6. It is obvious from Figure 5 and Figure 6 that when the switching arm of the converter phase leg is conducting, the corresponding CL arm has to synthesise enough voltage to support the DC bus voltage. However, in the phases where the switching arm is OFF, the CL arms synthesise a voltage which is the difference between the DC voltage and one of the desired line-line voltages, such that the correct voltages appear at the AC terminals.

Interval (degrees)	**VCL1**	**VCL2**	**VCL3**
30 – 150	Vm1	Vm1 – Vab	Vm1 – Vac
150 – 270	Vm2 – Vba	Vm2	Vm2 – Vbc
270 – 30	Vm3 - Vca	Vm3 - Vcb	Vm3

Table 1: Chain-link voltages for the different conduction intervals

The current in a chain-link, when its associated upper arm diode is conducting, will be the difference between the AC line current and the DC-link current. For non-conducting diode phases the chain-link current is simply equal to the AC line current.

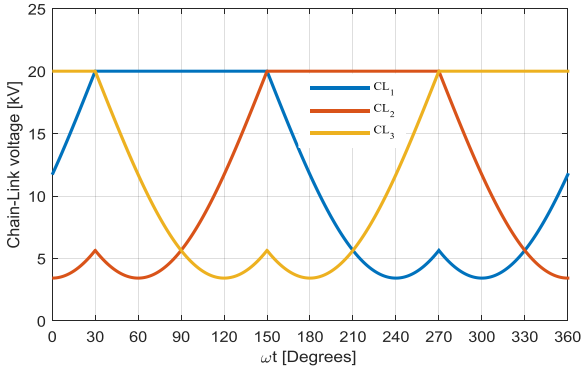


Figure 6: Voltage synthesised by the converter Chain-Links in a typical 20kV (DC)/11kV system

Clearly the current flowing in each upper arm diode is equal to the DC-link current when it is conducting and zero otherwise; see Table 2 and Table 3.

Interval (degrees)	$\mathbf{I_{CL1}}$	$\mathbf{I_{CL2}}$	$\mathbf{I_{CL3}}$
30 – 150	I_a - I_{dc}	I_b	I_c
150 – 270	I_a	I_b – I_{dc}	I_c
270 – 30	I_a	I_b	I_c - I_{dc}

Table 2: Chain-link currents for the different conduction intervals of the upper switch diodes

Interval (degrees)	$\mathbf{I_{S1}}$	$\mathbf{I_{S2}}$	$\mathbf{I_{S3}}$
30 – 150	I_{dc}	0	0
150 – 270	0	I_{dc}	0
270 – 30	0	0	I_{dc}

Table 3: Current through the S arm diodes for different conduction intervals

5 Converter Control Strategy

For successful operation of the converter, the powers exchanged with the AC grid and with the DC network have to be regulated so that power balance between the AC and DC network is always maintained in steady state. In addition, a control scheme is required to regulate the individual chain-link capacitor voltages.

Assuming the DC link voltage is kept at a reference value, the converter DC side output current determines the power transferred to the DC network. On the AC side, power exchange depends on the amplitude and phase of the converter voltages with respect to the grid voltages.

A PI regulator implemented in a standard synchronous reference frame is used for the control of power exchange between the converter and the AC network because since it has very good steady state response, low current ripple and constant switching frequency compared to hysteresis and predictive control techniques. The synchronous reference frame scheme enables decoupled control of active and reactive power exchange between the converter and the AC network where necessary.

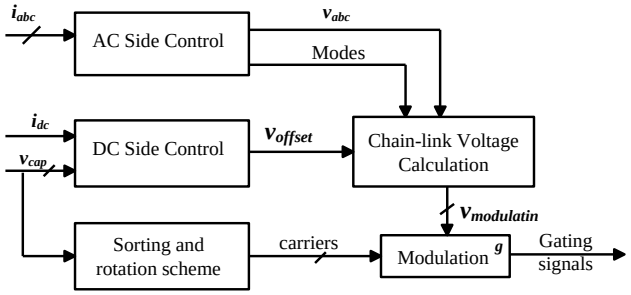


Figure 7: General converter control structure

The general structure of the control scheme for the converter is shown in Figure 7. The DC side control regulates the power exchange between the converter and the DC network by controlling the DC current in order to maintain the converter total stored energy at the desired value. The AC side control on the other hand regulates the power exchange between the AC network and the converter. It independently controls the active and reactive power according to demand values. A sorting and rotation scheme ensures that the local chain-link capacitor voltages are balanced over a set period of time.

4.1 DC Side Control

The DC side converter control strategy shown in Figure 8 contains two control parts; - converter total energy control and DC-link current control. The converter total energy control ensures the power coming from AC side is fully transferred to the DC side without any net power being sourced or absorbed by the chain-links (in steady state). It aims to keep the total converter energy to the rated value by setting a reference DC-link current for the DC-link current controller.

The controller is designed based on the relationship between the power imported or exported to the converter given by (2) and (3). In steady state, the power imported to the converter has to be equal to the power exported from the converter.

$$P_{AC} = P_{DC} \tag{2}$$

$$\frac{dw_c(t)}{dt} = V_{DC} I_{DC}(t) \tag{3}$$

where W_c is the total stored energy in the converter

Assuming the DC grid has constant voltage magnitude, the plant transfer function in s-domain will be (4).

$$\frac{w_c(s)}{I_{DC}(s)} = \frac{V_{DC}}{s} \tag{4}$$

The DC-link current controller on the other hand regulates the DC-link current at the value demanded by the energy controller, by adjusting the DC voltage component synthesised by each chain-link (V_{m1}, V_{m2} and V_{m3}). The controller is designed based on the relationship between the voltage and current for a system with the impedance dominated by RL as described in (5).

$$u(t) = Ri(t) + L\frac{d}{dt}i(t) \tag{5}$$

The plant transfer function in s-domain is given by (6).

$$\frac{i(s)}{u(s)} = \frac{1}{R + LS} \tag{6}$$

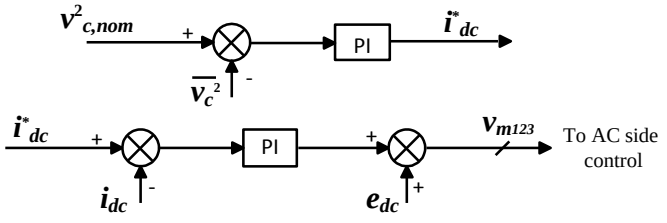


Figure 8: DC side converter control

4.2 AC Side Control

The AC side control strategy (Figure 9) regulates the power exchange between the converter and the AC network by controlling the AC line currents to reference values. A Park transformation is used to transform the three phase AC grid currents to a synchronous reference frame. Parallel PI controllers are then used to regulate the active and reactive current components. These controllers output the demand phase to phase voltages to be synthesised by the converter.

The conduction intervals (modes) of the upper arm diodes are determined from the demanded three phase voltages as presented in Figure 5. Based on the conduction interval, the demand chain-link phase output voltages are then calculated from the relationships given in Table 1 and are then used to modulate the chain-link sub-modules of the converter.

The current controller is designed based on the relationships between the AC side output voltages of the converter and the AC line currents (7).

$$\begin{bmatrix} ud \\ uq \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} id \\ iq \end{bmatrix} + R\begin{bmatrix} id \\ iq \end{bmatrix} + \omega L\begin{bmatrix} -iq \\ id \end{bmatrix} + \begin{bmatrix} ed \\ eq \end{bmatrix} \quad (7)$$

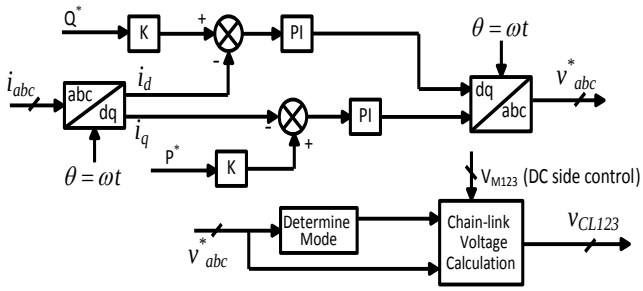


Figure 9: AC Side Converter Control

Both phase-shifted and level-shifted multicarrier modulation strategies can be applied to modulate the sub-modules of this converter as is the practice with other MMCs [13]. Phase-shifted carrier modulation gives reduced floating capacitor voltage ripple compared to level-shifted carrier modulation. Level-shifted carrier modulation on the other hand offers much better harmonic profile and lower converter semiconductor loss [13].

The level-shifted carrier modulation strategy was chosen in this case because of its relative advantages over phase-shifted carrier modulation. However, the modulation strategy does not intrinsically ensure balancing of the floating capacitor voltages and therefore it has to be integrated with a local capacitor voltage balancing algorithm.

The capacitor voltages (Figure 13c) contain line frequency harmonics which are reflected in the DC side voltage of the converter as ripple. This ripple has to be eliminated or otherwise it will result in oscillation in the DC current. Variable carrier amplitude modulation is applied to the level-shifted carriers to eliminate the effect of the capacitor voltage ripple. The amplitudes of the carrier signals are frequently updated to be equal to the sub-module voltage magnitude they are assigned to.

4.3 Capacitor Voltage Balancing Strategy

A sub-module rotation scheme [6] is applied to the sub-module state signals produced by the in-phase level-shifted multicarrier PWM scheme. The scheme equally distributes the sub-module capacitor voltage deviations and ensures that the sub-modules in each phase have a similar average duty over a period of time. The general block diagram of the sorting and rotation scheme is shown in Figure 10.

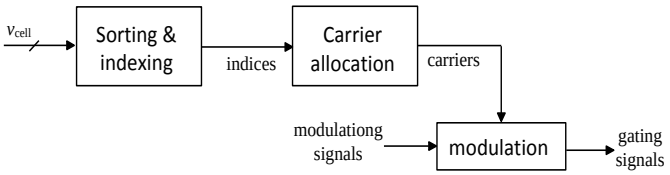


Figure 10: Block diagram of sorting and rotation scheme for the submodule capacitor voltage balancing

The chain-link capacitor voltages are measured regularly and sorted in ascending or descending order depending on whether the operation of the converter results in charging or discharging of the inserted chain-link sub-modules. Based on the amplitude of the sub-module capacitor voltages, indices to virtual locations within the chain-link are assigned. State signals are then assigned to the sub-modules based on their indices. Table 4 shows an example of the application of sorting and indexing algorithm for a six-sub-module converter chain-link.

Sub-module voltages	V1	V2	V3	V4	V5	V6
Measured	1450	1478	1438	1462	1442	1455
Sorted (ascending)	1438	1442	1450	1455	1462	1478
indices	3	6	1	5	2	4

Table 4: Sorting and indexing algorithm

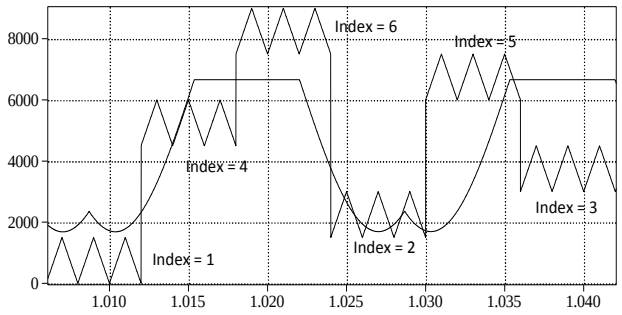


Figure 11: Example of carrier signal allocation for different sub-module indices

The selection of carriers to be assigned to a particular sub-module depends on the direction of the chain-link current. When the current flows in a direction which results in the chain-link capacitors being charged, the carrier signal which produces the highest duty ratio will be assigned to the sub-module with the lowest voltage and the carrier signal which produces lowest duty ratio will be assigned to the sub-module with the highest voltage. Conversely, when the direction of current is reversed and the chain-link capacitors

are discharging, the carrier signal which produces the lowest duty ratio will be assigned to the sub-module with the lowest voltage and the carrier signal which produces the highest duty ratio will be assigned to the sub-module with the highest voltage. Figure 11 shows an example of a carrier allocation for different values of indices determined by the sorting and indexing algorithm.

To avoid extra switching that can be caused by the voltage balancing algorithm, switching state rotation is applied only at switching instants. When an additional sub-module has to be inserted or bypassed, the balancing algorithm will determine which sub-module has to be inserted or bypassed based on the assigned virtual indices.

5 Simulation Results

The proposed SSMMC converter and the control concepts are validated using a representative small scale simulation model with the parameters listed in Table 5**Error! Reference source not found.**. Compared to a full-scale practical implementation, relatively few sub-modules per chain-link are used. However, they are still enough to validate the operation of the converter and the adopted sub-module voltage balancing strategy. The higher number of sub-modules in a full-scale system would greatly improve the waveform quality. An AC interface reactor and transformer leakage inductance of 12% impedance is used (a value in the typical range for HVDC MMC converters) and the chain-link sub-module nominal voltage is 1.5kV.

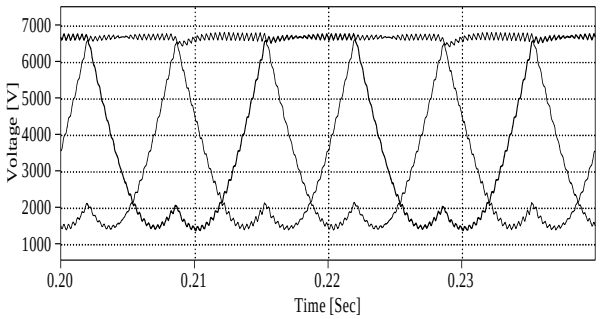
A full switching model of the converter is developed in PLECS simulation package with all the control schemes implemented and the converter chain-links populated with half-bridge sub-modules.

Figure 12(a) and (b) show the demand chain-link voltages for the three chain-links and the synthesised chain-link voltage for phase 'A'. The current through the chain-link for one phase is presented in Figure 12 (c).

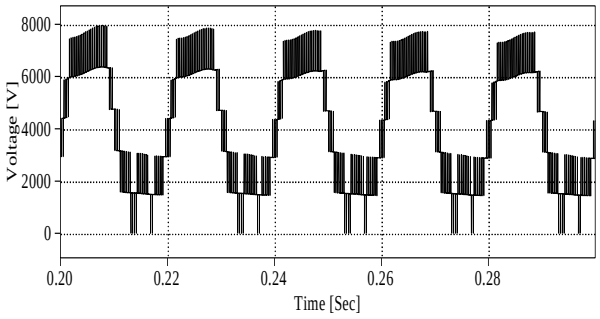
Note that there are multiple commutations of the diodes at the expected commutation points. This is due to quantisation of the chain-link voltages and can be eliminated by coordinating control of the adjacent chain-links – although that is not investigated further here. The output voltages and currents of the other two phases are similar to these waveforms except that they are 120^0 phase shifts between two consecutive phases.

System parameter	Values
Rated power, P	6.7 MW
AC supply voltage, vs (L - L)	3.7 kV
AC Equivalent Inductance, Ls	0.76 mH
DC bus voltage, vdc	6.7 kV
DC-Link Inductance, Ldc	7.35 mH
Nominal Chain-link Voltage, vsub-module	1500 V
Chain-Link Capacitance, C	4.0 mF

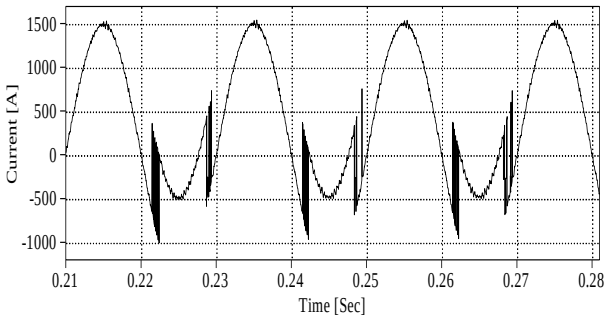
Table 5: Parameters used in the simulation model



(a) Three phase modulating waveforms



(b) One phase chain-link outout voltage

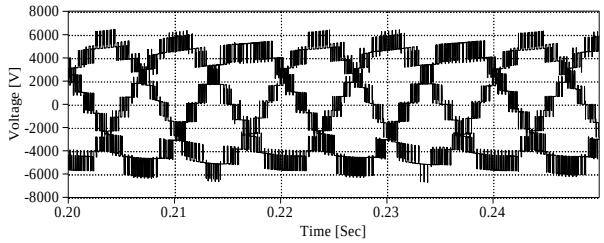


(c) One phase chain-link output current

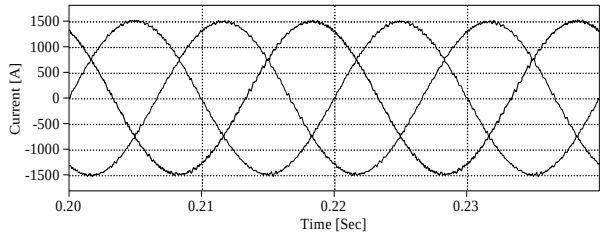
Figure 12: Simulation results of chain-link voltage and current for one converter phase at P = 6.7 MW, Q= 0.

It can be observed that the converter phase to phase output voltages and AC line currents presented in Figure 13 (a) and (b) have high quality. The percentage total harmonic distortion (THD) of the AC voltage is 12.3 %. The waveform quality is expected to be greatly improved in a practical system with high number of sub-modules (typically in the order of hundreds).

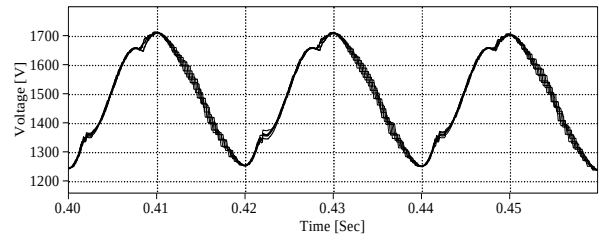
Figure 13(c) shows the chain-link capacitor voltages in a chain-link. The voltages are well maintained within the desired range of operations with a peak to peak ripple of 30%. The 30% peak - peak ripple achieved in this study with 4mF capacitor and six sub-modules per chain-link can be improved with the use of larger capacitance or a higher number of sub-modules if necessary.



(a) Converter phase to phase output voltages



(b) Three phase AC line currents



(c) chain-link capacitaor voltages

Figure 13: simulation results of chain-link phase to phase output voltages and AC line currents at P = 6.7 MW, Q= 0

4 Converter Efficiency and Dimensioning

The semiconductor loss of the converter has been evaluated to establish the converter efficiency and to assess the cooling requirement in a practical demonstrator. The losses have been obtained through well-known analytical methods [20, 21] for VSC semiconductor loss estimation with knowledge of the device forward conduction drop and switching energy (E_{on}, E_{off} and E_{rr}) from an example device datasheet. In this study, the Toshiba MG1200FXF1US53C IGBT with anti-parallel diode, rated 3.3kV 1.2kA, has been selected as a representative device for the loss evaluation.

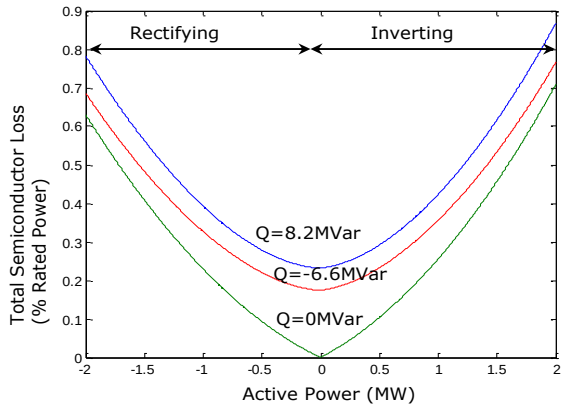


Figure 14: Total Semiconductor Loss as a function of rated power

Figure 14 presents the estimated semiconductor losses as a function of the real power exchanged between the converter and the AC grid. As can be observed from the plot, the semiconductor loss is small as expected; less than 1% of the rated power for all the considered operating points.

To provide an idea of the size of the converter and potential saving in terms of number of submodules and devices required, we provide an estimate of the size of the converter arm and compare these values with a similar rated standard MMC with half bridge submodules. Considering the SSMMC, each converter arm is expected to be able to support the DC bus voltage, similar to the MMC. Consequently, for the SSMMC, the number of submodules required per arm and therefore per phase can be obtained from (8).

$$n_s^{ssmmc} = \left\lceil \frac{V_{DC}}{V_c} \right\rceil \tag{8}$$

However, for the standard MMC [3], two arms are required in each phase of the converter, with each expected to be able to support the whole DC bus voltage. Therefore, the number of submodules in a phase of the MMC can be described as (9).

$$n_s^{mmc} = 2n_s^{ssmmc} \tag{9}$$

From (8) and (9), the number of submodules required for the investigated star switched modular multilevel converter is 50% of that which would be required for the standard MMC for a similar application, ignoring switching effects. Considering that one of the two arms in each phase of the star switched MMC is only responsible for switching conduction from one arm to the other and only sees the line voltage, the number of devices required for the SSMMC can be obtained from (10) and that of the MMC from (11).

$$n_{device} = 3\left(2 + \frac{1}{\sqrt{2}}\right) n_s^{ssmmc} \tag{10}$$

$$n_{device} = 12 n_s^{ssmmc} \tag{11}$$

Considering (10) and (11), the theoretical savings on the number of devices for using the SSMMC can be derived to be 32% of that required for the implementation of the MMC.

5 Conclusion

A hybrid modular multilevel converter that could be considered for HVDC power transmission has been presented. The converter circuit has desirable features for applications requiring low volume as fewer capacitors are required compared to the standard MMC. The basic structure of the converter topology has been described and control schemes supporting the operation of the converter are presented. Semiconductor loss performance of the converter has been estimated considering a scaled medium voltage system and a device count analysis shows that there is a substantial reduction in the number of submodules (50%) and switching devices (32%) compared to that required for the standard MMC.

The expected performance of the proposed converter has been validated through simulation and modelling. Results from the simulation models are presented to validate

successful operation of the converter and the proposed control schemes.

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