Ultra-Low Inductance Design for a GaN HEMT Based 3L-ANPC Inverter

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***Abstract*—In this paper, an ultra-low inductance power cell design for a 3L-ANPC based on 650 V GaN HEMT devices is presented. The 3L-ANPC topology with GaN HEMT devices and the selected modulation scheme suitable for wide-bandgap (WBG) devices are presented. The commutation loops, which are the main contributors to voltage overshoots and increase of switching losses, are discussed. The ultra-low inductance power cell design based on a four layer PCB with the aim to maximise the switching performance of GaN HEMTs is explained. Gate driver design for GaN HEMT devices is presented. Common-mode behaviours based on SPICE model of the converter is analysed. Experimental results on the designed 3L-ANPC with the output power of up to 1 kW are presented, which verifies the performance of the proposed design in terms of ultra-low inductance.**

***Index Terms*—Wide bandgap (WBG) power devices, gallium-nitride (GaN), HEMT, three-level active neutral point clamped (3L-ANPC) converter, photovoltaic (PV) systems**

I. Introduction

600 V normally-off GaN HEMTs are the perfect candidate for grid-connected applications. Such GaN normally-off HEMTs have been introduced by Panasonic at 600 V and GaN Systems at 650 V. There are several practical applications with those WBG devices. For instance, in [1], GaN HEMTs are implemented in a DC/DC converter for the Maximum Power Point Tracking (MPPT) control in PV applications, and the converter exhibited with a peak efficiency of 98.59% at 48 kHz switching frequency. Furthermore, the same devices have been used in other applications such as resonant LLC DC/DC converters, three-phase inverters and synchronous buck converters. Those cases have shown the high switching and conduction performance of the GaN HEMT devices in different operating conditions [2]–[5]. The potential and technology development of GaN devices in power converters is discussed in [2]. Specifically, in [3], GaN devices are adopted on a three-phase inverter with 99.3% efficiency at 900 W output power and 16 kHz switching frequency. The comparison of GaN HEMT with Si IGBT is discussed in [4] for high speed motor drive applications. Finally, GaN HEMTs are demonstrated along with 1200 V SiC MOSFETs in single-phase PV applications in [5], where the converter has achieved 99.2% peak efficiency at 1.4 kW output power and 16 kHz switching frequency. The presented converter proves the stable operation of WBG devices under wide load, switching frequency and ambient temperature conditions. Furthermore, normally-on GaN HEMTs at 600 V voltage class with and without cascode structures are discussed in [6] and [7] for various topologies. More in details, performance improvement in a synchronous buck topology is presented in [6] and it is shown that smaller reverse recovery charge and output capacitance of GaN HEMTs lead to reduction in turn-on losses and up to 2% efficiency improvement in comparison to Si MOSFET. The current collapse phenomena for 600 V normally-on GaN HEMT is presented in [7]. Although the device is statically rated at 600 V, the experimental results are presented up to 50-60 V due to the increase in on-state voltage drop during dynamic testing. Nevertheless, the results presented in the referenced papers show that WBG-based power converters can achieve very high efficiency at high switching frequencies, which is not possible with conventional Si-based power devices. Application and implementation challenges and benefits of GaN devices in high density power converters are discussed in [8] and [9]. Finally, reliability-driven assesment of GaN HEMTs and Si IGBTs in PV systems is discussed in [10].

Active Neutral Point Clamped (ANPC) inverter is a member of the half-bridge neutral point clamped inverter family and it was introduced in [11] as an alternative to the Neutral Point Clamped (NPC) inverter [12] for improving loss balancing and better utilization of semiconductor chip areas in the inverter. Replacing diodes in the NPC inverters with active switches provides additional zero states, and at the same time different modulation strategies can be applied with a flexible utilization of the redundant switching states. The topology has been discussed thoroughly for industrial drive applications in literature [13]–[16]. The schematic of the studied converter for a double-stage three-phase grid-connected PV system is presented in Fig. 1. As it can be observed, each leg of the 3L-ANPC inverter is formed by 6 active switches ($S_1 - S_{18}$ of three legs) in order to achieve a three-level phase output voltage with respect to the neutral point N, and the power devices ($S_1 - S_{18}$) are rated at a half of the DC-link voltage V_{DC}. Consequently, it is possible to use GaN HEMT devices at the 600 V class for three-phase grid-connected applications, where the DC link voltage is within a range of 650-1000 V. In

this configuration, a DC-DC converter between the PV strings and the 3L-ANPC inverter is adopted in order to flexibly maximize the energy production (i.e., MPPT control) as well as to extend the operating hours of the PV systems (e.g., in the case of weak solar irradiance). The power delivered by the DC-DC converter is then fed to the 3L-ANPC inverter, while the DC-link voltage is usually maintained as constant by controlling the inverter. Normally, for the PV system, it should inject high-quality grid currents at unity power factor operation, and thus the modulation schemes applied to the 3L-ANPC inverter should be specially designed.

Different modulation strategies can be implemented for the 3L-ANPC inverter in order to achieve a balanced switching loss distribution or doubling of the effective switching frequency at the output [17]. Solutions proposed in [13]–[16] are limited to the use of Si devices and were optimised for IGBTs as well as for MOSFETs. A modulation strategy based on reverse conduction capability of SiC MOSFETs has been introduced in [18] for a single-phase leg, as further shown in Fig. 2. It can be seen from the driving signals that there are four operating states: 1) positive voltage, 2) zero state positive current, 3) zero state negative current and 4) negative voltage. Specifically, taking the leg-A shown in Fig. 1 as an example, the positive voltage is applied to the output of the phase leg by turning-on S_1 and S_3 and the output current flows through the two devices in series. During the positive active-state, S_4 ensures an equal DC-link voltage sharing between S_5 and S_6 without conducting any current. The transition from positive active-state to zero-state is accomplished by switching S_1 off, and then simultaneously switching S_2 and S_5 on, and thus the current is divided in two parallel paths:$S_2 - S_3$ and $S_4 - S_5$. Same commutation scheme is used for complementary switches during the negative active-state and the zero-state. This modulation method ensures low conduction losses at zero-states, and the outer switches (S_1 and S_6) are exposed to switching losses at unity power factor. In a Si-based converter, IGBTs with antiparallel diodes can be employed; while in GaN based converter, only HEMTs will be sufficient because of the reverse conduction capability of HEMT devices. Therefore, although the number of active devices in Si and GaN will be the same, the number of total switches will be half in GaN based inverter due to the absence of antiparallel diodes, leading to reduced converter volume as well as heatsink size. In addition to Si IGBTs, Si-based super-junction MOSFET at 600 V class can also be counted as alternative device type due to good on-state performance. However, nonlinear behaviour of output capacitance of super-junction devices places large transient load on the complementary switch and extensive reverse recovery charge increases turn-on losses in hard-switching topologies [5].

In this paper, an ultra-low inductance design for 3L-ANPC inverter based on 650 V GaN HEMT devices is presented. In Section II, gate driver design for GaN devices are presented. In Section III, power cell commutation loop design for ultra-low inductance is presented and the common-mode challenges of the proposed design are discussed in Section IV. Finally, experimental results are presented in V.

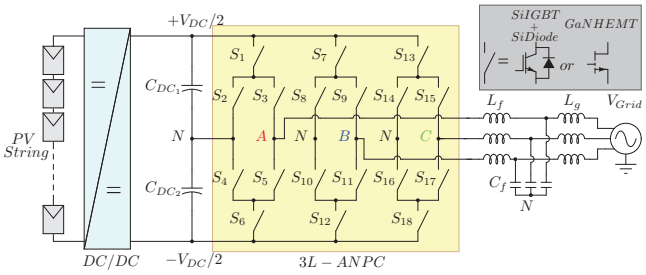


Fig. 1. Grid-connected three-phase double-stage 3L-ANPC inverter with an LCL filter in PV applications

II. Gate Driver Design

The device used in this paper is GS66508T, a normally-off enhancement mode 650 V, 30 A HEMT from GaN Systems. The device parameters are presented in Table I. Although the device is a normally-off e-HEMT, the gate threshold voltage (V_{th}) and input capacitance (C_{iss}) are significantly lower in comparison to Si-based MOSFETs or IGBTs. Therefore, a low inductance gate driver is required with immunity to cross-talking between commutating switches due to high dV/dt capability of GaN HEMTs.

The proposed isolated gate drive design for GaN HEMT devices is presented in Fig. 3. The PWM signal to each switch is transferred by fibre optic link from the control board and passed through an inverting Schmitt trigger in order to avoid any false turn-on or turn-off triggering. The signal is then fed to digital signal isolator for transfer of PWM signal to isolated gate driver circuit with high common-mode dV/dt immunity and low propagation delay. In this arrangement, the Si861x series from Silicon Labs is used as the signal isolator with 50 kV/μs common-mode dV/dt immunity and 10 ns propagation delay. The device also provides 5 kV_{rms} electrical isolation between input and output stages. For the power transfer to gate driver circuit at the isolated side, regulated DC/DC converter with 1 W, +12 V single output and 3 kV_{DC} isolation capability is used. Ideally, the isolation capacitance should be as small as possible in order to avoid interaction between the floating gate driver circuit and non-isolated logic stage. The

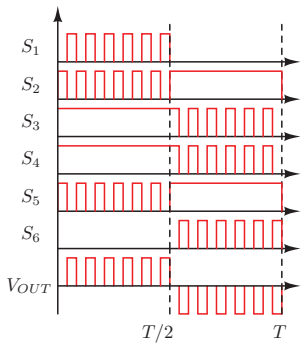


Fig. 2. Switching sequences for leg-A of the 3L-ANPC inverter [18].

TABLE I
GS66508T GAN HEMT PARAMETERS

Drain-Source Voltage (V_{DS})	650 V
Continuous Drain Current (I_{DS})	23 A @ 100 ^{o}C
Drain-Source On-State Resistance ($R_{DS_{ON}}$)	55 mΩ @ 25 ^{o}C
	129 mΩ @ 100 ^{o}C
Input Capacitance (C_{iss})	200 pF
Output Capacitance (C_{oss})	67 pF
Reverse Transfer (C_{rss})	2 pF
Gate Charge (Q_g)	6.5 nC
Min. Gate Threshold Voltage (V_{th})	1.6 V
Gate-Source Voltage (V_{GS})	-10 to +7 V
Maximum Junction Temperature (T_j)	150 ^{o}C
Reverse Recovery Charge (Q_{rr})	0 μC
Package Stray Inductance (L_σ)	0.4 nH
Device Package	GaN$_{PX}$

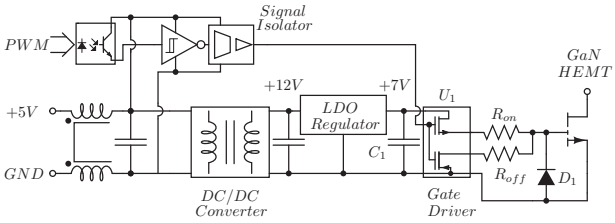


Fig. 3. Gate Driver Design for GaN HEMT.

selected DC/DC converter has 30 pF isolation capacitance. The +12 V output of the converter is then fed to low-dropout regulator to provide +7 V for the supply of non-isolated gate driver. UCC27511 from Texas Instruments is selected as the gate driver IC which provides split output with 4 A and 8 A source and sink peak current capability respectively. Separation of turn-on and turn-off paths provide optimisation of turn-on and turn-off speeds independently for GaN HEMT along with providing immunity to Miller capacitance caused turn-on. As turn-off resistor R_{off} provides low impedance path for positive dV/dt only; during negative dV/dt across the device, the Miller current will flow through the turn-on resistor R_{on}, which is generally selected larger than R_{off}, and create negative spikes across device gate and source terminals. Depending on the resistance value of R_{on} and dV/dt, the negative spike can reach or exceed the limits of the device presented in Table I. Therefore, a clamping diode D_1 across gate and source of the device is placed and presented in Fig. 3 to provide a current path for Miller current during negative high dV/dt conditions. According to these considerations, the R_{on} and R_{off} are chosen as 15 Ω and 1.5 Ω respectively.

The printed circuit board (PCB) design for the isolated stage of the GaN HEMT gate driver is shown in Fig. 4. The design is based on a two-layer PCB with surface mount components in order to achieve low inductance design for high speed operation. As the gate charge of GaN HEMT is significantly lower than SiC or Si based devices with similar current and voltage ratings, low power surface mount packages (e.g. 0603) are used to reduce the footprint of the circuit and also to

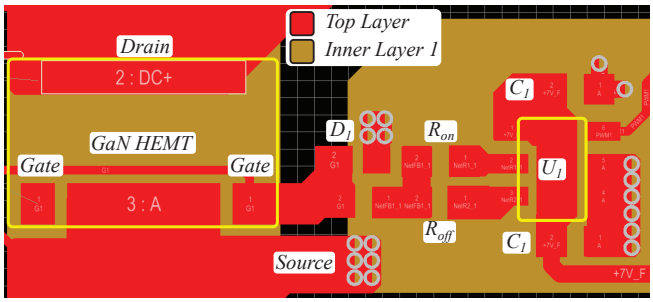


Fig. 4. PCB design for GaN HEMT gate driver.

minimise the gate loop inductance.

III. COMMUTATION LOOP DESIGN

The 3L-ANPC topology provide six different switching states (two for active-states $+V_{DC}/2$ and $-V_{DC}/2$, four for zero-states) for IGBT-based applications. The switching states and commutation schemes are discussed thoroughly for loss balancing and better utilisation of Si IGBTs. In literature, parallel conduction of S_2, S_3, S_4 and S_5 has not been considered as a switching state due to difficulty of the parallel conduction of IGBTs [11]. With respect to any selected switching strategy, S_1 or S_3 may be subject to switching losses for positive output voltage and positive output current. In the selected switching strategy presented in Fig. 2, S_1 and S_6 switches will be subject to switching losses at positive and negative halves of the output waveform respectively with unity power factor operation. The possible commutation loops that can be used for commutating the output current between positive state and upper and lower neutral states formed by $S_2 - S_5$ are presented in Fig. 5. The total commutation inductance formed by the commutation loop stray inductance L and the DC-link capacitor self-inductance L_{DC1} has to be minimised for reducing voltage overshoots and switching losses. The self-inductance of DC-link capacitor can be minimised by paralleling high frequency capacitors (e.g., ceramic, film) and commutation loop inductance by placing conductors that carry opposing currents in adjacent layers to induce magnetic field self-cancellation.

The proposed low inductance commutation loop design for the 3L-ANPC inverter is presented in Fig. 6. It is worth to note that the proposed layout is realized with a low inductance surface mount package of GaN HEMTs. The packaging technology eliminates bond wires and solder joints with extremely low stray inductance of 0.4 nH per device [19]. It is the stray inductance that is a key to achieve high switching speeds while low voltage overshoots and switching losses. In comparison to conventional TO-220 package, stray inductance of the GaN HEMT package has 17.5 times less stray inductance. Six GaN HEMT switches $S_1 - S_6$ are placed on a 4-layer PCB with symmetrical layout where $S_1 - S_3$ are placed on the top side and $S_4 - S_6$ are placed on the bottom side. $S_1 - S_6$, $S_2 - S_4$, $S_3 - S_5$ switch pairs are vertically aligned for providing symmetry between upper and lower sides of the 3L-ANPC phase leg. Top layer and bottom layer of the PCB

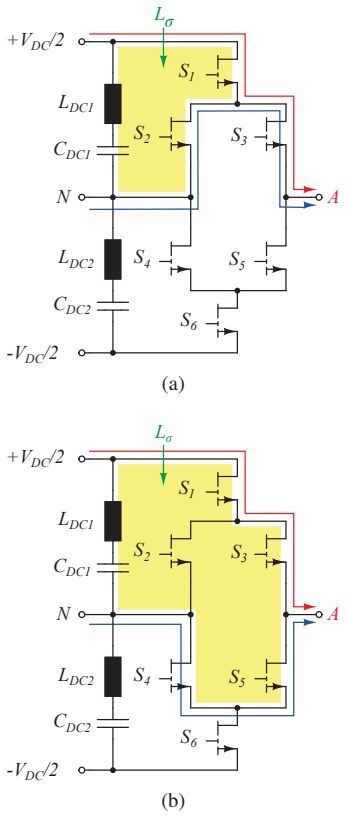


Fig. 5. Commutation loops in 3L-ANPC from positive to neutral states: (a) positive state to upper neutral state (b) positive state to lower neutral state.

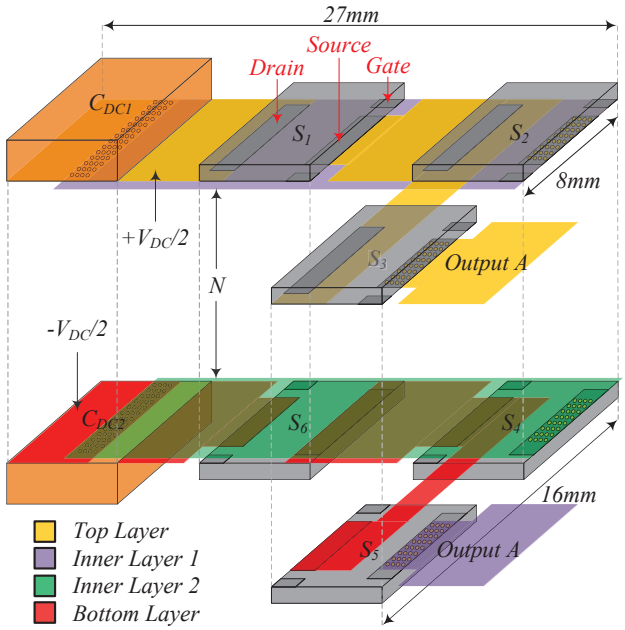


Fig. 6. Power cell design in a 4-layer PCB.

are used for interconnection of DC-link capacitors, switches and connection to $+V_{DC}/2$ and $-V_{DC}/2$ while inner layers are used as return paths and connection to the neutral point.

The stray inductance for each commutation loops presented in Fig. 5(a) and 5(b) can be approximately calculated from the well-known equation of the loop inductance:

$$L_\sigma = \frac{\mu_r \cdot \mu_0 \cdot h \cdot l}{w} \tag{1}$$

where h is height, l is length and w is width of commutation loop, μ_r is the relative permeability of the PCB material (FR4) and μ_0 is the permeability of natural air. The equivalent series inductance L_{DC1-2} of 1 μF, 500 V Ceralink capacitors presented as C_{DC1} and C_{DC2} in Fig. 6 is 2.5 nH per capacitor. The self-inductance of the GaN HEMT package is 0.4 nH per device. The total commutation inductance, which includes stray inductance, DC-link capacitor self-inductance and GaN package inductance, is calculated as 3.51 nH and 5.37 nH for commutation loops presented in Fig. 5(a) and 5(b) respectively. Therefore, the presented structure minimises the commutation loop inductances presented in Fig. 3 and enables very high switching performance of GaN HEMT in the 3L-ANPC topology.

IV. Common-Mode Analysis

The proposed four layer power cell design provides low inductance commutation loops by overlapping GaN devices on top and bottom layer of power cell PCB. Due to the overlap, top devices use top layer and inner layer 1 for gate drive circuits and bottom devices use upper layer 2 and bottom layer for gate drive circuits. The overlap of gate drive planes and tracks create a parasitic capacitance between drain and source nodes of overlapping devices and presented as C_{S1}, C_{S2}, C_{S3} and C_{S4} in Fig. 7. The parasitic capacitances can be calculated by the following equation:

$$C_s = \frac{k \cdot \epsilon_0 \cdot A}{d} \tag{2}$$

where k is the relative permittivity of the dielectric material between each PCB layer, ϵ_0 is the permittivity of pace, A is the overlapping area of planes and d is the thickness of FR4 between each layer. According to material properties and calculated overlapping areas, the parasitic capacitances C_{S1}, C_{S2}, C_{S3} and C_{S4} are calculated as 57.4 pF, 43 pF, 44.7 pF and 17 pF.

By using GaN HEMT and gate driver components (e.g. gate driver IC, DC/DC converter) SPICE models, circuit presented in Fig. 7 is simulated for the positive half-cycle of output voltage in LTSpice to investigate the common mode current flow through parasitic capacitances and logic circuit. In the simulation, the common-mode inductor at the input of each gate driver is omitted in order to evaluate the current flow through the non-isolated side of the circuit. The common-mode currents through parasitic capacitances C_{S1}-C_{S4} with respect to rise of output voltage from 0 to 350 V are presented in Fig. 8. The results show that the parasitic capacitances cause circulating current flow between devices with large amplitude due to high dV/dt. The impact of this current flow to non-isolated logic side due to isolation capacitance of DC/DC

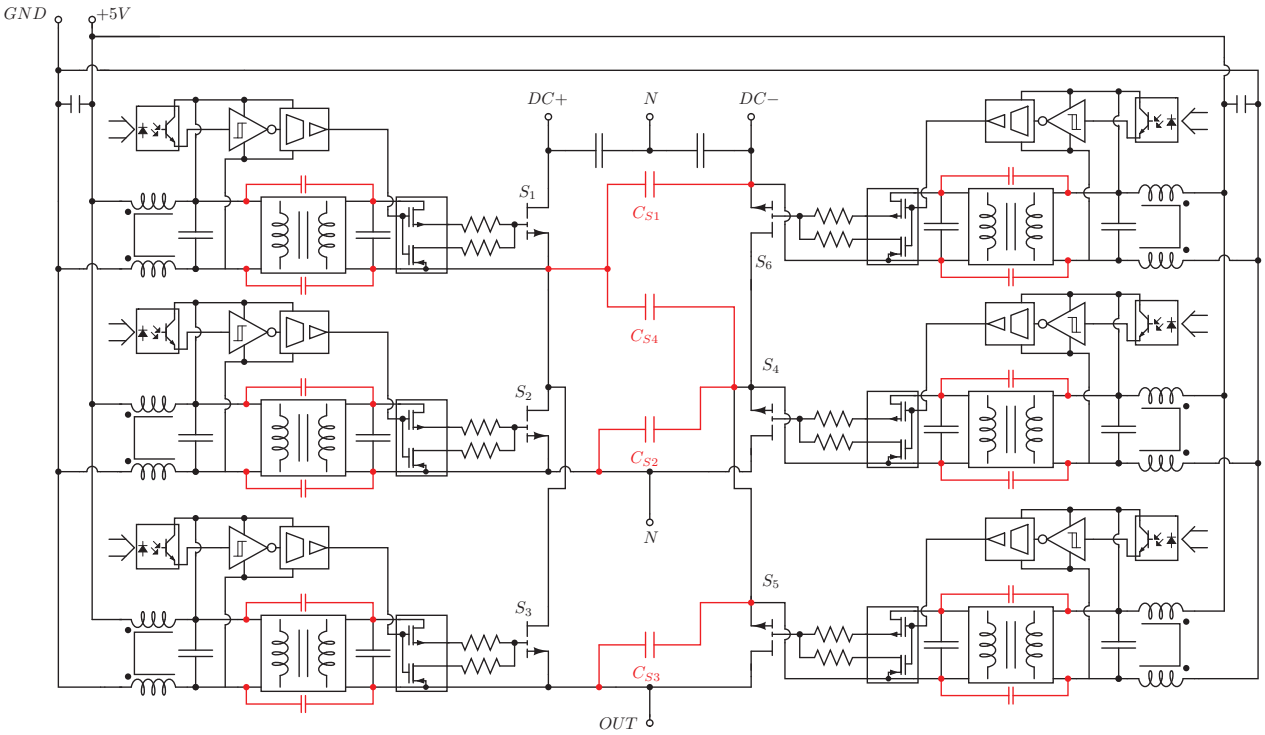


Fig. 7. Single phase 3L-ANPC switching cell with parasitic capacitances.

converters is presented in Fig. 9. Although the amplitude of common-mode current at non-isolated stage is significantly lower, it is still higher than logic current levels and can interfere with signal conditioning, causing false triggering. In order to suppress the common-mode current flowing through the non-isolated stage, common-mode chokes with value of 470 μH is place at the input of each gate driver. The placement of common-mode choke prevents the common-mode current from flowing through the non-isolated side of the circuit and contains the current circulation within the power cell. In order to fully eliminate the common-mode current circulation, the additional plane can be introduced between inner layer 1 and inner layer 2 with the penalty of increasing number of layers from 4 to 6. Another possibility is replacement of gate drive planes to avoid any overlaps between top and bottom side switches' gate drive circuits. This arrangement might increase PCB design complexity.

V. Experimental Results

The performance of 600 V Si IGBTs has been well studied in literature for different applications and some of these results have been discussed in the referenced literature. On the other hand, normally-off 650 V GaN HEMTs with low inductance package recently emerged for power electronic applications. Therefore, a GaN HEMT based single phase ANPC inverter demonstrator has been designed and built-up. The performance of GaN HEMT devices is experimentally evaluated and presented in this section.

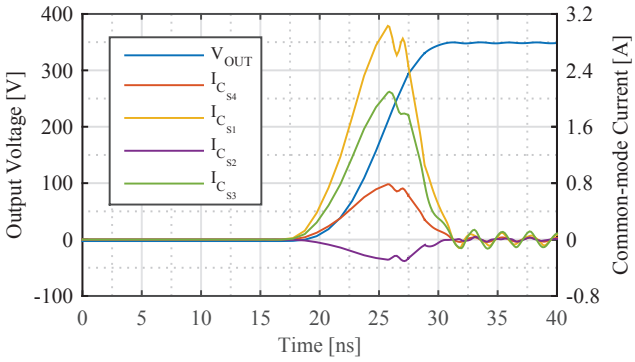


Fig. 8. Common-mode currents through parasitic capacitances with respect to output voltage rise.

The GaN HEMT based single phase ANPC inverter is presented in Fig. 10(a) and 10(b). The power cell is formed by four-layer PCB with 140 μm copper on each layer. The power cell consists of high frequency DC link capacitors, GaN HEMT switches, gate drivers, signal and power isolation circuits for gate drivers and fibre optic receivers for gate signals. The $S_1 - S_3$ GaN devices are placed on top side of the PCB while $S_4 - S_6$ GaN devices are placed on bottom side of the PCB in symmetry to $S_1 - S_3$ for minimised commutation loop and high switching speed. The PCB is designed to have a modular system with the option to extend the demonstrator to three-phase by stacking PCBs vertically. Regarding cooling

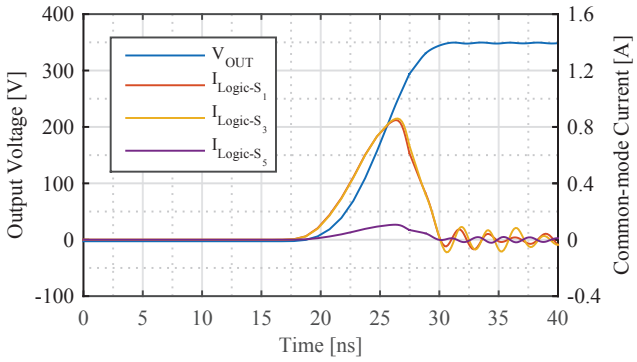


Fig. 9. Common-mode currents through non-isolated logic circuit with respect to output voltage rise.

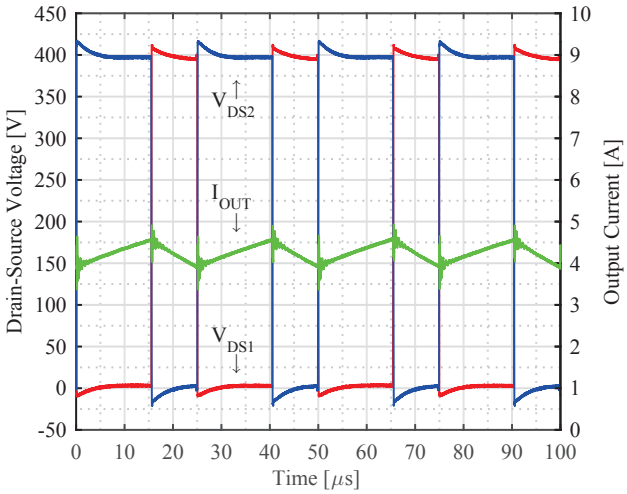
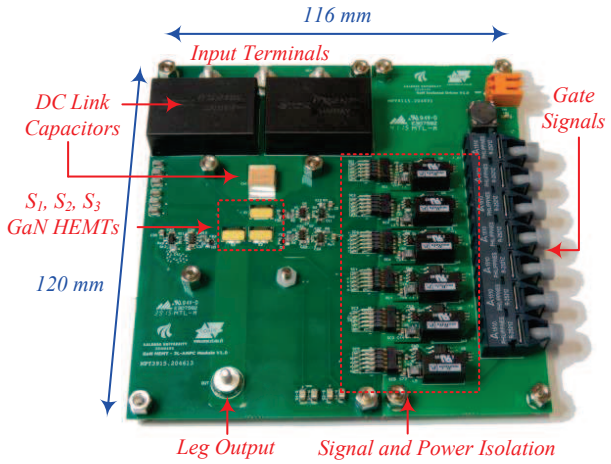
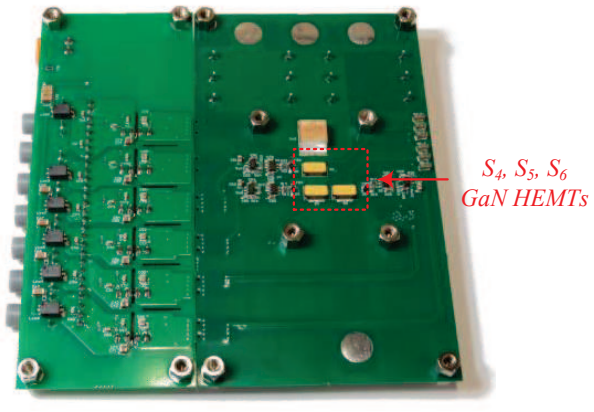


Fig. 11. Performance of the GaN HEMT in the 3L-ANPC inverter with buck configuration.



(a)



(b)

Fig. 10. Hardware of the GaN HEMT based single phase ANPC power cell: (a) top view and (b) bottom view.

of power switches, two commercial heat sinks are used. The heat sinks are joined by 4 screws with compression springs in order to apply equal contact pressure to the devices from top and bottom part of the PCB. The PCB has been presented without heat sinks in order to show device positions on the board.

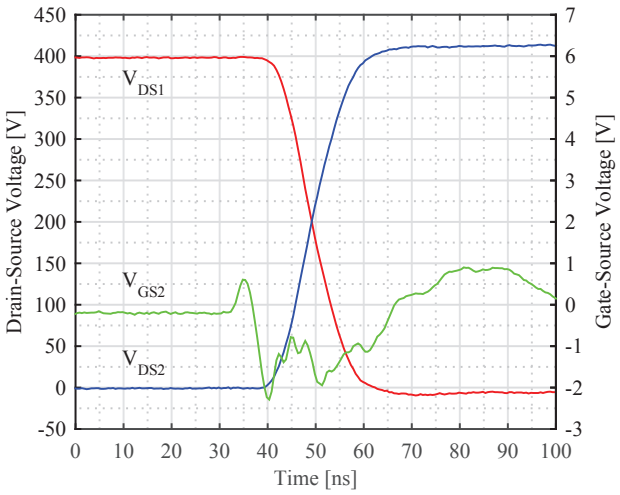
A. Switching Performance

The ANPC power cell is initially operated as a buck DC/DC converter in order to evaluate switching performance of GaN devices and designed power cell. For buck configuration, upper switches $S_1 - S_3$ are used where S_3 is kept on during the switching period and complementary gate signals are applied to S_1 and S_2 with 200 ns dead-time.

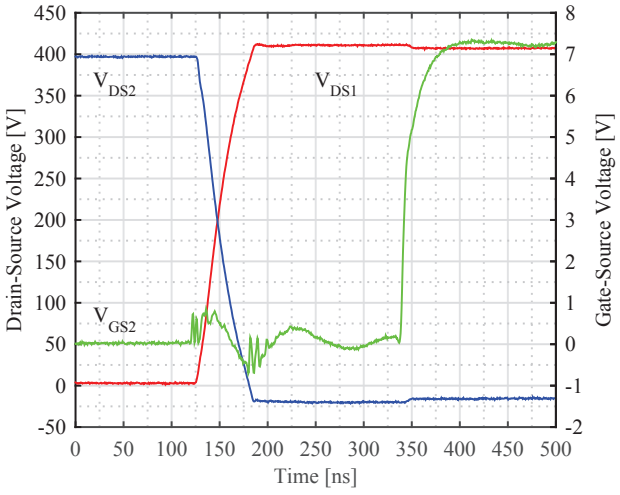
The switching waveforms at 40 kHz switching frequency with 400 V DC link voltage and 1 kW output power are presented in Figs. 11 12(a) and 12(b). The successful operation of switches in buck configuration is presented in Fig. 11 with device voltages and output current. In Fig. 12(a), the output current commutates from S_2 to S_1 and S_1 is subject to hard-switching. The commutation from S_1 to reverse conduction of S_2 is presented in Fig. 12(b). Drain-source voltage waveforms V_{DS1} and V_{DS2} prove high switching speed of GaN HEMTs with 13.2 ns rise and fall time of V_{DS2} and V_{DS1} respectively.

B. Inverter Performance

The single phase 3L-ANPC inverter prototype in Fig. 10 is tested with 700 V DC link, 10 kHz switching frequency to demonstrate performance of GaN based power cell without heat sink. The inverter test setup is presented in Fig. 13. The inverter is powered by a DC power supply with DC link decoupling capacitors. An RL load configuration is used for evaluation of performance under different load conditions. Efficiency and losses of power cell is measured by Yokogawa WT3000E precision power analyser with 0.01% power accuracy.



(a)



(b)

Fig. 12. Switching performance of the GaN HEMT in the 3L-ANPC inverter: (a) device voltage and output current, (a) hard commutation and (b) soft commutation waveforms with buck configuration.

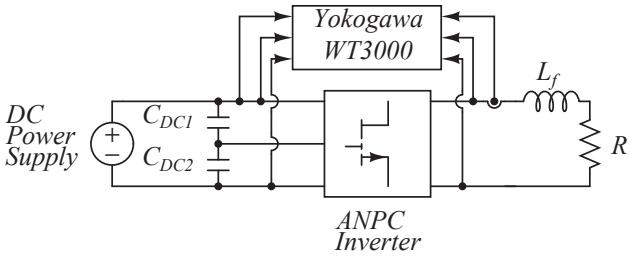
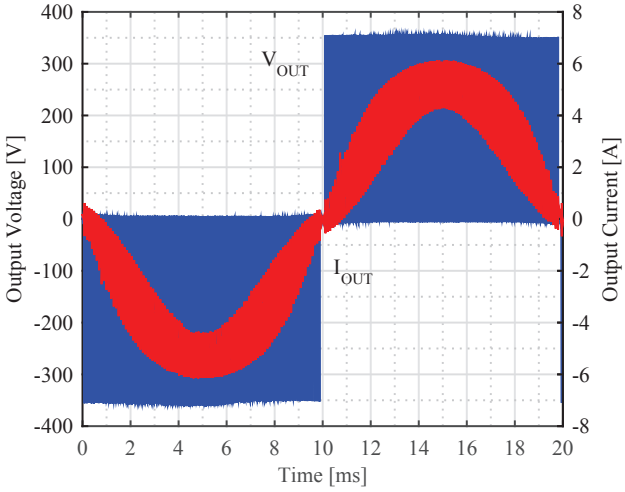
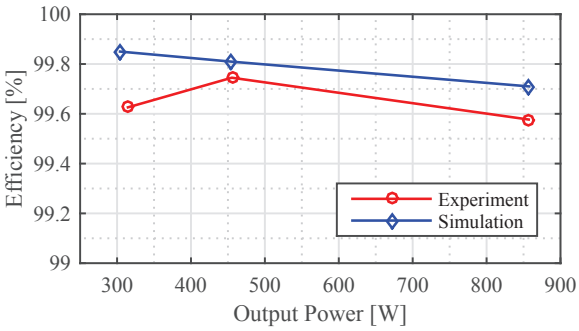


Fig. 13. Inverter test setup.



(a)



(b)

Fig. 14. (a) Experimental output voltage and current waveforms at 800 W output power and (b) efficiency of the 3L-ANPC power cell with experimental and simulation results.

The experimental output current and voltage waveforms, and power cell efficiency with experimental and simulation results are presented in Fig. 14 (a) and (b), respectively. The experimental results support validity of high performance of GaN HEMT devices in simulation compared with Si IGBTs. The efficiency comparison in Fig. 14 (b) validates the performance assumption of GaN HEMTs in the inverter operation mode.

VI. Conlusion and Future Work

In this paper, an ultra-low inductance power cell design based on 3L-ANPC topology and low inductance surface mount package GaN HEMT devices has been presented and experimentally demonstrated. The experimental results show that with the proposed layout, 13 ns rise time at 350 V blocking can be achieved with 20 V voltage overshoot at 1 kW output power. The layout also comes with the challenge of common-mode current circulation that can be eliminated by arranging gate drive placement carefully or by introducing shielding between top and bottom device gate drive circuitry. As part of the future work, the optimisation of switching

frequency with respect to output filter size and converter efficiency will be carried out.

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