Sizing of Power Electronics EMC Filters Using Design by Optimization Methodology

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***Abstract*—This paper proposes a synthesis of EMC filter design method for power electronics converters. It starts with the description of the legacy approach, using the usual Common Mode / Differential Mode decomposition, and underlines the need of symmetry and the associated limits. Then an illustration of a design by optimization process is provided in the case of a simple switching cell. Finally, a full system composed of a PFC rectifier is provided, using EMC filters on both AC and DC sides. This example requires a design by optimization, since the two filters exhibit strong interactions.**

Keywords—Power Electronics, EMC, Design by Optimization

I. INTRODUCTION

Power Electronics can be seen as the major "enabling technology", which initiated the "More Electrical" trend of the XXI century. However, if the switching mode power conversion allows high efficiency and easy control of the electrical power, it also generates high frequency disturbances, especially due to harmonics of absorbed currents and voltage, and also to stray currents induced in the ground. The mitigation of these stray effects is mandatory in modern systems where all becomes "all electronic", with higher susceptibility to external noise. The "ElectroMagnetic Compatibility" vocabulary has been launched in the early 90's [1], and is today a mandatory step in converter design. EMC filters are a significant part of the weight and cost of a power converter, very often between 25% and 40% of the total converter [2]. The specificity of EMC filters of Power Electronics converter is that the design has to account for the high voltages and currents operated in the converter, therefore, design constraints are not only the attenuation of noise, but also limited losses and saturation for filter components. With the development of power electronics in embedded networks, as aircraft or automotive applications, the weight reduction becomes clearly a major challenge that has to be addressed. For instance, the first studies of More Electrical Aircraft have led to the conclusion that it was not so interesting in comparison with conventional hydraulic systems, due to the added weight of power electronics converters [3]. In this context, the EMC filters are obviously under concern, and have to be designed according to a minimum weight. Two parallel strategies can be defined: either technological integration, to reduce the filter weight by using new materials and technologies [4-5] or design by optimization, by trying to use at best given technologies and materials. This second approach will be proposed in this paper. Part II will start with the conventional way to design filters, and remind the basics notions used in EMC filter design. Part III will introduce the design by optimization concept for EMC filters, applied to a simple switching cell. Finally Part IV will present a full converter including two filters, which have to be designed simultaneously due to a strong interaction. The major advantage of design by optimization will be underlined in this case.

II. CONVENTIONAL FILTER DESIGN

A. Common Mode Differential Mode Separation

EMC investigations and filter design widely uses the well-known Common Mode (CM) Differential Mode (DM) separation. The mathematical definition of this specific EMC basis is reminded hereafter, according to the notations of Fig.1.

$$\begin{bmatrix} V_{DM} \\ I_{DM} \\ VCM \\ I_{CM} \end{bmatrix} = [P] \cdot \begin{bmatrix} V_1 \\ V_2 \\ I1 \\ I_2 \end{bmatrix} \text{ with } [P] = \begin{bmatrix} 1 & -1 & 0 & 0 \\ 0 & 0 & \frac{1}{2} & \frac{-1}{2} \\ \frac{1}{2} & \frac{1}{2} & 0 & 0 \\ 0 & 0 & 1 & 1 \end{bmatrix} \quad (1)$$

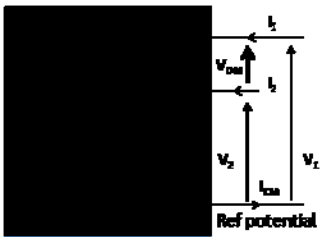

Fig. 1. Conventional quadrupole notations and link with CM/DM basis

The main difference with conventional electrical dipole representation used by electrical engineers is to take into account the reference potential and the associated current I_{CM}. V_{DM} is simply the natural voltage used between wires, and if I_{CM}=0, I_{DM} becomes I_1. As illustrated in [6], the main interest of this CM/DM representation is that it allows solving the quadrupole equations using two uncoupled systems, corresponding to a dipole for CM and another dipole for DM,

provided that the electrical circuit is symmetrical. This can be simply illustrated in Fig.2 and equation (2) & (3). The link between V_1, V_2 and I_1, I_2 is clearly coupled since it is a quadrupole, and the expression of the same relation in the DM/CM basis underlines that for a symmetrical circuit (i.e. $Z_1 = Z_2$), the two equations (3) in DM and CM become decoupled.

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 1/Z_{12} + 1/Z_1 & -1/Z^{12} \\ -1/Z_{12} & 1/Z_{12} + 1/Z^2 \end{bmatrix} \cdot \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} I_{DM} \\ I_{CM} \end{bmatrix} = \begin{bmatrix} 1/4Z_1 + 1/4Z_2 + 1/2Z_{12} & 1/2Z_1 - 1/2Z_2 \\ 1/2Z_1 - 1/2Z_2 & 1/Z_1 + 1/Z^2 \end{bmatrix} \cdot \begin{bmatrix} V_{DM} \\ V_{CM} \end{bmatrix} \quad (3)$$

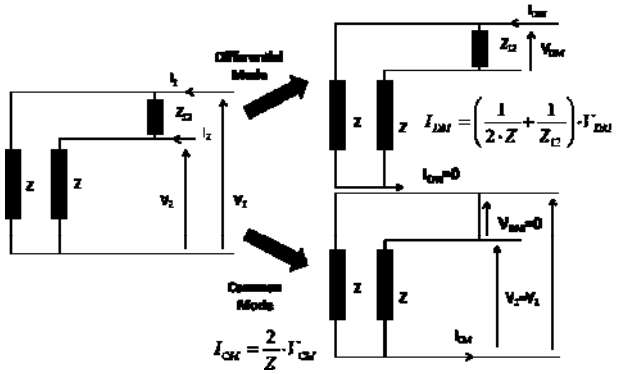

Fig. 2. Conventional quadrupole notations

In a more general case developed in [6], it is clearly shown that for a symmetrical link illustrated in Fig.3 (i.e. Z5 = Z6 and Z2 = Z3), the relations between input and output becomes decoupled if expressed in the CM/DM basis.

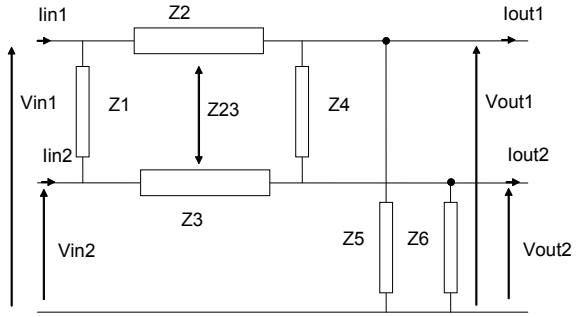

Fig. 3. Electrical link representation (from [6]). The relation between input and output becomes decoupled if symmetrical and expressed in CM/DM basis

Therefore, the CM/DM representation allows simplifying the study of the ElectroMagnetic Interferences (EMI), by solving only dipoles instead of quadrupoles, but it is crucial to keep **symmetry** of the electrical circuit.

B. Filter topologies

EMC filters for power electronics usually use simple second order filters. The topology of these filters depends on both converter and line impedances [7].

For DM filter, the topology supposes a low impedance on the converter side and a high one on the line side. Therefore, the topology is the one of Fig.4a. For CM filter, the converter impedance is supposed to by high, and the line one can be quite low, leading to the topology of Fig.4b.

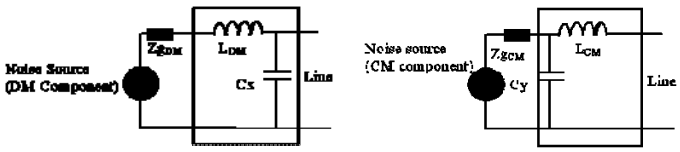

Fig. 4. a) typical DM filter b) typical CM filter

The filter attenuation is defined by Eq. (4)

$$AdB = 20.Log\left(\frac{V_{line\_without\_Filter}}{V_{line\_with\_Filter}}\right) \quad (4)$$

With some assumption on converter impedances in DM and CM ($Z_{gDM} = 0$, $Z_{gCM} >> Z_{line}$), both attenuations for DM and CM filters are given by Eq. (5) and Eq.(6) (Z_N being the Line impedance, represented by a Line Impedance Stabilization Network)

$$A_{DM} = 20.Log\left(1 + \frac{L_{DM}}{2.Z_N} \cdot s + L_{DM} \cdot Cx \cdot s^2\right) \quad (5)$$

$$A_{CM} = 20.Log\left(1 + \frac{Z_N}{2} \cdot Cy \cdot s + L_{CM} \cdot Cy \cdot s^2\right) \quad (6)$$

C. Design methodology

The legacy approach consists in measuring the EMI on the LISN, in the CM/DM basis, without any filter. These disturbances are compared to the required standard, in order to determine the desired attenuation on the whole frequency range. Then the cut-off frequency of the filters, both in DM and CM, are adjusted to provide the needed attenuation. This design process is illustrated in Fig. 5 in the case of CM. In this figure, a 2kW Buck converter has been considered (parameters given in Table I) and simulated using Pspice with a quite precise ElectroMagnetic environment (stray inductances, stray capacitances, Pspice models of components).

Once the cut off frequency has been found, the determination of the filters elements L and C depends on technological considerations. Very often, most of the filter weight and volume come from the magnetics [8], and therefore capacitances are increased. For Cx (DM), the limitation may be the bandwidth, due to esl (equivalent series inductor) which may be too large for big capacitances. For Cy (CM), safety issue arises due to the connection of these capacitors to metallic parts which are accessible to the users. In our example, Cx has been limited to 6.8µF, and Cy (between power line and chassis) to 28nF, according to EN

501178, Annex A.5.2.8.2 table A1 (DC Voltage = 400V). These quite high values of capacitance lead to small values of magnetics (what was the objective). The discussion in part D will underline some limitations of this choice.

Last, the implementation on the CM and DM filters on the converters power lines has to guarantee the symmetry rule, therefore, the final scheme is the one depicted in Fig.6. The values of the line elements account for the splitting of each filter among the two lines, as well as for the coupling of magnetics between the two lines. This magnetic coupling is interesting to reduce the size of CM filter, and also allows avoiding the influence of DM inductance on CM one and vice versa. At this point, all filter components are supposed to be ideal, including the coupling. Obviously this will not be the case in real life, but it will not affect the global design of the filter, since these stray effects only impact the high frequency behavior. Only the unit magnetic coupling is too optimistic, but it can easily be taken into account when realizing the components, by modifying the desired inductances, accounting for the leakage inductances.

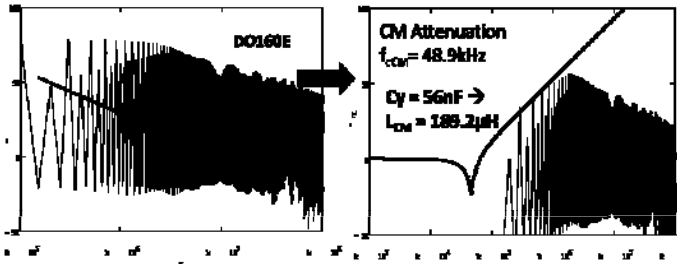

Fig. 5. Illustration of the desired attenuation and the choice of cut-off frequency in the case of CM for the Buck converter under study.

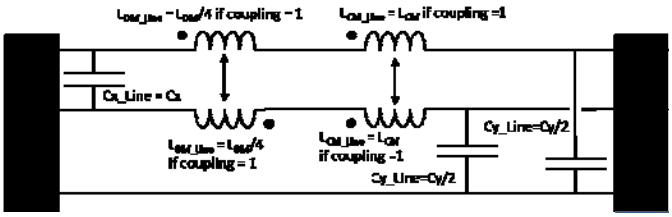

Fig. 6. Implementation of the DM and CM filter on the power lines, accounting for the necessary symmetry and the coupling of magnetics between lines.

D. Limitations of the Conventional Method

The legacy design method is based on the symmetrical realization of the filter. If, for instance the DM filter is not equally split among the two power lines, despite the good inductor and capacitor values for achieving the filter, the circulation of CM current generates different voltage drops on each part of the DM inductor, what creates additional DM noise. Moreover, the conventional design method supposes that the optimum corresponds to a maximization of the capacitors. In the considered example, this is not true. Indeed, the global weight of capacitors is evaluated to 50g when the filter mass is 54g ! There is thus another possible optimum to be found with increased inductances and lower capacitance.

Also, all attenuations have been obtained under the assumption that the converter impedances are either zero or very large in DM or CM. When trying to obtain better performances in terms of weight for EMC filter, all these assumptions will perhaps no more be valid, and design by optimization must be more generic. This will be detailed in the next section.

TABLE I. CONVERTER AND FILTER PARAMETERS

Power Converter			
Power		2kW	
DC Input Voltage		400V	
DC Output Current		10A	
Switching Frequency		100kHz	
Duty Cycle		0.5	
Input Capacitor		Cin= 400µF, esl = 10nH, esr=0.2Ω	
EMC Filter			
F_{cDM} = 37.7kHz F_{cCM} = 48.9kHz			
CM/DM basis		Power Line Values	
L_{DM}	2.6µH	L_{DM_Line}	650nH – Coupling -1
Cx	6.8µF	C_{x_Line}	6.8µF
L_{CM}	189.2µH	L_{CM_Line}	189.2µH Coupling 1
Cy	56nF	C_{y_Line}	28nF

III. DESIGN BY OPTIMIZATION IN A SIMPLE CASE

A. EMC Model of a Switching Cell

The time domain simulation can be used to investigate the EMI from a power converter, as shown in the previous part. However, simulation time, memory space, convergence issues are often associated with this kind of simulations, and this is definitively not adapted to optimization. Therefore, the model of the switching cell in the frequency domain is preferred [9]. The idea of this modeling method is to replace the switching devices by equivalent sources, reproducing the voltage and current discontinuities. For the considered Buck converter, the equivalent circuit is given in Fig.7: the current source corresponds to the switch current and the voltage source to its voltage. These sources can be expressed in the frequency domain, either by a FFT of the switch signals (simulated or measured), or by approximating these waveforms with simple slopes and performing the Laplace transform of these sources. Then, the converter is associated with the filter to be designed and the LISN, and the disturbances can immediately be evaluated using the formal resolution of the equivalent circuit of Fig.7 in the frequency domain.

B. Optimization Principle

The design methodology starts from technological description of the components : EMC filter inductors and capacitors are characterized by geometrical data and material properties, or interpolated from manufacturer datasheets. Then, electrical quantities, such as capacitance, inductance,

but also maximum flux, maximum current density or rms current, … are obtained thanks to analytical formulas. Voltage and current ripple are also evaluated, as well as EMC behavior using the equivalent circuit of Fig.7-bottom. Other additional constraints such as the cooling system of the semiconductors can be added, but will not be developed in this paper. The full optimization process is illustrated in Fig. 8. All models are implemented in a specific optimization framework developed in our lab [10].

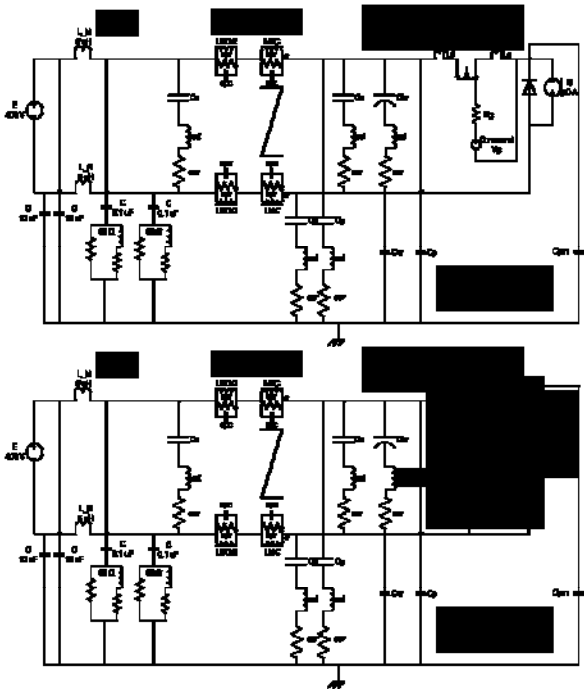

Fig. 7. Top: buck converter model - Bottom: Equivalent circuit for EMC studies.

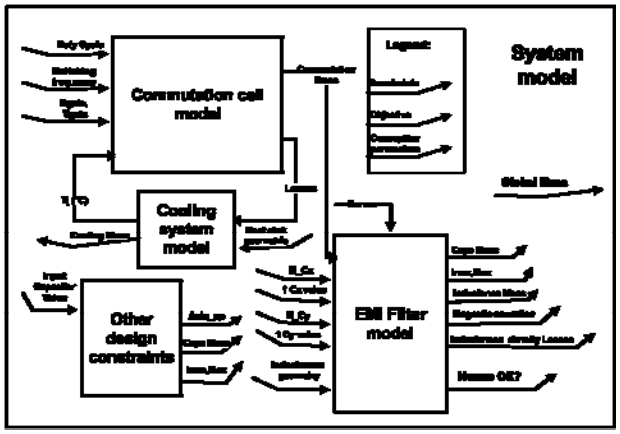

Fig. 8. Design methodology.

In reference to Fig.8, the cooling system has not been considered. The capacitor model is simply an interpolation of manufacturer datasheets, providing the weight of the capacitors as a function of the capacitance, for both technologies Cx and Cy (Fig. 9). Several capacitors can be associated in parallel if needed. As explained previously, the inductors are described using technological variables: a toroidal core is used, with homothetic variation (changing its heights –one of the design parameters– changes all other size), the turn number is also a design variable, as well as the wire diameter The magnetic material is fixed. Permeability has been chosen at 60 for DM inductor, and 5000 for CM one. To avoid any saturation, the maximum flux in the core is a constraint during the optimization process. For the Common Mode inductor, the peak flux results both from peak CM current and non-perfect coupling between the two wirings (leakage flux). The peak Common Mode current is evaluated using the equivalent frequency of the MOSFET voltage slope [4], and the leakage effect is taken into account using [11].

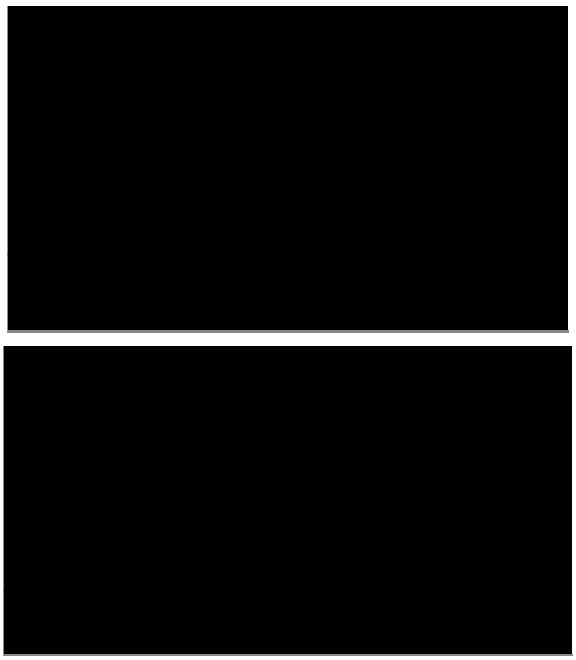

Fig. 9. Top: Interpolation for Weight vs Capacitance. Top: Cx – Bottom Cy

C. Results

The optimization of the proposed buck converter has been performed to respect all design criteria (maximum current density, saturation …), including the EMC standard DO160E. The main optimization results are given in Table II. As stated in the discussion of the previous section, the optimal design does not anymore result in increasing the capacitors, since it has been shown that the magnetics were very small in the previous design. It is worth noting that the cut off frequencies for DM and CM has not changed a lot in comparison with the legacy design. Indeed, the considered converter is symmetrical; therefore, the mode separation assumption (what is the basis for legacy approach) is valid. Also the non-perfect coupling of the CM inductor replaces the DM filter (the leakage inductor of the designed CM filter is evaluated to 38µH, which is sufficient for filtering the DM noise.

D. Discussion

The Design by Optimization performed in this simple application example shows that the optimum design does not correspond to the legacy approach. Of course, in this simple case, other approach may have provided more or less the same results, but it should be noticed that we kept the system simple

in order to present the methodology. For instance the converter has been symmetrical, what avoids any mode coupling. Furthermore, the presented methodology only focused on EMC filter design, keeping all other parameters constant. The full methodology also applies by changing the switching frequency, the driver parameters, the input capacitor, … but it is out of the scope of this paper. Next section will illustrate how the method can also be applied to a more complex topology: a three phases PFC rectifier with both input and output filters.

TABLE II. EMC FILTER LEGACY DESIGN AND OPTIMIZATION RESULTS

Legacy design		Optimization Results	
L_{DM_Line}	650nH – Coupling -1	L_{DM_Line}	38µH (CM leakage)
C_{x_Line}	6.8µF	C_{x_Line}	467nF
L_{CM_Line}	189.2µH Coupling 1	L_{CM_Line}	479µH Coupling 0.92 (computed)
C_{y_Line}	28nF	C_{y_Line}	14.6nF
Weight 55g		Weight: 13g	

IV. APPLICATION TO PFC RECTIFIER

A. Studied Converter

In comparison with the previous example, the power range is completely different. We keep the aircraft application, but we try to design a converter between the HV AC grid and a HV DC grid. According to the system optimization presented in [12], the AC network voltage is fixed to 350V-400Hz and the DC voltage to 990V. The power is 120kW. The switching frequency is fixed to 40kHz. The circuit is given in Fig. 10. It is worth noting that we decided to insert two different LISN, one at the input and one at the output. Indeed, even if it is not described in the DO160, we wanted to fix the EMC environment of this converter, and there is no specific load to plug on the DC side. Therefore, two LISN are the best way to provide a known environment for the EMC study of the converter. The boost inductors are fixed (51.2µH) according to current ripple, the output capacitor (13.6µF) according to voltage ripple. Some stray capacitances are added in order to be representative of CM noise generated by the converter. The floating points of the PFC legs (100pF) and the DC bus stray capacitance (300pF) are thus considered. The filter topology on the AC side and on the DC side are shown on Fig. 10.

B. Manual Filter design

Designing both input and output filters is not an easy task. Indeed, the C_{y_AC} capacitors on the AC side may originate an additional CM current, especially if the boost inductors are non-perfect (i.e. exhibit a stray parallel capacitance). Therefore, if increasing these C_{y_AC} reduces the disturbances measured on the AC LISN, it may increase the noise on the DC one. In the same idea, increasing the C_{y_DC} capacitors reduces the high frequency impedance on the DC side and thus may increase the CM current on the AC side [12-13]. Therefore, both DC and AC filters have coupled effects on both noise on DC and AC LISN, and therefore should be designed simultaneously. To perform the design, we fixed all capacitors to the maximum allowed values and used the trial and error method with a time simulation software, varying the CM and DM inductors (DC and AC) until we fulfilled the DO160F on both AC and DC sides. Table 3 shows the obtained results.

TABLE III. EMC FILTER MANUAL DESIGN FOR PFC

AC side		DC side	
L_{DM_AC}	350µH	L_{DM_DC}	614µH
C_{x_AC}	1µF	C_{x_DC}	500nF
L_{CM_AC}	200mH	L_{CM_DC}	180mH
C_{y_AC}	8nF	C_{y_DC}	8nF
Total Weight: 98.88kg			

C. EMC equivalent circuit and optimization models

In order to use the Design by Optimization method, we have to provide models for all physical phenomena to be taken into account. We used exactly the same models as in the previous section (just adapting the boundaries for the core size, and the manufacturer datasheets for capacitor interpolation).

Regarding EMC model, we used the same approach as presented in section III, representing all current/voltage variations by equivalent sources. As a result, three voltage sources are replacing the three bottom switches of the three PFC legs, whereas one single current source allows reconstructing the DC current exciting the DC output capacitor and the DC circuit (including the DC filter, stray elements and DC LISN). The equivalent circuit is depicted in Fig. 12.

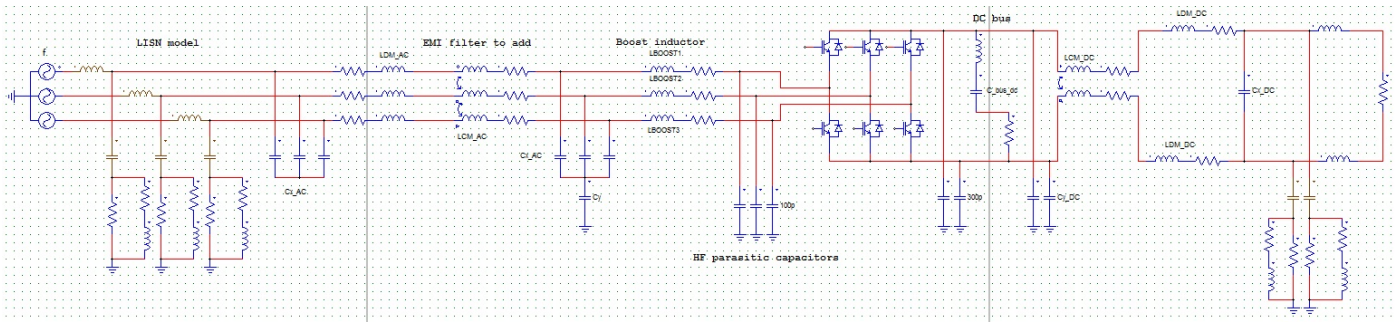

Fig. 10. Circuit description of the PFC with the two LISN and the two filters

D. Optimization Results

Results are provided in Table IV. To facilitate comparison, we kept the capacitors identical and just optimized the inductors. Obviously, a full optimization is feasible. The optimization result shows an improved global weight. The DM inductors are so small that they are part of the Common Mode inductors (using the leakage). As shown in Fig.11, the EMC constraints are respected, on both DC and AC side, and the EMC model used (CADES in Fig. 11) exhibit a good agreement with the time simulation software. With this result, the Design by Optimization method is validated on a complex case, and shows a quick convergence to more or less the same optimal point as the one obtained after a long and boring trial and error method. Furthermore, additional degrees of freedom can be considered, as filter capacitors, switching frequency… what would lead to more global results.

TABLE IV. EMC FILTER MANUAL DESIGN FOR PFC

EMC Filter			
AC side		DC side	
L_{DM_AC}	486µH (leakage of CM)	L_{DM_DC}	540µH (leakage of CM)
C_{x_AC}	1µF	C_{x_DC}	500nF
L_{CM_AC}	236mH	L_{CM_DC}	170mH
C_{y_AC}	8nF	C_{y_DC}	8nF
Total Weight: 90.36kg			

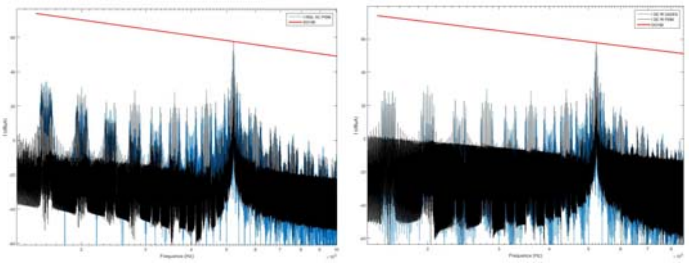

Fig. 11. AC and DC noise in comparison with the DO160F standard after optimal design of the filter

V. CONCLUSION

Design by Optimization method has been presented in the case of EMC filter design, and compared to legacy approach. This new way of design is promising, since it allows avoiding all usual assumptions, such as "capacitors are negligible compared to magnetics", or the usual CM/DM separation, which may be wrong for non-symmetrical topologies. It does also not consider any assumption for converter impedance. EMC models in the frequency domain are useful for this task, using other analytical models for taking into account other physical constraints associated with components design. All these models have been implemented in a specific framework, dedicated to optimization. This avoids many programming efforts and expertise in optimization, in order to conduct such a design method.

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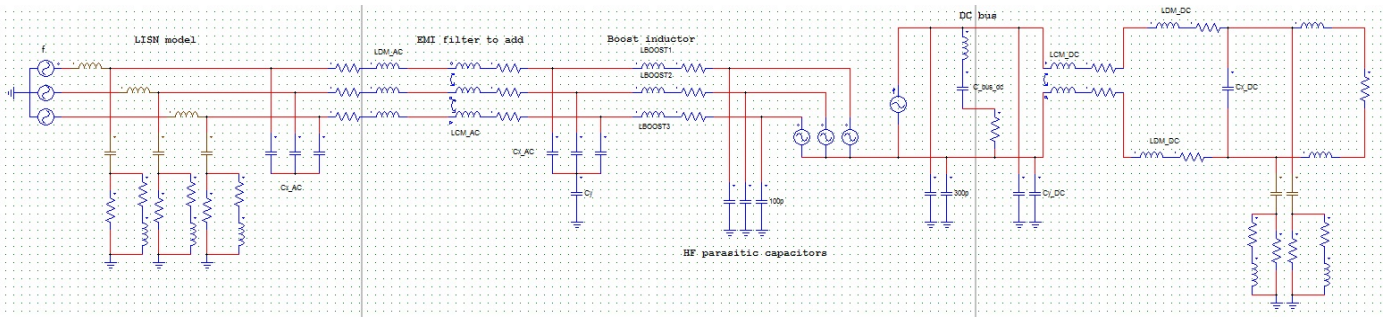

Fig. 12. Equivalent circuit of the PFC for EMC modelling