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Paper

Modular Integration of a Matrix Converter

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The future development of high-performance power electronics will rely increasingly on system-level integration, where semiconductor devices are co-packaged with other active and passive components (e.g., gate drivers, filter capacitors, and inductors) into a power module. In view of the widespread electrification of pivotal elements of the energy generation and distribution infrastructure (e.g., smart grids, electric aircraft, electric vehicles), *modularity* is also increasingly gaining importance as a means of enhancing overall system performance and reducing long-term maintenance costs. This paper focuses on the development of a highly integrated three-to-one phase matrix converter for avionic applications. It proposes an integration approach that enhances the volumetric and gravimetric power handling capability, with enhanced electromagnetic and electrothermal performance as compared to established solutions. Maintenance is also simplified by the modular assembly approach. © 2015 Institute of Electrical Engineers of Japan. Published by John Wiley & Sons, Inc.

Keywords: integrated power converter/switches, double-sided cooling, matrix converter

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1. Introduction

AC-to-AC power conversion requires switches that enable bidirectional (BD) current flow between the power source and the load and blocking the voltage irrespective of its polarity. Steady advances in semiconductor technology keep enhancing the electrothermal performance of solid-state power switches, and packaging is presently very often the limiting factor of performance and reliability. In order to overcome the limitations of standard bond-wire packaging technology, novel approaches have been proposed over the last decades based on the replacement of bond wires with solid bumps. These have enabled a dramatic improvement of the thermal and electromagnetic performance and allowed optimum space exploitation and advanced integration schemes targeting application-related switch performance optimization [1–6].

Figure 1 shows the circuit schematic of a BD matrix-converter-type switch (in the following, BD switch). In the case of insulated-gate bipolar transistors (IGBTs) being used as the active devices, a series diode is necessary to ensure reverse blocking capability (i.e., between the emitter and collector terminals). During operation, current conduction is either through the device pair T1–D1 or through T2–D2. Figure 2 shows the cross-section and the actual structure of a vertical IGBT and a vertical diode chip (in this case, latest generation 70-µm-thick vertical IGBTs and diodes, rated at 200 A/600 V) with an indication of their electrical terminals. The most effective interconnection solution between the IGBT emitter (E) and the diode anode (A) terminals is achieved by flipping, for instance, the diode upside down and contacting its top surface to the top surface of the IGBT.

The interconnection can be achieved by means of surface power bumps instead of bond wires, a technological feature already demonstrated that enables keeping the backside of each device in contact with a substrate for optimum thermal management (see [1,3,5], for example).

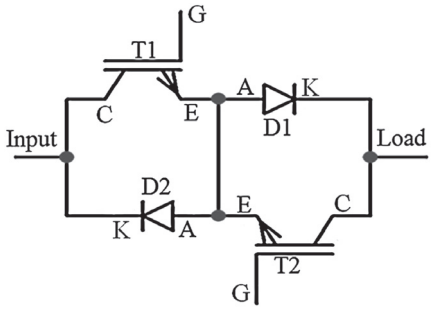

Fig. 1. Circuit schematic of a bidirectional power switch

Color Figure - Online only

2. Power Switch Integration

The mounting scheme is illustrated in Fig. 3. The upper devices are flipped upside down, and the interconnection between the two layers of chips is implemented by means of bumps soldered directly between the two device surfaces. This way, the parasitic inductance of the switch can be greatly reduced by removing bond wires and by ensuring that the flow of current through the switch is entirely vertical. Thermal management is also improved since all devices have their backside in contact with a principal cooling plane; partial heat removal also takes place via the surface, through the interconnection posts, and the stacked device. The design of the basic switch and the choice of specific technology features, such as the shape, material, and size of the bumps, for instance, rely on a *built-in reliability* design approach, consisting of extensive structural analysis (e.g., finite elements) of the electrothermal and thermomechanical stress both during the assembly process and under real operational mission profiles [5,6]. So, for instance, here the bumps are implemented by means of stacked copper–molybdenum–copper (Cu_Mo_Cu) layers to

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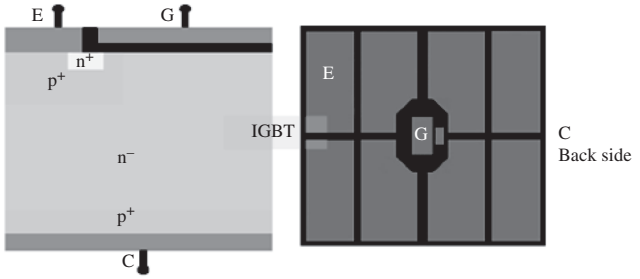
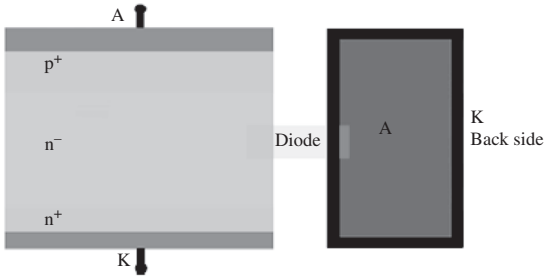


(a) Schematic cross-section and actual structure of IGBT



(b) Schematic cross-section and actual structure of DIODE

Fig. 2. 70-μm-thick vertical chips, where the top metallization is treated with AlSiCu finish to be solderable

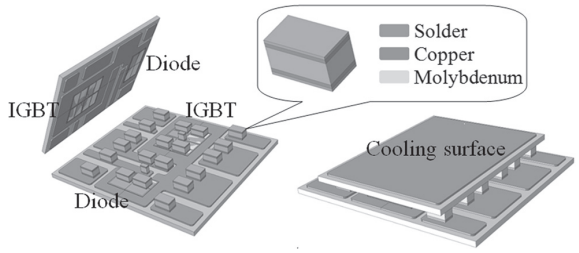


Fig. 3. Stacked assembly of substrate–chip–bump–chip–substrate for a bidirectional switch

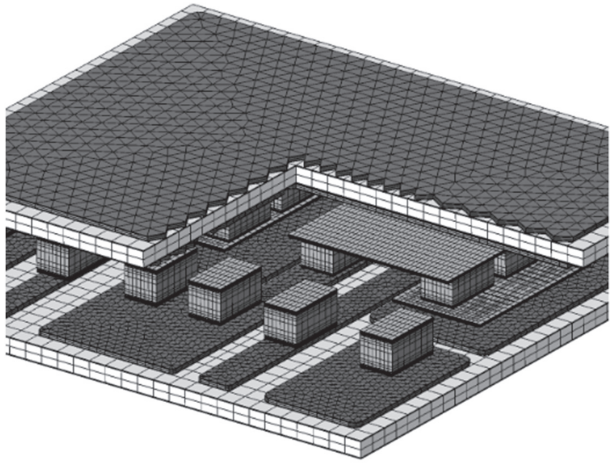


Fig. 4. Representative cut view of the meshing system to discretize the sandwich assembly

minimize the creep strain accumulation in the solder joints as compared to solid copper bumps.

The modeling and simulation were done using the commercial finite element analysis software ABAQUS 6.12-3 and its graphic user interface CAE. Figure 4 shows a cut-out view of the meshing system consisting of 156 294 elements to discretize the assembly with an AlN (aluminum nitride)-based substrate.

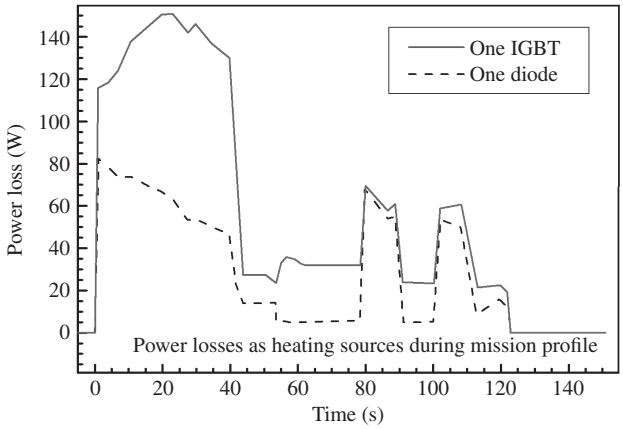


Fig. 5. Power losses of one IGBT and one diode during a mission profile derived from a real system operation

3. Thermomechanical History

The thermal and mechanical performances of the assembly using two different vertical interconnection posts (Copper_only and Cu_Mo_Cu type) were analyzed. The power loss of the IGBTs and diodes, as shown in Fig. 5, were taken as the heating source to simulate the thermal performance of the assembly during realistic mission profile, and the heat exchange boundary condition of 5000 W/m^2 K was applied to both the top and bottom cooling surfaces of the assembly. Then the temperature field obtained from the thermal simulation was used as inputs to simulate the further development of stress/strain in the assembly during the mission profile. During the first stage, all the solder joints were deactivated, and thus no strain and stress development occurred on them until solidification of the molten solder was established. In both cases (Copper_only and Cu_Mo_Cu type), the assembly was first subjected to a predefined temperature profile associated with five mission profiles, as illustrated in Fig. 6, to simulate the stress and strain development.

For the thermal and mechanical properties of the materials in the assembly, Chaboche's plastic model was used to describe the mechanical properties of the Cu and Al, and Anand's creep model was used to describe the mechanical properties of the Sn–3.5Ag solder alloy. All the mechanical and thermal properties for the Cu, Al, and Sn-3.5Ag were taken from Refs. [7,8].

4. Simulation Results

The simulation results of the temperature distribution in the assembly, Fig. 7, revealed that the highest temperature occurs at the IGBT that is attached to the top substrate at 23.01 s during mission profile with only 1.5 °C lower for the copper_only bump type. This is understandable because the power loss by the IGBT is higher than that of a diode and the cooling surface of the top substrate is smaller than that of the bottom substrate. The highest maximum temperature in the assembly is with Cu_Mo_Cu-type bumps, which is due to the molybdenum in the bumps having a lower thermal conductivity as compared to copper.

The maximum von Mises stress and creep strain accumulations are at the corners of the solder layer in contact with the emitter metallization of the IGBT, which are the most critical areas of failure. Such a result can be attributed to the mismatch of thermal expansion between the Sn–3.5Ag solder and the Si chips. Furthermore, it is also related to the joining area or the shapes and size of the bumps. This can be seen from the representative simulated results of the assembly with copper_only and Cu_Mo_Cu bumps, as shown in Figs. 8 and 9.

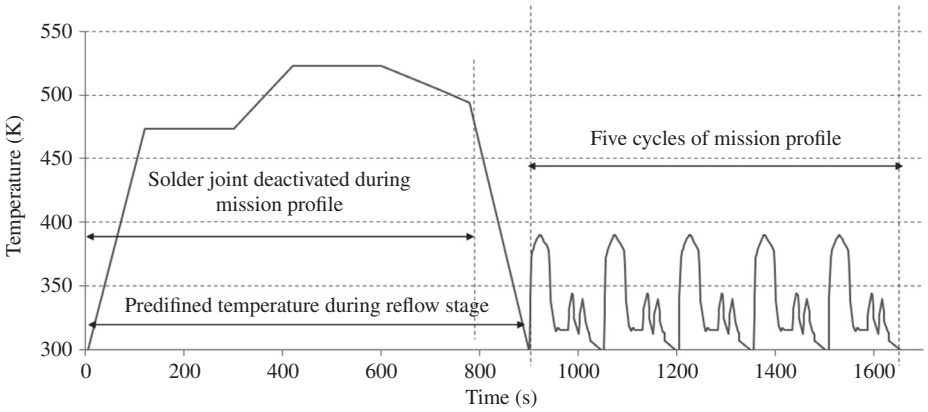
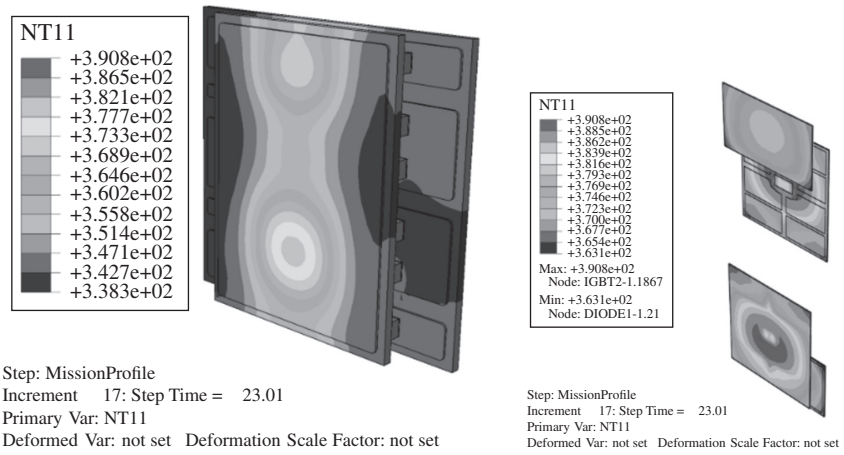
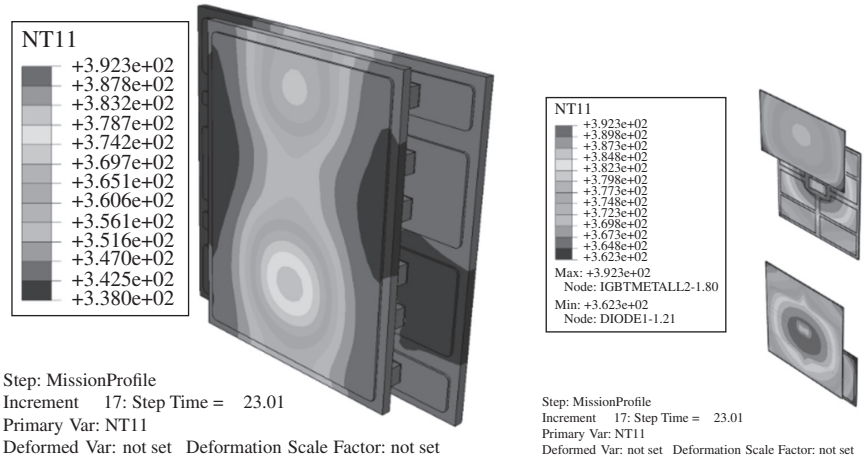


Fig. 6. Thermal history of predefined temperature of a single reflow process followed by five cycles of mission profile



(a) Copper_only bump type model



(b) Cu_Mo_Cu bump type model

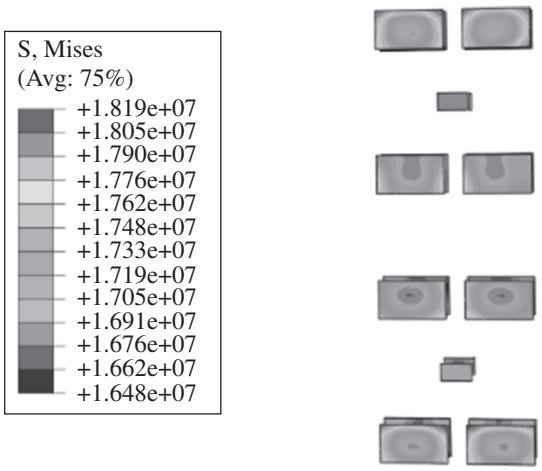
Fig. 7. Simulated temperature field at 23.01 s during one cycle of temperature mission profile

Figures 10 and 11 compare the simulated maximum residual von Mises stress and creep strain accumulation in all solder joints for copper_only and Cu_Mo_Cu-type bump assemblies. •In comparison with the bumps made of copper, the bumps constructed with molybdenum and copper can reduce the maximum residual stress and the creep strain accumulation in the solder joints.

5. Switch Prototype and Reliability Test

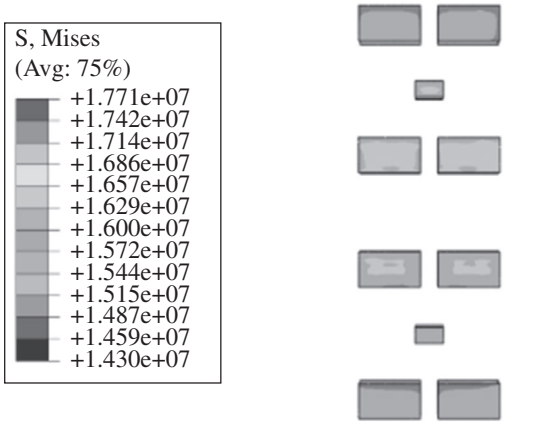
The prototype was designed and constructed with an AlN-based substrate. First, the transistor and diode chips were soldered to the underside (collector and cathode) onto a direct-bonded copper substrate with a 100-μm-thick Sn−3.5Ag preform that was employed in a fluxless reflow soldering process at a peak temperature of 260 °C for 5 min. Then the bumps were soldered onto the chips using the 62Sn36Pb2Ag solder paste reflowed at a peak temperature of 240 °C for 5 min. Finally, the two substrates shown in Fig. 12(a) were positioned one on top of the other and soldered using the 62Sn36Pd2Ag solder paste at a temperature of 260 °C for 5 min.

The switches were then assembled and gel-filled for insulation to deliver the hardware prototype parts, as shown in Fig. 12. An



Step: Mission_Profile5, fifth cycle of mission profile
Increment 112: Step Time = 151.0
Primary Var: S, Mises
Deformed Var: U Deformation Scale Factor: +1.000e+00

(a) Copper_only bump type model



Step: Mission_Profile5, fifth cycle of mission profile
Increment 100: Step Time = 151.0
Primary Var: S, Mises
Deformed Var: U Deformation Scale Factor: +1.000e+00

(b) Cu_Mo_Cu bump type model

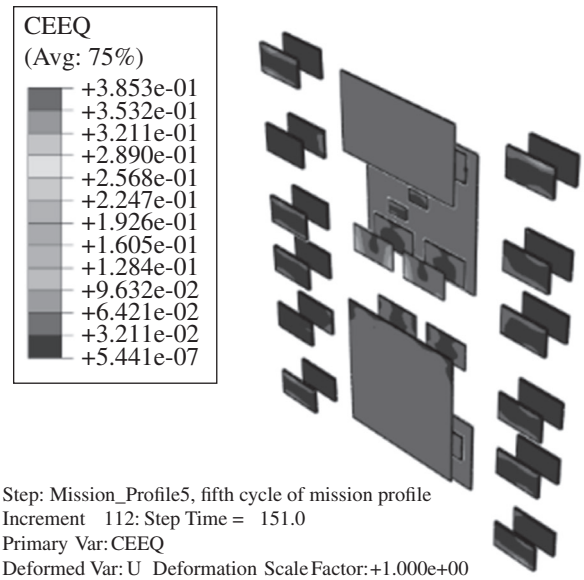
Fig. 8. Simulated distribution of von Mises stress in the solder joints after 5 cycles of the mission profile

important feature of these switches is their ability to separate the transistor driving path (gate and emitter terminals) from the power terminals.

For the switches of Fig. 12, preliminary reliability tests for technology validation, summarized in Fig. 13, delivered an initial lifetime estimate of ∼240 cycles (∼430 h), based on thermal cycling between −60 °C and 150 °C (in these tests, the variation of the IGBT on-state voltage for a fixed on-state current and temperature was used to monitor the interconnect degradation [9]). The two main factors that contribute to the rapid increase of on-state voltage in the end-of-life period are degradation of the solder layer underneath chip and bumps and peeling-off of the copper tracks from the ceramic. The number of cycles at which these effects become detrimental depends on the type and quality of the materials involved in the assembly.

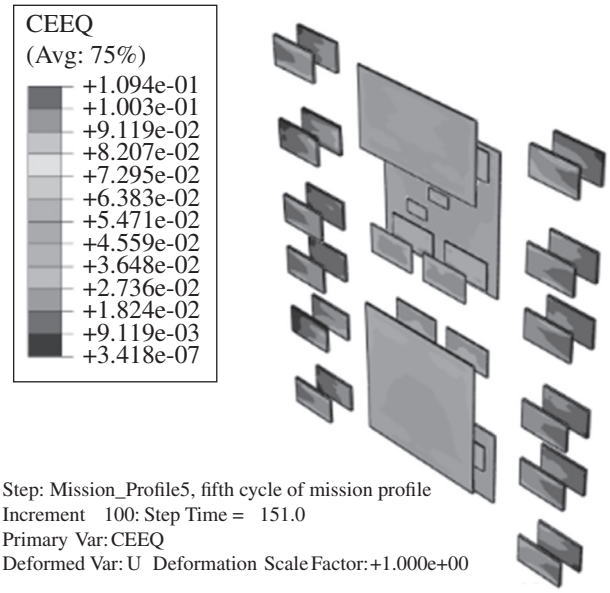
6. Power Module Integration

At least three switches as per Fig. 1 are required to build a three-to-one phase matrix converter, as shown in the circuit schematic of



Step: Mission_Profile5, fifth cycle of mission profile
Increment 112: Step Time = 151.0
Primary Var: CEEQ
Deformed Var: U Deformation Scale Factor: +1.000e+00

(a) Copper_only bump type model



Step: Mission_Profile5, fifth cycle of mission profile
Increment 100: Step Time = 151.0
Primary Var: CEEQ
Deformed Var: U Deformation Scale Factor: +1.000e+00

(b) Cu_Mo_Cu bump type model

Fig. 9. Simulated distribution of creep strain accumulation in the solder joints after 5 cycles of the mission profile

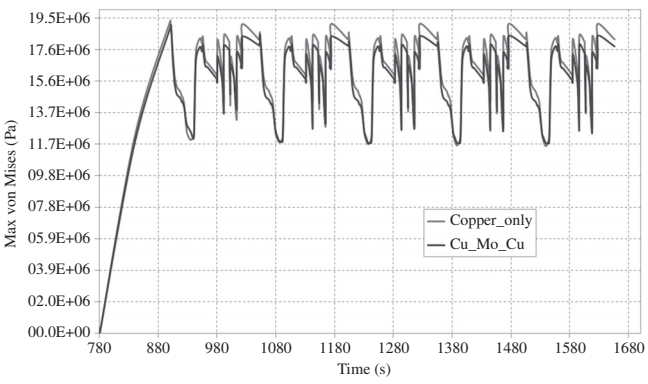


Fig. 10. Evolution of maximum von Mises stress in all solder joints through 5 cycles of mission profile

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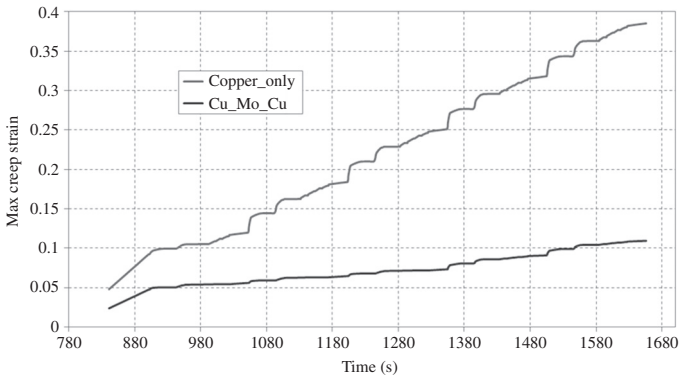
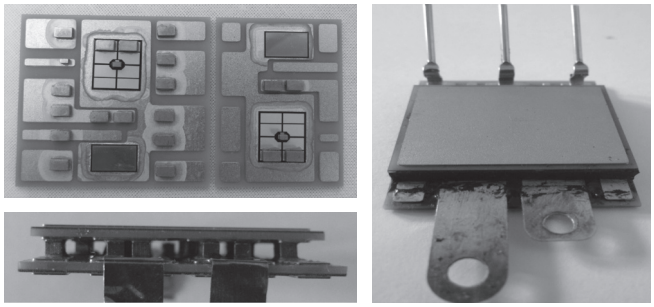


Fig. 11. Evolution of maximum creep strain in all solder joints through five cycles of mission profile



(a) (b)

Fig. 12. Bidirectional switch prototype. (a) Switch components view and side view of assembled switch. (b) Fully terminated and insulated switch

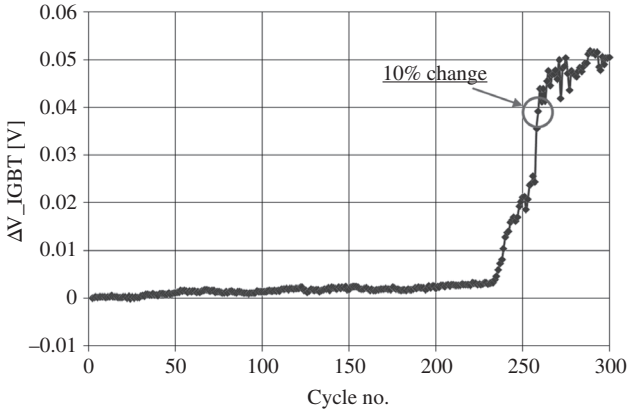


Fig. 13. Preliminary lifetime estimation results for the integrated bidirectional switches

Fig. 14. The controller is designed based on a four-step voltage-based commutation scheme, which is set to generate a constant output voltage by properly changing the required gate pattern at all times. In such a topology, current commutations take place not between the device pairs in the same BD switch but within device pairs in different phases and switches, conducting current in the same direction. So, for instance, in the case of Fig. 14, current commutations would be between the pairs T1–D1 and T3–D3, T1–D1 and T5–D5, and T3–D3 and T5–D5 during the positive half wave of the input voltage, and between the pairs T2–D2 and T4–D4, T4–D4 and T6–F6, and T2–D2 and T6–D6 during the negative half wave.

So, for minimizing the parasitic inductance associated with layout and interconnection, it is better to refer to the positive and negative cells in each BD switch: it is between such cells

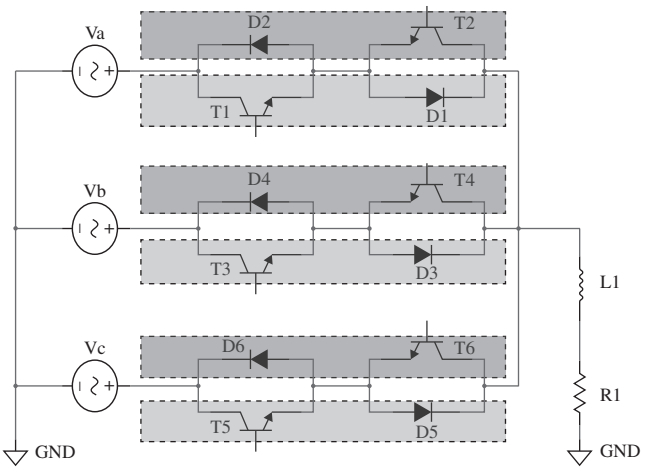


Fig. 14. Circuit schematic of a three-to-one matrix converter

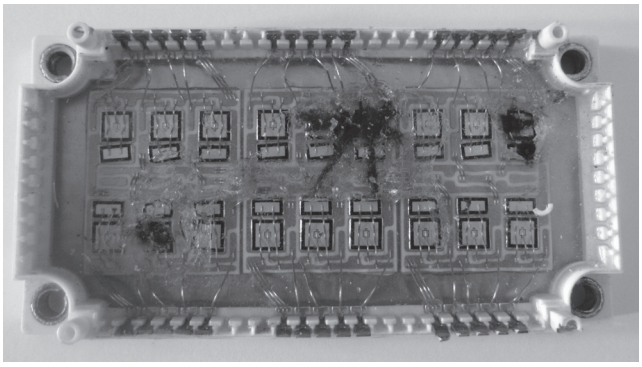
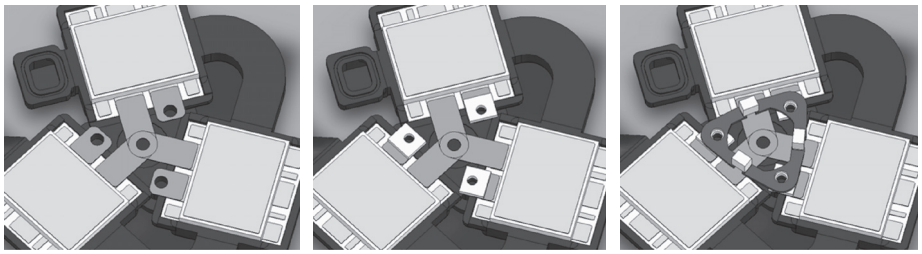


Fig. 15. Convectional wire-bonded matrix converter power module

(identified with different colors in Fig. 14) that it is important to minimize the electromagnetic path for enhanced performance in the application.

The proposed matrix-converter module integration in standard packaging technology is intrinsically limiting in the achievable system performance (e.g., maximum switching frequency) due to the well-known shortcomings of bond-wire technology and 2D layout. For instance, Fig. 15 shows the photograph of a failed integrated three-to-three phase BD power module. Current commutations, as discussed above, would necessarily imply a relatively high inductance and asymmetric loops (i.e., some switch pairs are closer to each other than the others), even with optimized external bus-bar design. Power and temperature distribution are not easy to be maintained uniform over the module during transient operation, and the unification of source drive-terminal and source power-terminal prevents very high speed transistor commutation. Moreover, as is evident from Fig. 15, failure of a single chip implies the need to replace and dispose of the whole module, with a major disproportion between the cause and effect (i.e., cost of a single chip as compared to the cost of the module) resulting in non-negligible long-term running costs of the power system. Clearly, the impact of a single chip failure is even more significant in the case of passives, gate drivers, sensors, and logic circuits when co-packaged within the same module.

To overcome such limitations and drawbacks, here an alternative module integration approach is pursued. Referring to the schematic diagram of Fig. 14, the module is constructed using three independent BD switches. The switches are enclosed within a forced-liquid-based cooler that can cool the top and bottom side of the switch. A common output terminal (load side) and three input terminals (input side) are designed to be connected only by



(a) Load interconnects (b) Gap between load and phase (c) Input filter interconnects

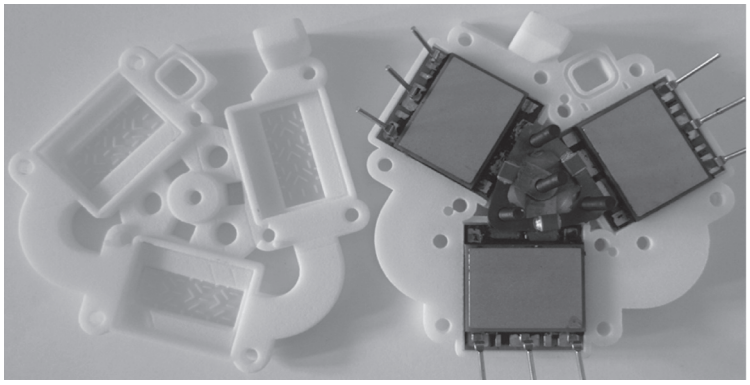


Fig. 16. Internal view of the assembly and the interconnection setup

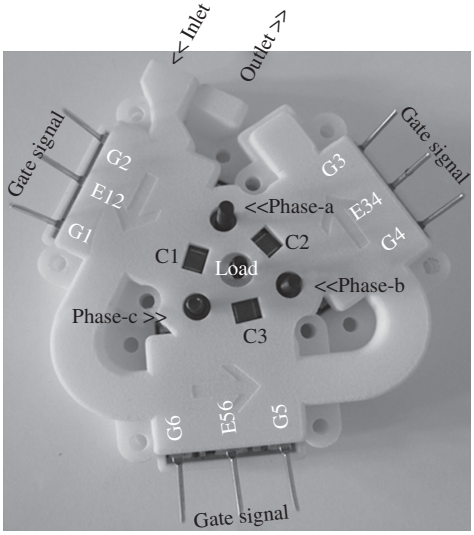


Fig. 17. Three phase-to-single phase matrix converter assembly with water cooler. G1–G6 are six IGBT gate connections and E12, E34, and E56 are common emitter connections for each bidirectional switch

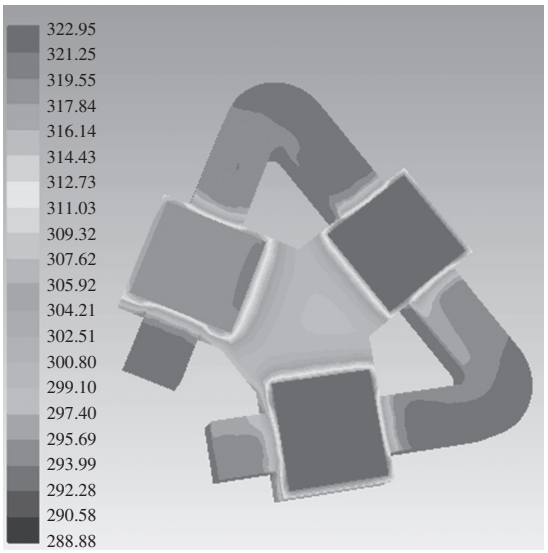


Fig. 18. Heat transfer temperature contour (in K) using ANSYS Fluent of 0.08 m/s water flow

means of bolts and screws (no soldering), as shown in Fig. 16. Three rectangular blocks of copper are placed on each phase to form a gap between the load and phases (Fig. 16(b)). As seen from Fig. 16(c), properly shaped interconnect enables enclosing phase-to-phase high-frequency filtering capacitors (here, a total of 6.6 μF ceramic capacitance is introduced between the phases; the value can be easily increased by stacking the capacitors one on top of the other. The module design is fully symmetrical, so that each switch sees identical electromagnetic and electrothermal conditions. Figure 17 shows the closed module. The power and gate signals are completely separated, and the topside of the enclosure (the cooler) can be used to mount gate drivers and additional filter and control elements to deliver a self-contained unit.

The water cooling system flow path inside the power module is designed to directly target the hot spot (light blue area shown in Fig. 16) where the power devices are located. The flow of liquid will start from the inlet and go to the top surface of each of the three switches; and once it passes the third switch, it turns down and flows via the bottom side of each switch to get to the outlet. Although this initial cooler design, with a single inlet and outlet, cannot guarantee exactly symmetrical thermal conditions for the switches, 3D simulations carried out with established industrial computational fluid dynamic design tools indicated that the temperature gradient would be low enough to make it a viable and easier solution for initial testing. In the simulations, the liquid flow rate is defined as the inlet boundary condition with initial liquid temperature set at 300 K. At the outlet, the external gauge pressure is set to zero. Thermal properties of the materials involved in the model have been assigned to evaluate the heat conduction through all solid bodies due to the fluid flow. For this simulation, a heat transfer coefficient of 5 W/m^2K was used for each wall that is exposed to the air considered as a free convection. An evenly

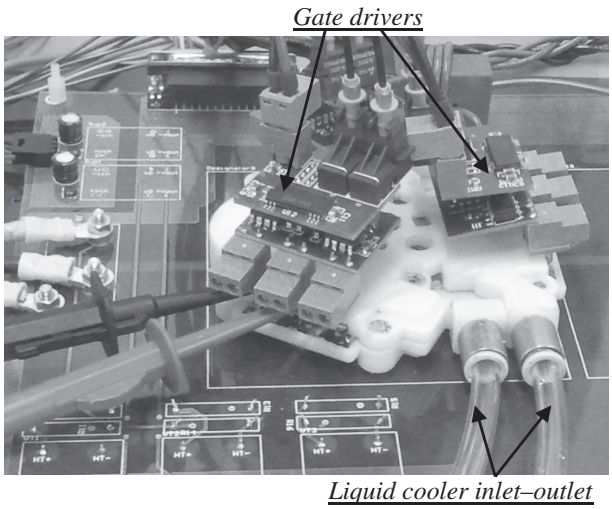


Fig. 19. Hardware and test setup for preliminary functional testing

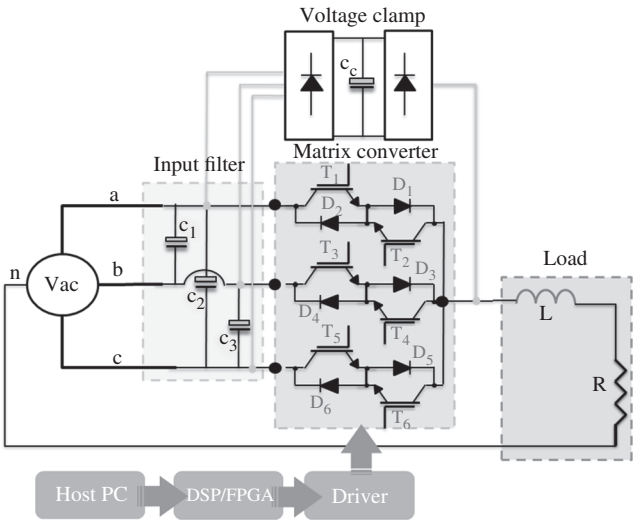


Fig. 20. Schematic of the experimental setup

distributed heat flux of 10 000 W/m^2 is used for the top surface of each of the three silicon blocks. This is a typical value used for water cooler in power electronics [10]. A velocity of 0.08 m/s (a flow rate of 0.3 l/min) is used at the inlet, while the outlet is fixed at zero pressure. This flow rate corresponds to the realistic heat transfer value between 500 and 5000 W/m^{2}K. Figure 18 shows the resulting temperature distribution. Although the cooler design is not fully symmetrical, this initial study ensured that the asymmetry is negligible under realistic operational conditions and the cooler design can easily be optimized.

7. Functional Tests

The fully assembled module was subjected to some preliminary functional tests. Figure 19 shows the assembled hardware and test setup. The corresponding schematic circuit is also shown in Fig. 20, containing the popular snubber configuration (voltage clamp) used with matrix converters where two diode bridges feed a DC regulated snubber capacitor. This clamp circuit is used to protect the BD switches from getting damaged as a result of over voltages or in the event of commutation failure. In the initial setup, a dedicated test board was built, which accommodates passives and interfaces with the control platform; also, the gate drivers were connected to the switch terminals still using additional connectors to enable more easily a thorough characterization of

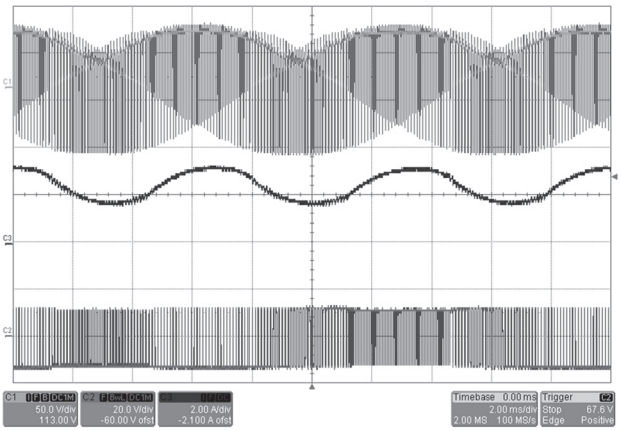


Fig. 21. Representative preliminary test waveforms for the modular matrix converter

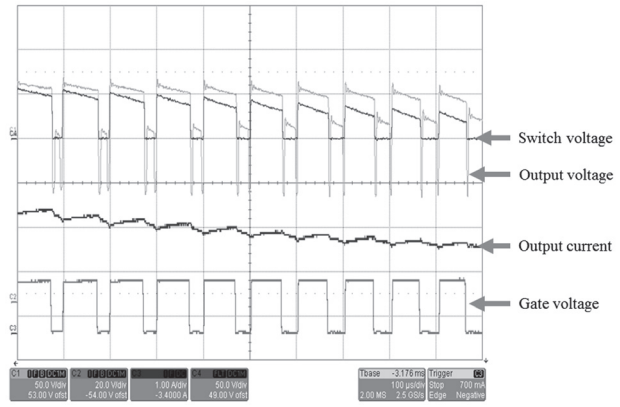


Fig. 22. Detailed view of test waveforms, including the voltage across a single bidirectional switch

the converter performance. In the final implementation, the PCBs (printed circuit boards) can be mounted directly onto the switch terminals (Fig. 17), and a number of passives can be allocated directly on the sides of the cooler for higher integration levels and a more compact overall design.

The overall open-loop control structure for three-to-one matrix converter drive is shown in Fig. 20. A four-step voltage-based commutation scheme is employed as a commutation control using a 32-bit TMS320C6713 digital signal processor (DSP) board and a general-purpose field-programmable gate array (FPGA)-based matrix converter interface card. The test conditions were very conservative to avoid unnecessary failures. The cooling liquid temperature was regulated in the range -15 to 20 $^\circ$C. Propylene glycol (which is 40% less toxic) is used for corrosion and frost protection. Figure 21 shows typical matrix converter waveforms: from bottom to top, gate-drive signals (C2, 20 V/div), load output current (C3, 2 A/div), and load output voltage (C1, 50 V/div). In these tests, the output voltage was set as DC, but a purely resistive-inductive *RL* load was used without any filter capacitors, which explains the load voltage and current waveforms. The switching frequency is 10 kHz.

Figure 22 shows a zoomed-in view of the waveforms, and also the voltage drop measured across one of the BD switches (C4). As can be seen, the switching waveform is free from overshoots of any sort, indicating a significantly contained value of the overall switch parasitic inductance. Finite-element electromagnetic analysis indicated a value of just a few nanohenries for each current conduction path in a switch at 10 kHz [11].

The wave forms in Fig. 23 show the output voltages measured while operating at different cooling liquid temperatures with

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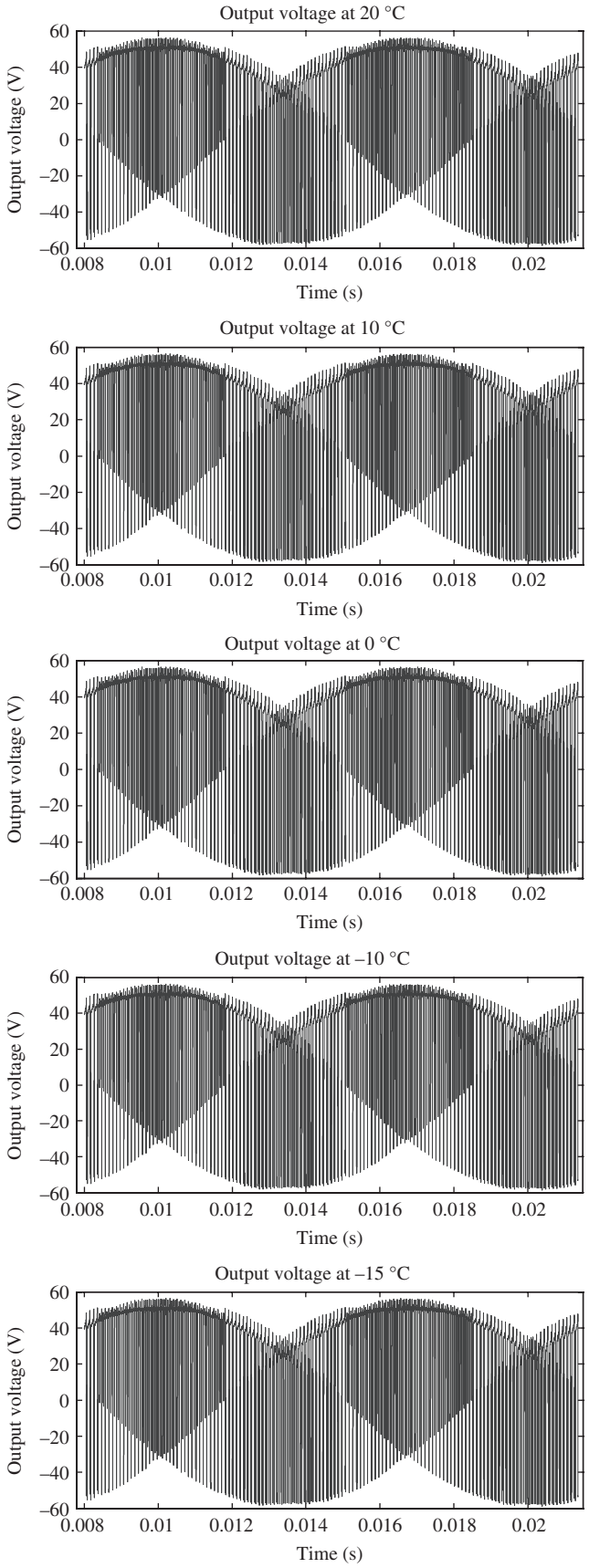

Fig. 23. View of test waveforms measured at different operating cooling fluid temperatures

Table I. Functional test conditions

	Parameter	Value
V_{in} (3φ)	Input supply voltage	50 and 100 V
f_{in}	Input line frequency	50 Hz
C_{in}	Input capacitance	6.6 uF
R_{out}	Load resistance	9.6–56.7 Ω
L_{out}	Load inductance	10 mH
V_{out} (1φ)	Output voltage	85 V
f_{out}	Output frequency	0 Hz
I_{out}	Output current	8.9–1.5 A
f_s	Switching frequency	10 KHz
Module	Volume	∼82.7 cm^3

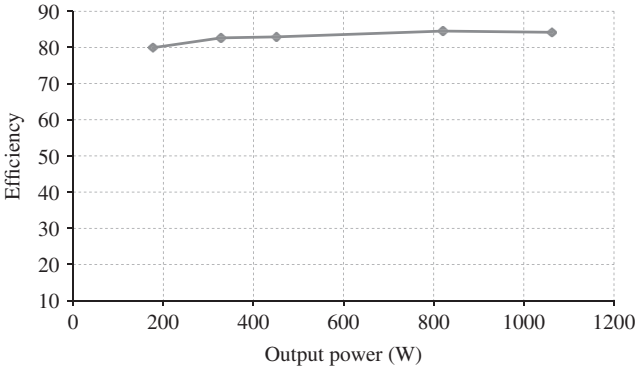

Fig. 24. Efficiency of the three-to-one matrix converter prototype against its output power

50 V/3φ input voltage. As seen from the results, the module shows no indications of failure or difference and remains active over the entire temperature range (−15 °C to +20 °C). The indication is that such module can be further implemented over a wide and harsh temperature range. The converter is also tested at 100 V/3φ input with various load resistances, as shown in Table I and Fig. 24.

Figure 24 shows the efficiency, which is the ratio between the output and input power of the converter. A power analyzer is used to detect the measurement of the three input and single output voltages and currents. The load resistance was varied, while the 3φ input voltage was fixed at 100 V. As seen from the graph in Fig. 24, the power efficiency of the converter remains >80%.

8. Conclusions

This paper presented the modular integration of a three-to-one phase matrix converter. It aims to progress beyond the state of the art in power system assembly by proposing a solution that significantly improves the electromagnetic and electrothermal performance of the semiconductor switches, as a result of both an original switch design and assembly process and system-level integration of the switches in the converter. In particular, fully bond-wire-less, double-sided cooling and layout symmetry are the key aspects of the design. The proposed approach is transferable to a number of topologies and has the additional important benefit of limiting the impact of single device/switch failure on the overall system availability. The solution can be of interest to all applications in which weight and volume reduction are highly favored, such in as aerospace, automotive, traction.

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References

(1) Mermet-Guyennet M. New structure of power integrated module, *Proceedings of the 4th International Conference on Integrated Power Systems (CIPS 2006)*, Naples, June 2006.

(2) Johnson CM, Buttay C, Rashid SJ, Udrea F, Amaratunga GAJ, Ireland P, Malhan RK. Compact double-side liquid-impingement-cooled integrated power electronic module, *Proceedings of the 19th International Symposium on Power Semiconductor Devices & ICs (ISPSD2007)*, Jeju, May 2007.

(3) Solomala P, Castellazzi A, Mermet-Guyennet M, Johnson M. New technology and tool for enhanced packaging of semiconductor power devices. *Proceedings of IEEE International Symposium on Industrial Electronics (ISIE 2009)*, Seoul, July 2009.

(4) Castellazzi A, Solomon A, Agyakwa P, Li J, Trentin A, Johnson CM. High power density, low stray inductance, double sided cooled matrix-converter type switch. *Proceedings of International Symposium on Power Electronics Conference (IPEC 2010)*, Sapporo, June 2010.

(5) Li JF, Castellazzi A, Solomon A, Johnson CM. Reliable Integration of Double-Sided Cooled Stacked Power Switches based on 70 µm Thin IGBTs and Diodes, *Proceedings of International Conference on Integrated Power Electronics Systems (CIPS2012)*, Nuremberg, March 2012.

(6) Castellazzi A, Dai T, Li JF, Solomon A, Trentin A, Wheeler P. Integrated matrix converter switch. *Proceedings of the 10th International Conference on Power Electronics and Drive Systems (PEDS2013)*, Kitakyushu, April 2013.

(7) Xingsheng L, Haque S, Guo-Quan L. Three-dimensional flip-chip on flex packaging for power electronics applications, *IEEE Transactions on Advanced Packaging* 2001; **24(1)**:1–9.

(8) Zeanh A, Dalverny O, Karama M, Woirgard E, Azzopardi S, Bouzourene A, Casutt J, Mermet-Guyennet M. Thermomechanical modelling and reliability study of an IGBT module for an aeronautical application. *Proceedings of 9th International Conference on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, EuroSimE*, Freiburg im Breisgau, 2008.

(9) Dai T, Li JF, Corfield M, Castellazzi A, Wheeler P. Real-time degradation monitoring and lifetime estimation of 3D integrated bond-wireless double-sided cooled power switch technologies. *Proceedings of 2013 15th European Conference on Power Electronics and Applications (EPE) EPE'13 ECCE Europe*, Lille, 2013.

(10) Rizvi MJ, Skuriat R, Tilford T, Bailey C, Johnson CM, Lu H. Modelling of jet-impingement cooling for power electronics. *10th International Conference on Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems, EuroSimE*, Delft, 2009.

(11) Solomon A, Castellazzi A, Trentin A. 3D integration of a three-phase bi-directional power switch. *Proceedings of the 2011-14th European Conference on Power Electronics and Applications (EPE 2011)*, Birmingham, 2011.

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