Dependence of overcurrent failure modes of IGBT modules on interconnect technologies

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Abstract

Insulated gate bipolar transistor (IGBT) modules which can fail to short circuit mode have great of applications in electricity network related fields. Single IGBT samples have been constructed with the standard Al wire bonding, flexible printed circuit board (PCB) interconnect and sandwich structure technologies. The overcurrent failure modes of the constructed IGBT samples have been tested under a range of energy levels, and the structures of the tested samples have been characterized with scanning electronic microscopy and three-dimensional X-ray computed tomography imaging. The results obtained indicate that the IGBT samples constructed with the three interconnect technologies can fail to both open circuit mode and short circuit mode. The sandwich structure IGBT sample can fail to short circuit mode under an energy level of 750 J which can meet realistic industrial applications. The networked conductive phases within the solidification structure and the Sn-3.5Ag filled in the cracks within the residual Si IGBT are responsible for forming the conducting paths in the tested samples. Both liquid phase and gas phase can be formed and the highest temperature can reach the boiling point of Si even if the sandwich structure IGBT sample is tested with short circuit failure mode.

***Keywords*:** Failure to short circuit; Failure to open circuit; Wirebond; Flexible PCB;

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Sandwich structure; Microstructure

1. Introduction

Insulated gate bipolar transistor (IGBT) modules are widely used as switching devices in various applications such as traction motor drives, renewable energy, high voltage direct current links, pulse power systems, switch mode power supplies and uninterruptable power supplies etc. In those electricity network related applications, a preference for failure to short circuit behavior in the event of device destruction which is caused by unexpected overcurrent or overvoltage fault is one of the known requirements for the IGBT modules to meet the technological development. This is because in series connected strings of the IGBT modules where a level of redundancy can be employed, the strings can still function correctly in the event of the failure occurring in a single or several redundant modules, and the failed modules can be replaced in the next scheduled maintenance. This ability is especially important for the systems which are installed very remotely, at places which are not easy to access or where the cost of unscheduled maintenance is very high [1].

Interconnect is the important part of the packaging process for achieving failure to short circuit behavior of an IGBT module. This is because the failure is in general caused by extremely rapid electric-thermal energy dissipation in the module, while both the mechanical structure and the thermal and electric conducting paths of the module during the operation heavily depend on the interconnect technology. Al wire bonded interconnect is the standard technology which has been used for many years in the conventional power modules including IGBT modules. Because of limited ability to dissipate heat and relatively high parasitic inductance which often restricts the thermal and electrical performance, several alternative interconnect technologies have been proposed and under intensive investigation for overcoming this problem [2-9]. Of them, only the press pack technology has been used for developing a couple of the IGBT modules featuring failure to short circuit behavior.

The first commercially available IGBT module which was claimed to have ability to fail to short circuit behavior was called Press-Pack IGBT and introduced by Westcode [9-11]. Another IGBT module which was reported to have ability to fail to short circuit behavior was called StakPak IGBT module and introduced by ABB [12,13]. Both IGBT modules were developed based on the press pack interconnect technology, and are complicated in mechanical structure and in manufacturing process. Also, in order to achieve uniform pressure distribution and uniform heat dissipation between the different IGBTs, all the components in the modules have to be very flat and precise which makes it very expensive to manufacture.

The present work is concerned with overcurrent failure modes of the IGBT modules constructed with three relatively simple interconnect technologies, including the standard Al wire bonding, flexible printed circuit board (PCB) and sandwich structure technologies [8,14-17]. The main aim is to investigate and find relatively simple and cost effective solution for design and manufacturing of the IGBT modules which feature failure to short circuit behavior. The specific objectives of this paper are: (i) to test the failure behaviors of the IGBT modules constructed with the three interconnect technologies; (ii) to demonstrate the ability of featuring failure to short circuit behavior for the sandwich structure IGBT module under realistic energy levels in the event of IGBT destruction; (iii) to characterize the microstructures of the tested IGBT modules with both failure to open circuit behavior and failure to short circuit behavior; and (iv) to provide insight into the phase changes of the component materials in the IGBT modules during the overcurrent testing.

2. Materials and methods

2.1 Materials and sample preparation

Instead of destroying the whole IGBT modules having complex structures, the samples of single IGBT modules have been constructed with the three interconnect technologies for

the overcurrent testing. For all the samples, the substrate used is commercially available AlN-based direct bonded copper (DBC) substrate, which had two Cu islands on one side and one single Cu plate on the other side of the AlN ceramic tile. The thickness of the AlN ceramic tile was 1 mm, and those of Cu islands and Cu plate on both sides were 0.3 mm.

2.1.1 Al wire bonded samples

For preparing the samples with the Al wire bonding technology, the 13.5 mm × 13.5 mm × 0.3 mm 1700V/50A Si IGBTs with central gate were obtained from Dynex Semiconductor Ltd (Lincoln, UK). They have ~0.1/1/1 μm thick Ti/Ni/Ag metallization on the collector or the back side and ~5 μm thick Al metallization on both the emitter and gate of i.e. the top side. During the assembling process, 100 μm thick eutectic Sn-3.5Ag solder paste was first applied with stencil printing on each of the AlN-based DBC substrates. Then the Si IGBT die was placed on the printed solder paste, and the solder was reflowed in air at a peak temperature of 260 °C for 5 minutes. After this, the surface oxide of the DBC substrate was removed by applying a flux at 60 °C for one minute followed by rinsing with de-ionized water. Finally, 99.999% pure 375 μm diameter Al wire was bonded on both the top side of the IGBT and the DBC substrate using an ultrasonic bonding machine for achieving the necessary interconnection. Fig. 1 shows the photograph of one as-prepared IGBT sample constructed with the Al wire bonding technology.

2.1.2 Flexible PCB interconnected samples

For preparing the samples with the flexible PCB based interconnect technology, the 13.5 mm × 13.5 mm × 0.5 mm 2500V/50A Si IGBTs with corner gate were obtained also from Dynex Semiconductor Ltd (Lincoln, UK). They have ~0.1/1/1 μm thick Ti/Ni/Ag metallization on the collector or the back side and ~5 μm thick Al metallization on the gate, and ~5/0.1/1/1 μm thick Al/Ti/Ni/Ag metallization on the emitter of the top side. The flexible PCB was custom manufactured from Stevenage Circuits Ltd (Stevenage, UK). It consisted of

100 μm thick polyimide sandwiched by 100 μm thick Cu tracks on both sides. There were ϕ1.2 mm and ϕ1.6 mm through vias which connect the top and bottom side Cu tracks, and ~4/0.1 μm thick NiP/Au finish on the surfaces of the Cu tracks. Sintering of Ag nanoparticle was used for both the IGBT die attachment and bonding the flexible PCB to emitter side, and paste of the Ag nanoparticles was obtained from Cookson Electronics (South Plainfield, NJ 07080, USA).

During the assembling process, one piece of the flexible PCB was first placed and fixed on a piece of 25 μm thick Ag foil with the same size. This was to blind vias on one side of the flexible PCB and improve the bonding of the sinterd Ag layer to the side walls of the vias. Then 100 μm thick paste of Ag nanoparticles was applied on the top and filled into the through vias of the flexible PCB by using stencil printing, and dried at 130 °C for 30 min. At the same time, a layer of 100 μm thick paste of Ag nanoparticles was also printed on the the DBC substrate, and dried 130 °C for 30 min. Following this, one Si IGBT were placed on the dried paste on the substrate, and then the flexible PCB with dried paste was aligned and put on the top side of the IGBT at one end and on another pad of the dried paste on the DBC substrate at the other end. A dummy Si die with the same thickness as the IGBT was also placed on top of the 25 μm thick Ag foil on the flexible PCB at the end without the IGBT. This dummy Si die was used to mechanically compsensate the height of the flexible PCB, but not bonded to the Ag foil with any joining material. All the components were further fixed with kapton tape, and the sintering was carried out with a house made sintering press at a temperature of 250 °C and a pressure of 5 MPa for 5 minutes. After the sintering, a 99.999% pure 375 um diameter Al wire was bonded on the corner gate of the IGBT for finalizing the sample preparation. Figs. 2 and 3 give the cross-sectional schematic and photograph of one as-prepared flexible PCB interconnected IGBT sample for the overcurrent testing. The dummy Si is not shown in Figs. 2 and 3 because it was easily removed after the sintering

process.

2.1.3 Sandwich structure samples

Mechanical constraint was added to the flexible PCB interconnected IGBT sample to form the sandwich structure sample. This was achieved by placing a top DBC substrate similar to but slightly larger than the flexible PCB, and soldering two small pieces of DBC substrates between the top and bottom DBC substrates with eutectic Sn-3.5Ag solder paste to form the mechanical support and constraint. During the soldering process, a compressive force of ~100 N was applied on the top DBC substrate with the house made press, and the solder was reflowed in air at a peak temperature of 260 °C for 5 minutes. Fig. 4 shows the cross-sectional schematic of the sandwich structure IGBT sample.

2.2 Overcurrent testing

2.2.1 Testing procedure

The overcurrent testing was carried out with a test rig schematically shown in Fig. 5. A 0 to 600V XDC600-20 digital DC power supply made by Xantrax (Burnaby, BC, Canada) was connected to a capacitor bank which contained 9 Nippon (Tokyo, Japan) 6800 uF 400 V aluminium electrolyte capacitors connected in parallel. An anti-parallel diode was connected across it as a free wheel diode. The positive terminal of the capacitor bank was connected to the collector terminal while the negative terminal of the capacitor bank was connected to the emitter terminal of the IGBT sample.

During the testing, the capacitor bank was pre-charged to a specified energy level by adjusting the voltage output of the power supply. The overcurrent was triggered by using a gate drive to turn on the IGBT. After turned on, the IGBT went into the saturation region, where the collector current reached its maximum value and stayed there until the IGBT's junction temperature exceeded its intrinsic or thermal limits after which the device braked down followed by a sudden influx of current from the capacitor bank. The current through

and the voltage across the IGBT were recorded on the Tektronix DPO 7017 digital phosphor oscilloscope (Beaverton, OR, USA) by using a Rogowski coil manufactured by Power Electronic Measurements Ltd. (Nottingham, UK) and a Yokogawa (Taiwan, China) model 701926 high voltage differential probe respectively. The recorded residual voltage across the IGBT was used to judge whether the overcurrent testing of the IGBT resulted in open circuit failure mode (OCFM) or short circuit failure mode (SCFM).

It should be noted that the discharge profile during the testing was not controlled, and this was to mimic the failure of an IGBT in the real industrial scenario. This is because in reality, the discharge does not follow any profile rather than the natural discharge profile defined by the parasitic inductance, capacitance and resistance of discharge path. The IGBT was turned on by applying +18 V to the gate terminal without any intentions to turn off the device or to modulate the discharge profile. This turn-on induced classic Type-II failure into the device (a failure which happens when the device is turned-on into an existing short circuit in the circuit).

2.2.2 Estimation of realistic energy level in the event of IGBT destruction

In a typical real industrial application, e.g. a voltage source dc to dc converter, the energy from the mains is stored locally in the capacitor bank known as a filter or line capacitor before delivering it to the IGBT. The value of this capacitor depends upon the application and can be in range starting from micron Farad to Farads. For an converter, operating at 1300 V having a DC link capacitor of 24 mF, the total energy stored in the system would be $E = \frac{1}{2}CV^2 = 20.3kJ$. This is considered to be realistic amount of energy that the IGBT power module will face in real industrial applications. If this amount of energy gets dissipated in IGBT power module, it can cause explosion of the module with ejection of shrapnel [18]. If an IGBT power module is of 1500 A containing 30 IGBT dies (50 A each) connected in parallel this implies that there would be about 680 Joules of energy per device if

the module fails uniformly. Hence for the present samples which all contain only one IGBT, the stored energy of about 750 J which is slightly higher than 680 J have been taken as a benchmark for the overcurrent testing.

2.3 Structure characterization

After the overcurrent testing, the failed samples constructed with the standard Al wire bonding technology and the flexible PCB interconnect technology were observed and analyzed using a Hitachi TM300 desktop scanning electronic microscope (SEM) and Quantax 70 energy-dispersive X-ray spectroscopy (EDXS) microanalysis system. Depending on the different samples, the morphologies and elemental compositions on the surfaces of the IGBTs and/or the microstructures and elemental compositions on the polished cross sections were observed and analyzed. For preparing the polished cross sections, the tested samples were first cut using a diamond saw, and then they were mounted within an epoxy resin which was later grinded and polished using first 600 grit size SiC paper down to 1 μm diamond suspension.

The sandwich structure IGBT samples tested with both SCFM and OCFM were characterized using three-dimensional (3D) computed tomography (CT) imaging, carried out on an Xradia Versa XRM-500 system. This was to accurately calculate the volumes of the failure site, in particular, the amounts of the material that was removed due to melting and/or vaporization during the overcurrent testing. The volumes were calculated using imaging analysis method with the publically available software ImageJ. The calculated results will be used to provide insight into the phase change of the component materials and estimate the possible highest temperature.

3. Results

3.1 Overcurrent testing

3.1.1 Al wire bonded samples

Under the energy level of benchmark, 750 J, pre-charged to the capacitor bank, the tested sample resulted in part evaporation and blow-out of all the Al wire bonds carrying the current. The OCFM due to such loss of all the Al wire bonds was observed when the energy level was reduced to 500, 250 and 125 J. All the Al wire bonds were remained on the top of the tested IGBT, and SCFM was achieved when the energy level was further reduced to 62.5 J.

Figure 6 presents representative waveforms of the recorded current through and the voltage across the IGBTs during the testing. A residual voltage of ~ 40 V can be seen for the sample which failed to OCFM at the energy level of 500 J, while a residual voltage of nearly zero can be seen from the sample which failed to SCFM at the energy level of 62.5 J. Table 1 summarizes the peak current, current saturation time and failure mode from all the tested samples. For the Al wire bonded samples which resulted in OCFM under the testing energy level of 750 down to 125 J, the peak current of 6000 A down to 600 A reached within the saturation time of 1 mS to 7.5 mS. For the Al wire bonded sample which achieved SCFM under the testing energy level of 62.5 J, the peak current of 1100 A reached within the saturation time of 3.8 mS.

3.1.2 Flexible PCB interconnected samples

The first sample was tested at 500 J and resulted in an OCFM. The second sample was tested at 250 J, and resulted in SCFM. Then another two samples were tested at 375 J and 312.5 J. The one tested at 375 J was noted to have OCFM, while the one tested at 312.5 J achieved SCFM. Therefore, the energy required to achieve SCFM should be between 312.5 J and 375 J.

The peak current, current saturation time and failure mode from all the tested flexible PCB interconnected samples are also listed in Table 2. It can be seen that under a similar testing energy level and peak current, the saturation time for the flexible PCB interconnected sample was clearly longer than that for the Al wire bonded sample. This can readily be

attributed to the larger contact/conducting area in the flexible PCB interconnected sample which would have lower resistance and larger volume of the material for heat dissipation. As a result, a longer time was needed for the IGBT's junction temperature exceeded its intrinsic or thermal limits no matter whether it resulted in OCFM or SCFM.

3.1.3 Sandwich structure samples

Under the energy level of benchmark, 750 J, pre-charged to the capacitor bank, the tested sandwich structure sample was observed to achieve SCFM. Then the sample was tested under double of that energy, i.e. 1500 J, and it was noted that the sample acquired OCFM as the integrity of the structure was lost. Figure 7 presents the waveforms of the recorded current through and the voltage across the IGBTs of the two tested samples during the testing. A residual voltage of ~ 40 V and nearly zero for the samples which failed to OCFM and SCFM are similar to those shown in Fig. 6 for the Al wire bonded samples. This reveals that under the resolution of the test rig, the residual voltages across the IGBTs which were used to judge OCFM and SCFM were independent of the interconnect technologies though much different energy levels could have been used.

In addition, it should be pointed out that for the majority of the test groups listed in Table 1, only one sample had been tested. However, for the Al wire bonded samples, two samples have been tested with SCFM under an energy level of 62.5 J. For the sandwich structure samples, three samples had been tested with SCFM under 750 J and two samples had been tested with OCFM under 1500 J. Therefore, in comparison with the Al wire bonded samples and flexible PCB interconnected samples, the sandwich structure samples would indeed improve the energy level to achieve SCFM.

3.2 Structure characterization

3.2.1 Al wire bonded samples

Figure 8 shows the photographs of two representative tested samples failed to OCFM

and SCFM. It can be seen that all the Al wire bonds carrying the testing current had gone in sample which went to OCFM. Material removing of the Si IGBT also occurred on almost the entire surface of the tested vehicle, part of which was covering with solidification product, and part of which was covered with Sn-3.5Ag solder residual or even Cu residual on the DBC substrate. By contrast, all the Al wire bonds are still remained on top side of the IGBT in sample which went to SCFM. On the local region very close to the Al wire bonds, there was material removing and the surface of the IGBT was covered with solidification product. On the majority of the surface of the IGBT, the Si and the Al metallization on the Si were still intact.

Figure 9 presents the representative SEM images taken from the cross sections of the tested Al wire bonded samples with OCFM and SCFM. From the tested samples with OCFM, the solidification product surrounded by intact Si can be seen to occupy part space of the original Si and in contact with the Sn-3.5Ag solder residual under the original Si. EDXS analysis revealed that the white phases were less than the black phase of Si in the solidification product, and they mainly consisted of Sn plus minor Al and Cu. As shown in Fig. 9 (b), the dendritic structure which resulted from the rapid and unstable solidification of the mixture of the molten Si-Sn alloy with mixed Al and Cu had been produced and occupied part space of the original Si after the overcurrent testing. Sn-3.5Ag solder filled in the cracks in within the Si can also be seen, which probably came from the injection of the molten Sn-3.5Ag solder into the cracks caused by the explosion due to rapid solid-gas phase transformation during the overcurrent testing.

From the tested sample with SCFM, the Al wire bond was partially connected to the original Si and partially connected to the solidification product which was extending to the Si-3.5Ag solder under the Si IGBT or the Cu of the DBC substrate. The scale of the solidification structure also in the form of dendritic structure was finer and smaller than those

observed in the tested samples with OCFM. EDX analysis reveals that the white phases were further less than the black phase of Si in the solidification product, and they consisted of more or less similar amount of Sn and Al. There were also some cracks observed within the original Si, and some of them were filled in with Sn-3.5Ag solder. A crater of ~0.5 mm in size was further observed under the residual wire bond, occupying the space of the original Si and Sn-3.5Ag solder there.

In addition, as pointed at by the arrows in Fig. 9 (a) and (c), it was the networked white phases consisting of Sn, Al and Cu, and the Sn-3.5Ag solder alloy filled in the cracks within the residual Si IGBT that formed the conductive channels in the spaces of the original Si IGBTs, and this will be further discussed below.

3.2.2 Flexible PCB interconnected samples

Figure 10 gives the photographs of two flexible PCB interconnected samples tested with OCFM and SCFM. In the sample tested with OCFM, most of the flexible PCB on the top of the IGBT had been blown off, and the bonding between the flexible PCB and the IGBT had been lost. In the sample tested with SCFM, only small part of the flexible PCB on the top of the IGBT had been blown off, and the bonding between the flexible PCB and the IGBT was still there.

Figures 11 and 12 present representative SEM images taken from the as-tested surfaces and the polished cross sections of the two samples shown in Fig. 10. It can be seen that crates with a depth of half to the entire thickness of the original Si IGBT were formed on the surfaces of both tested samples. The whole surfaces especially the walls of the craters in both samples were covered with a layer of solidification structure consisting of a mixture of black phase and white phase. Through careful observation, a primary phase consisting of black phase only and the coexisting eutectic structures consisting of both black phase and white phase could be identified, and hence the solidification structure was actually a hypo-eutectic

structure. EDXS analysis revealed that the black phase was Si, and the white phase consisted of Ag plus minor Cu and Al. Between the two samples, the one tested with OCFM under higher energy level contained higher percentage the white phase than the other sample tested with SCFM under lower energy level. In the sample tested with SCFM, the flexible PCB had reasonable bonding to the residual surface of the Si IGBT.

3.2.3 Sandwich structure samples

Figure 13 shows the photographs of the two sandwich structure samples after the overcurrent testing. It can be seen that the damage of the sample tested with OCFM under 1500 J was very catastrophic, and the sandwich structure had been disintegrated. By contrast, the top DBC was still fixed well in the sample tested with SCFM under 750 J.

From the reconstructed 3D X-ray CT images, ten relatively small crates were visible in the sandwich sample tested with OCFM, and only one relatively large crater was observed in the sandwich sample tested with SCFM. Fig. 14 presents one cross-sectional view of the 3D X-ray CT images for both samples. For the sample tested with OCFM under energy level of 1500 J, the craters had been through the entire thickness of Si IGBT, but just part of the top Cu track of the bottom DBC substrate. The sizes of the craters within the Si IGBT were approximately 0.5 mm to 4.0 mm, while those within the top Cu track of the bottom DBC substrate were reduced approximately to 0.25 mm to 2 mm in the plane direction. From the reconstructed 3D images, the total volume of all the craters within the Si IGBT was calculated to be 13.6 mm^3 and that within the Cu track to be 1.8 mm^3. The latter volume also included the removed sintered Ag joint between the original IGBT and the original Cu track. Furthermore, the top layer of the IGBT with a thickness approximately of 0.14 mm, equivalent to a volume of 25.1 mm^3 was also removed during the overcurrent testing. Therefore, it can be said that a total volume of 38.7 mm^3 from the Si IGBT had gone.

For the sample tested with SCFM under energy level of 750 J, the crater had been through thicknesses of both the Si IGBT and the top Cu track of the bottom DBC substrate. The average size of the crater within the Si IGBT was approximately 7.5 mm, while its average size within the top Cu track of the bottom DBC substrate was reduced approximately to 3 mm in the plane direction. From the reconstructed 3D images, the volume of the crater within the Si IGBT was calculated to be 24.0 mm^3 and that within the Cu track to be 4.4 mm^3. The latter volume also included the removed sintered Ag joint between the original IGBT and the original Cu track.

In addition, it should be pointed out that in the as-prepared sandwich structure samples, the conductive paths were exactly the same as those in the as-prepared flexible PCB interconnected samples. Therefore, after the overcurrent testing, a layer of solidification structure consisting of a mixture of Si and Ag, Cu and Al should also cover the surfaces and the walls of the craters formed in the sandwich structure samples.

4. Discussion

4.1 Dependence of failure modes on interconnect technologies

Under sufficient low energy level, SCFM can be achieved from the IGBT samples constructed with all the three investigated interconnect technologies. With increase in the energy level, SCFM would be changed to OCFM from the IGBT sample at a certain energy level depending on the used interconnect technology. The maximum energy levels for the three interconnect technologies to avoid OCFM are in the ascending order: Al wire bonding < flexible PCB interconnect < sandwich structure. The increase in this maximum energy level can be related to increase in the contact/conducting area, thermal mass and mechanical constraint in the interconnect technology. An energy level of 750 J which could meet realistic industrial applications had been achieved by using the sandwich structure IGBT sample

ensuring SCFM. In comparison with the press pack interconnect technology which was used to develop the IGBT modules to have ability to fail to SCFM, the present result can provide a simpler and more cost-effective solution for those applications.

Rapid solidification structure had been observed in all the tested samples, which verifies the formation of liquid during the overcurrent testing. Electrical arc and explosion were always observed during testing all the samples despite to different degrees. The existence of the explosion reveals that a certain amount of high temperature gas must also have been produced. As shown in Fig. 9 (b), the crater under the residual Al wire bond observed in the Al bonded sample tested with SCFM indicated that the hottest region and the most serious damage occurred close to the Al wire bond, but under the surface of the Si IGBT. Therefore, Al wire bonds could at least partially avoid the contact and attack by the formed liquid and gas. This is probably the main reason why the Al wire bonds were still on the surface of the IGBT tested with SCFM under low energy level. Under higher energy levels, the volumes of the formed liquid and gas were larger enough to be in touch with the Al wire bonds, or the explosion caused by the high temperature gas was strong enough to break down the Al wire bonds. This can be used to explain why all the Al wire bonds had gone and the samples failed to OCFM.

The saturation time for the Al wire bonded samples tested with SCFM under an energy level of 62.5 J was shorter than those for the samples tested with OCFM under energy levels of 250 J and 125 J. The reason why this occurred needs further investigation. One possibility may be related to the depth of the thermal overload breakdowns within the IGBT during the overcurrent testing. As mentioned previously, if the tested samples resulted in SCFM, the Al wire bonds stayed in-contact. It is thus reasonable to think that more energy could be dissipated in the IGBTs causing it to fail. By contrast, if the tested samples resulted in OCFM, the interconnect of the Al wire bonds broke down and thus more energy could be dissipated in

the electric arc formed during the testing rather than in the IGBTs. Therefore, during the initial stage of the overcurrent injection, the energy was probably dissipated in relatively deep regions of the IGBTs when the samples were tested under 62.5 J, while in the surface regions of the IGBTs close to the Al wire bonds when the samples were tested under higher energy levels. In this case, a little longer saturation time might be needed for the samples tested under 250 J and 125 J than the samples tested under 62.5 J to reach the juncture temperature limit. Another possibility may be associated with rates of temperature rise during the overcurrent testing. Generally speaking, a higher energy level would lead to a higher rate of the temperature rise, which would probably result in a higher juncture temperature limit. With appropriate combination of the rate of temperature rise and juncture temperature limit, it is possible for the samples tested under a lower energy level to have a saturation time longer than the samples tested under somewhat higher energy levels.

For the flexible PCB interconnected and sandwich structure samples, more energy is needed for the IGBT's juncture temperature exceeds its thermal limit because of the increase in contact/conducting area. On the other hand, the probability for the flexible PCB to partially be bonded to the surface of the tested IGBT would be increased because of the increased contact area between the flexible PCB and the IGBT, and/or the additional mechanical constraints. This is probably the reason why they improved the maximum energy for the IGBT sample to achieve SCFM and avoid OCFM.

4.2 Conducting paths in the samples after the overcurrent testing

Under high energy levels, the interconnect materials such as the Al wires and flexible PCB had gone after the overcurrent testing. It is hence obvious that the IGBT samples had OCFM because of loss of the continuity of the conducting paths. Under low energy levels when the IGBT samples tested with SCFM, the rapid solidification alloys covering the surfaces and walls of the formed craters and the Sn-3.5Ag filled in the cracks within the

residual Si IGBT were the electrical connections existing between the residual interconnect materials and the residual Sn-3.5Ag solder joints.

In the rapid solidification alloys, the dendritic structure was observed in the Al wire bonded samples and the hypo-eutectic alloy of Si-Ag, Al and Cu was observed in the flexible PCB interconnected samples. The black phase Si existing in all these samples has low electrical conductivity, and the networked white phases consisting of Sn, Ag, Al and/or Cu have high electrical conductivity. Therefore, it was the networked white phases and the the Sn-3.5Ag filled in the cracks within the residual Si IGBT which formed the conductive channels to connect the residual Al wire bonds or flexible PCB and the residual Sn-3.5Ag solder joints together for forming the continuous conducting paths in those samples tested with SCFM.

4.3 Phase changes occurring during the overcurrent testing

From Fig. 7, it can be seen that the durations of the current pulse which passed through the IGBTs tested with SCFM under 750 J and OCFM under 1500 J were approximately 44 mS and 7 mS, respectively. This implies that all the energy had been dissipated in 44 mS and 7 mS. Assuming that all the energy had been dissipated in the Si IGBT, the heat zone distance can be estimated by using the following Eq. (1) [19]:

$$X = \sqrt{\frac{K_{Si}t}{\rho_{Si}C_{Si}}} \tag{1}$$

Where X is heat zone size, t is time, and K_{Si} is thermal conductivity, ρ_{Si} is density and C_{Si} is specific heat capacity of Si.

With the properties of Si, the heat zone sizes X=1.8 mm and X=0.7 mm can be obtained from Eq. (1) for the durations of 44 mS and 7 mS. Because of such heat zone sizes and the durations of the current pulse, most of the energy can be assumed to dissipate in the heat zones causing temperature rise in Si and closely nearby materials. For the purpose of simplification, the energy can be further assumed to be consumed for heating, melting and

vaporizing the 4.4 mm^3 Cu and 24.0 mm^3 Si which initially occupied the space of the formed crater in the sample tested with SCFM, or heating, melting and vaporizing the 1.8 mm^3 Cu and 38.7 mm^3 Si which were removed in the sample tested with OCFM. Then the energy Q_b needed to heat the Cu or Si up to their boiling point can be calculated with the following Eq. (2):

$$Q_b = mC(T_m - T_r) + m\Delta H_m + mC(T_b - T_m) \quad (2)$$

Where m is mass, C is specific heat capacity, T_r is room temperature, T_m is melting point, T_b is boiling point and ΔH_m is latent heat of fusion. The energy Q_g required for the Cu or Si to further become gas phase can be calculated with the following Eq. (3):

$$Q_g = Q_b + m\Delta H_b \quad (3)$$

While ΔH_b is latent heat of vaporization. With the thermal and physical properties listed in Table 2 [20-22], the energy Q_b needed to heat 4.4 mm^3 Cu and 24.0 mm^3 Si to their boiling points are respectively 47.2 J and 243.6 J, and the energy Q_g required for the 4.4 mm^3 Cu and 24.0 mm^3 Si to further become gas phase are respectively 236.2 J and 958.6 J. By contrast, the energy Q_b needed to heat 1.8 mm^3 Cu and 38.7 mm^3 Si to their boiling points are respectively 19.3 J and 392.8 J, and the energy required to Q_g required for the 1.8 mm^3 Cu and 38.7 mm^3 Si to further become gas phase are respectively 96.6 J and 1545.7 J.

Indeed, a certain amount of the liquid formed during the overcurrent testing had been used to form the hypo-eutectic alloy of Si-Ag, Al and Cu which covered the surface and the side wall of the crater. However, its volume should be significantly smaller than the volume of the crater itself. Therefore, based on the above calculated values of Q_b and Q_g, it is reasonable to say that both liquid phase and gas phase had been formed, the energy levels of 750 J and 1500 J are enough to vaporize certain amounts of Si, and the highest temperature reached the boiling point of Si, 3265°C, during the overcurrent testing of the sandwich structure samples.

As aforementioned, a certain amount of high temperature gas must have been produced during testing all the samples. Similar estimation of the energy required for a certain amount of solid Si, Cu, Al and Ag to become gas phase can be applied to all the tested samples. As an approximation, it is reasonable to say that for all the samples tested under energy levels of 500 J and above, the highest temperatures should be similar to the boiling point of Si, 3265°C, as estimated for the sandwich structure sample tested under 750 J. The different energy levels used during testing these samples resulted in different amounts of Si gas and different sizes of the craters formed within the Si IGBTs. For those samples tested under lower energy levels, the highest temperatures in the Al wire bonded samples should at least reach the boiling point of Al, 2519 °C, and those in the flexible PCB interconnected samples should at least reach the boiling point of Ag, 2162 °C.

5. Conclusions

Based on the above results and discussion, the following conclusions are drawn:

1) Depending on the energy levels applied during the overcurrent testing, the IGBT samples constructed with the three interconnect technologies can have both OCFM and SCFM.
2) The standard Al wire bonded IGBT sample can fail to SCFM under very low energy level. The flexible PCB interconnect and sandwich structure technologies can increase the energy levels for the IGBTs to achieve SCFM.
3) The sandwich structure IGBT sample can achieve SCFM under an energy level of 750 J which can meet realistic applications (as defined in section 2.2.2), and thus can provide a simpler and more cost-effective solution than the press pack technology for those applications.
4) The continuous conducting paths in those samples tested with SCFM is formed by the networked white phases within the solidification structure and the Sn-3.5Ag filled in

the cracks within the residual Si IGBT which formed the conductive channels to connect the residual Al wire bonds or flexible PCB and the residual Sn-3.5Ag solder joints together.

5) Both liquid phase and gas phase can be formed and the highest temperature can reach the boiling point of Si when the sandwich structure IGBT samples are tested with both SCFM and OCFM.

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Table 1 Summary of the results of the overcurrent testing from all the tested IGBT samples

	Energy (J)	Voltage (V)	Peak Current (A)	Saturation time (mS)	Failure Mode
Al wire bonded samples	750	156	-	-	OCFM
	500	128	6000	1	OCFM
	250	90	1800	5	OCFM
	125	63	600	7.5	OCFM
	62.5	45	1100	3.8	SCFM
Flexible PCB interconnected samples	500	128	6000	10.8	OCFM
	375	110	4600	14.8	OCFM
	312.5	101	1100	39.0	SCFM
	250	90	-	-	SCFM
Sandwich structure samples	1500	221	17500	2.0	OCFM
	750	156	9000	3.0	SCFM

Table 2 Thermal and physical properties of Cu andv Si used to calculate the energy required for the phase changes

	ρ (kg/m^3)	C (J/kg)	T_m (°C)	T_b (°C)	ΔH_m (kJ/kg)	ΔH_b (kJ/kg)
Cu	8960	385	1085	2562	205	4730
Si	2329	750	1414	3265	1926	12800

Fig. 1 Photograph of one as-prepared IGBT sample constructed with the AL wire bonding technology for the overcurrent testing.

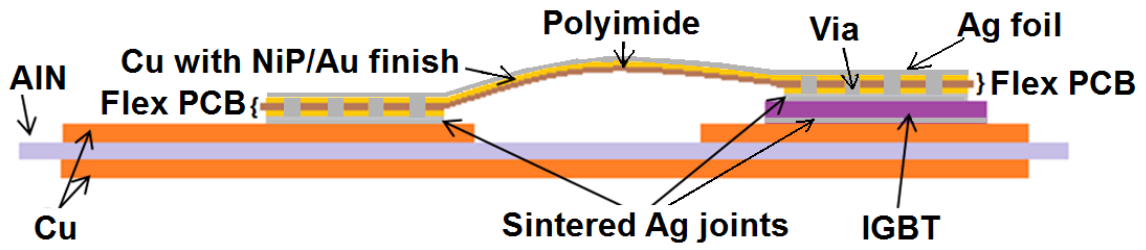


Fig. 2 Cross-sectional schematic of the flexible PCB interconnected IGBT sample (not to scale).

Fig. 3 Photograph of one as-prepared flexible PCB interconnected IGBT sample for the overcurrent testing.

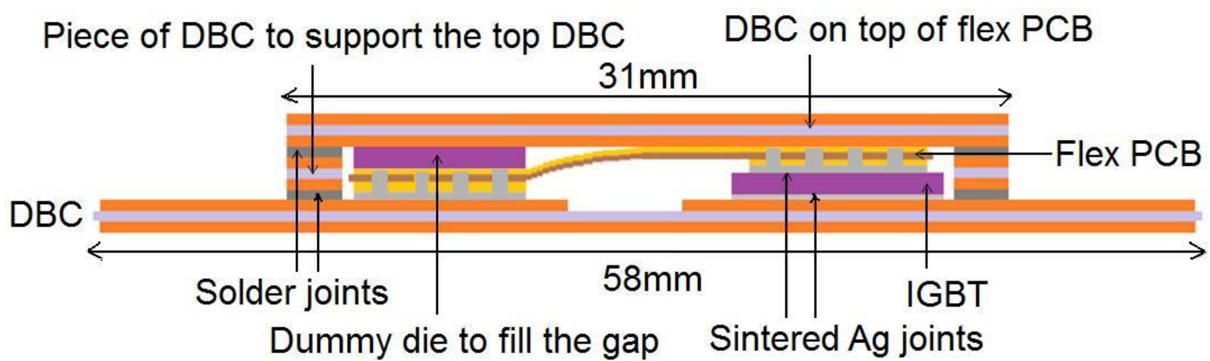


Fig. 4 Cross-sectional schematic of the sandwich structure IGBT sample (not to scale).

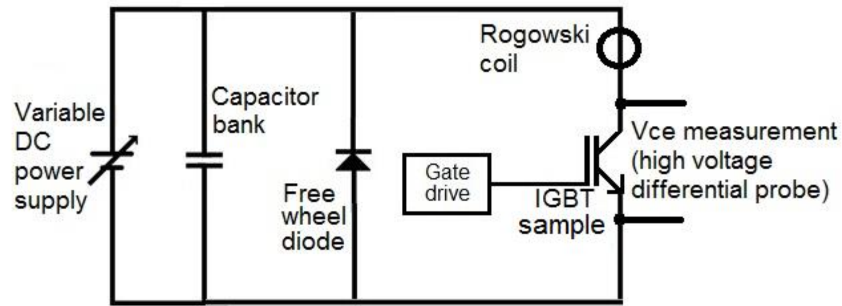


Fig. 5 Electrical circuit diagram of overcurrent testing.

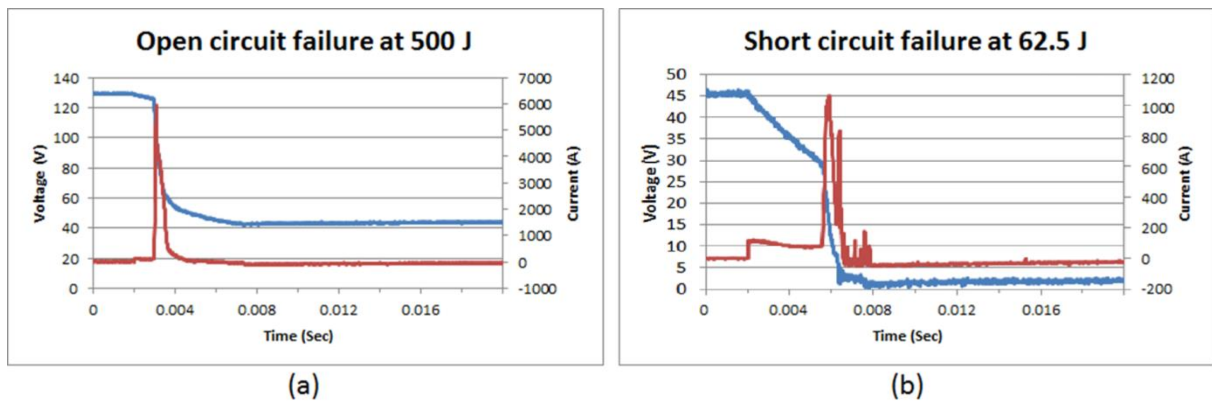


Fig. 6 Voltage and current waveforms of the Al wire bonded sample tested at: (a) 500 J; and (b) 62.5 J.

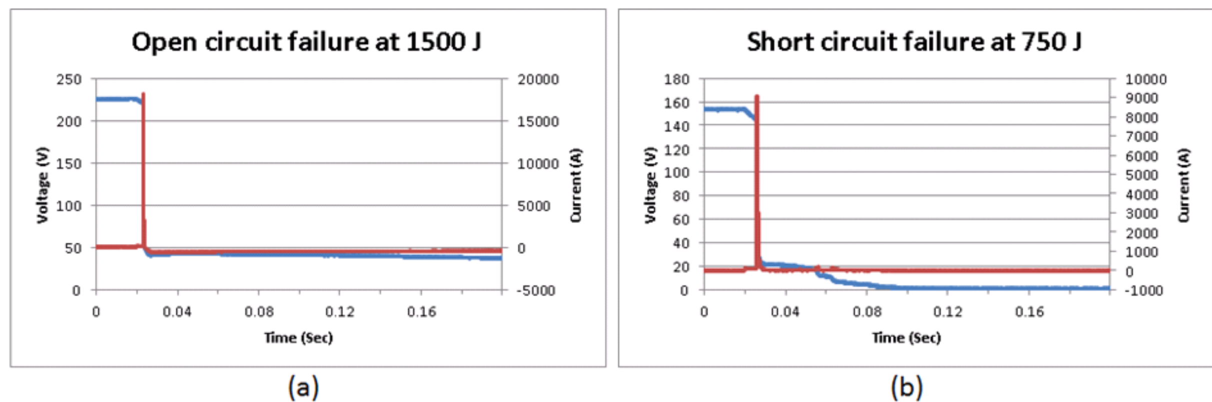


Fig. 7 Voltage and current waveforms of sandwich structure samples tested at: (a) 1500 J; and (b) 750 J.

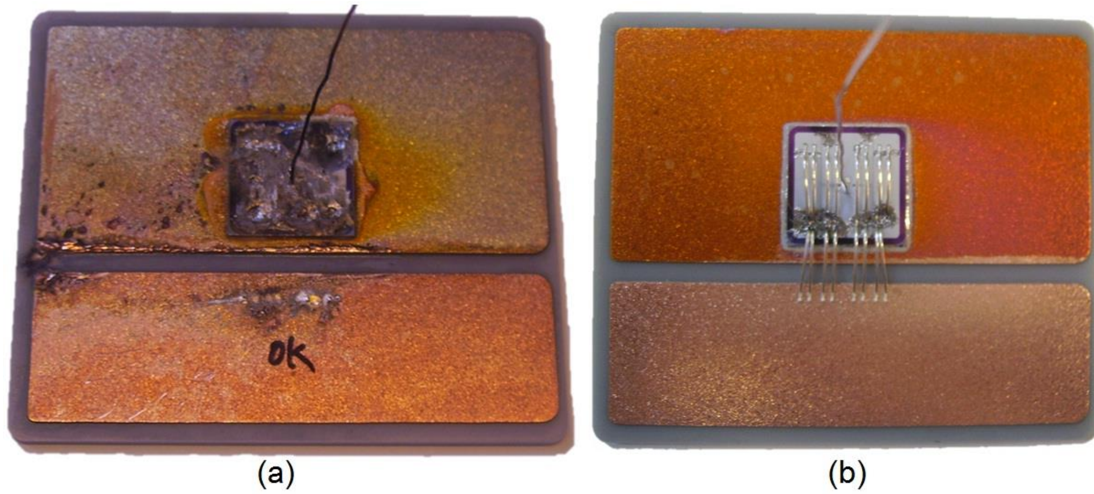


Fig. 8 Photographs of the Al wire bonded samples tested at: (a) 500 J, OCFM; and (b) 62.5 J, SCFM.

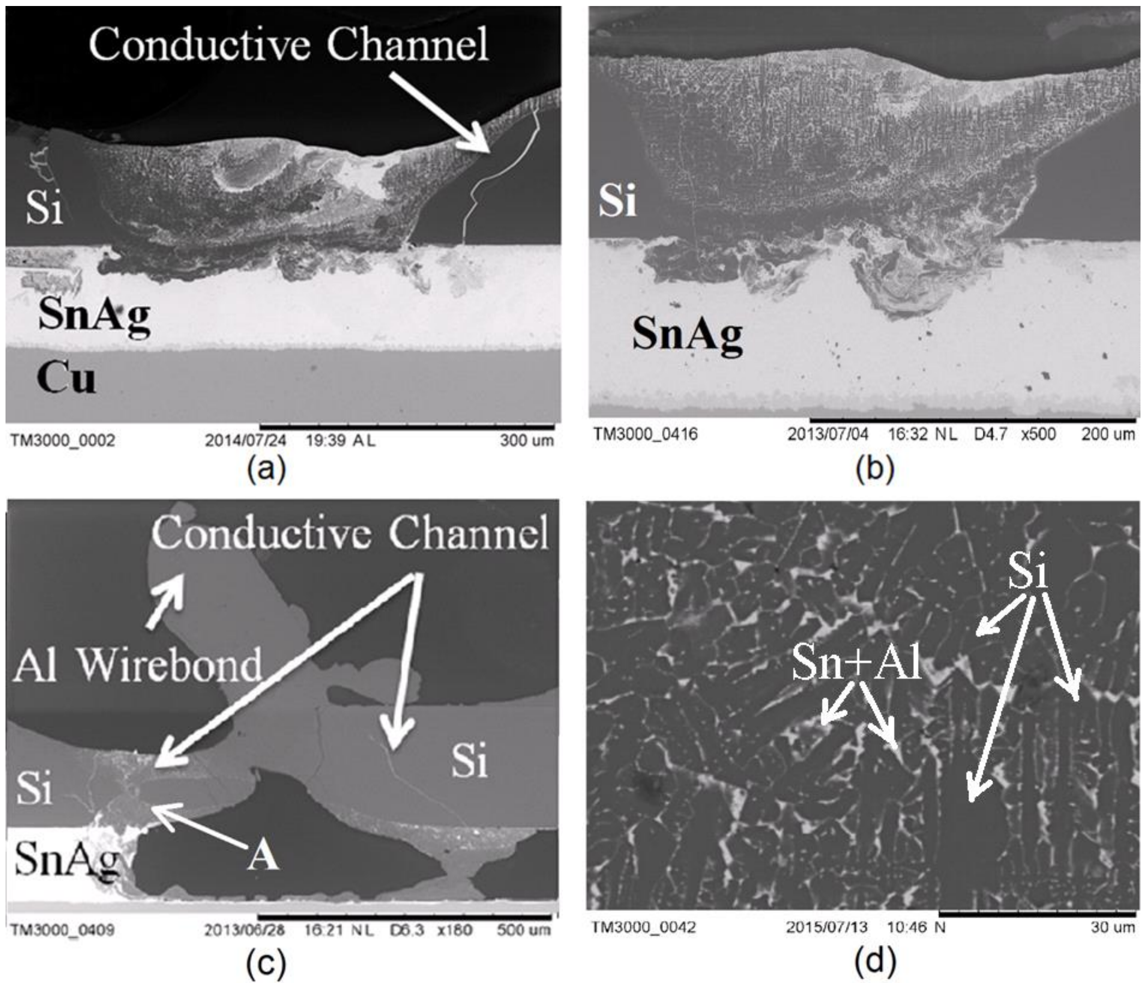


Fig. 9 SEM images taken from the polished cross sections of the Al wire bonded samples tested at: (a) 500 J, OCFM; (b) 500 J, OCFM, another location; (c) 62.5 J, SCFM; and (d) enlarged view around point A in (c).

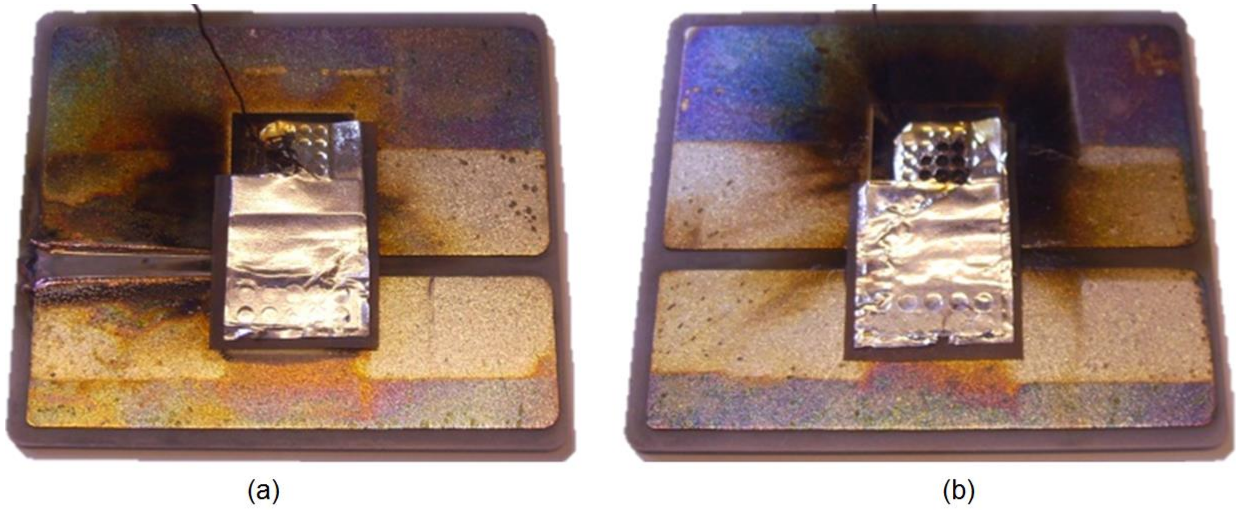


Fig. 10 Photographs of the flexible PCB interconnected samples tested at: (a) 500 J, OCFM; and (b) 312.5 J, SCFM.

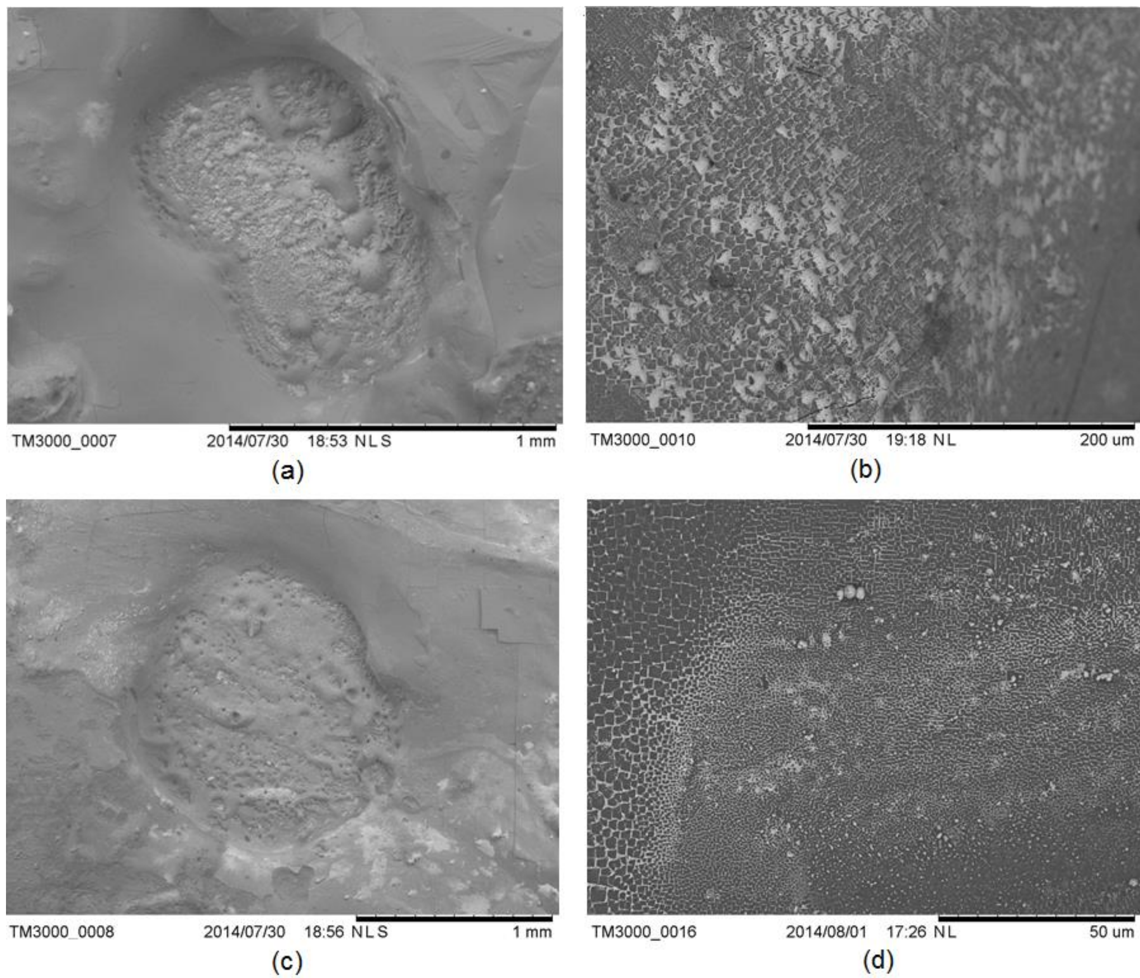


Fig. 11 SEM images taken from the surfaces of the flexible PCB interconnected samples tested at: (a) 500 J, OCFM; (b) enlarged local view of (a); (c) 312.5 J, SCFM; and (d) enlarged local view of (c).

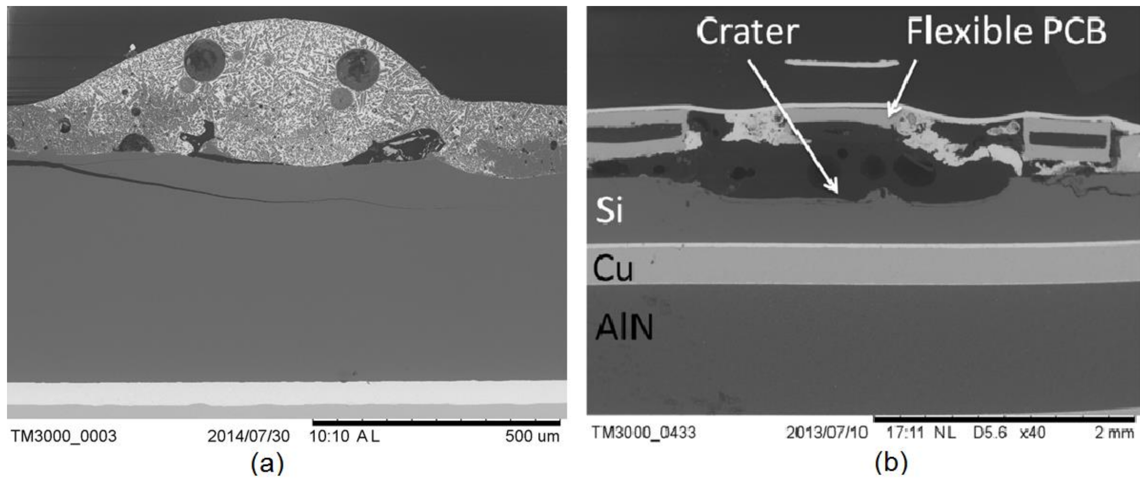


Fig. 12 SEM images taken from the polished cross sections of the flexible PCB interconnected samples tested at: (a) 500 J, OCFM; and (b) 312.5 J, SCFM.

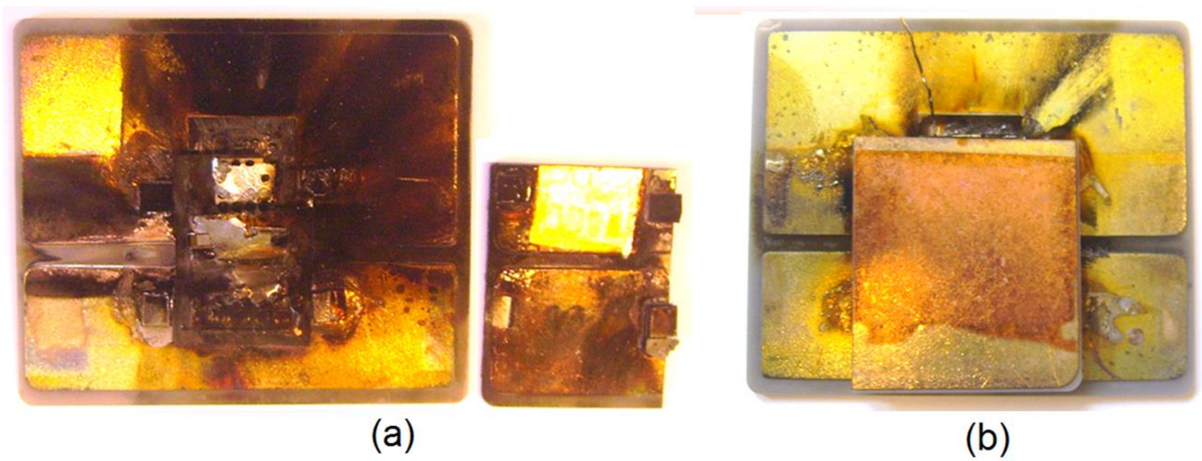
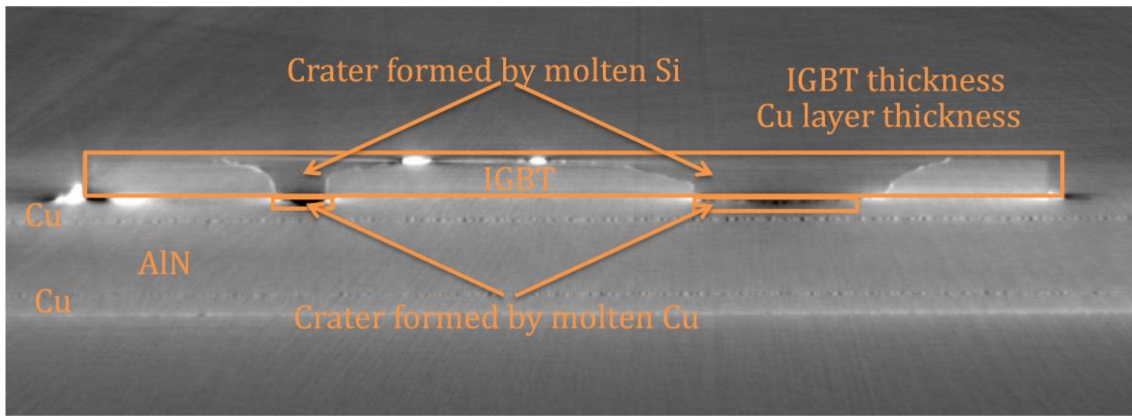
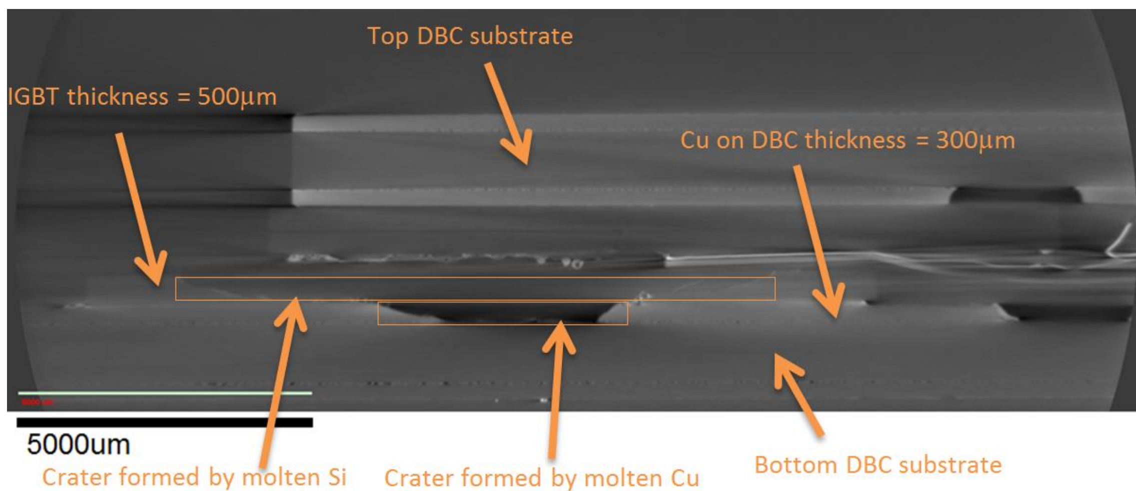


Fig. 13 Photographs of the sandwich structure samples tested at: (a) 1500 J, OCFM; and (b) 750 J, SCFM.



(a)



(b)

Fig. 14 Cross-sectional view selected from the reconstructed 3D X-ray CT images taken from the sandwich structure samples tested with: (a) OCFM under 1500 J, and (b) SCFM under 750 J.