A Novel Zero-Sequence Current Elimination PWM Scheme for an Open Winding PMSM with Common DC Bus

Zewei Shen, *Student Member, IEEE*, Dong Jiang, *Senior Member, IEEE*, Lei Zhu, *Student Member, IEEE*, Yunsong Xu, *Student Member, IEEE*, Tianjie Zou, *Member, IEEE*, Zicheng Liu, *Member, IEEE*, Ronghai Qu, *Fellow, IEEE*

***Abstract*- This paper introduces a novel pulse width modulation (PWM) scheme for an OW-PMSM driven by dual two-level three–phase inverter with common dc bus which can effectively deal with the inherent zero-sequence current (ZSC) problem. Based on conventional symmetrical unipolar double frequency SPWM scheme with appropriate phase-shift, the common mode voltage (CMV) of two inverters can keep the same and cancel out each other to eliminate the modulated zero sequence voltage (ZSV) disturbance source. In this case, the double frequency effect can be retained to reduce the ac side current ripple and suppress both the corresponding motor vibration and acoustic noise which is advantageous to improve the synthetic performance of motor. The DC bus voltage utilization of the novel PWM scheme is proved to reach the maximum value as same as the conventional modulated ZSV elimination scheme. Meanwhile, a zero-sequence controller is designed to suppress ZSC by further adjusting the two CMVs to counteract other zero-sequence disturbance sources. To verify the analysis, the proposed PWM technique associated with the control method is implemented in an OW-PMSM experimental setup to validate the superiority of proposed method.**

***Index terms*—Zero-sequence current, PWM, open-winding, PMSM, current ripple.**

I. Introduction

PWM-inverter-driven ac motors have become common in variable speed applications due to various advantages, such as high efficient, high dynamic performance and low harmonic distortion. Compared to conventional three-phase star-connected winding motor, open winding (OW) motor has the potential fault-tolerant capability because each phase current can be controlled separately [1] [2]. Moreover, the OW motor can be fed by dual-inverter which has higher DC bus utilization than the conventional single inverter fed star-connected winding motor and can reduce the voltage stress for power devices, so the dual inverter fed OW motor topology is favorable for the occasion that motor voltage is higher than DC link voltage. With the above advantages, OW motor drives are widely used in electric vehicles [3] [4], wind generation systems [5] [6] and aircraft starter-generator [7]. In addition, the dual two-level inverter can generate three-level phase voltage which has similar effect with the three-level inverter [8], but it has obvious advantages–the simple structure without neutral point clamping diode, the absence of neutral point fluctuation, and the flexibility and redundancy of space vector combinations [9]. So the dual inverter fed OW motor topology has the superiority comparing to the conventional three-level inverter fed star-connected winding motor topology.

However, owing to the opened neutral point of stator winding, the zero-sequence path in the motor emerges and the potential zero sequence current (ZSC) can be generated. Considering the power supply mode, the dual inverter usually can be fed by two isolated DC powers [10] [11] or single DC power [9] [12][13]. The two isolated DC powers can block the zero-sequence path in OW motor naturally and suppress the ZSC, the structure is shown in Fig. 1(a). Though this method can be adopted, the two isolated DC powers lead the system bulky and increase the cost. So in some occasions with the requirement of power density and cost, the single DC power fed dual inverter is preferred. When the single DC power is utilized shown in Fig. 1(b), the ZSC may has the possibility to be generated and consequently causing unwanted power losses, torque ripple which degrades the system performance [14]-[17].

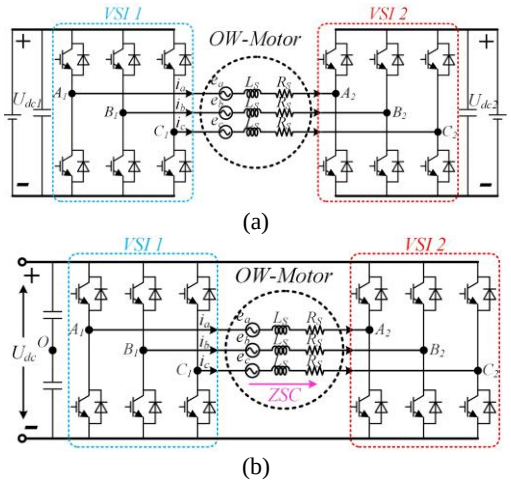


Fig. 1 The structures of dual two-level inverter fed OW motor: (a) with two isolated DC power, (b) with common DC power

Moreover, considering the type of OW motor, it can be roughly divided into two categories, *i.e.* the OW induction machine (OW-IM) and OW permanent magnet synchronous machine (OW-PMSM). Comparing to the OW-IM, the OW-PMSM is attracting more and more research attentions [14]-[19] [22] recently due to high efficiency, high torque density, and high power factor. For conventional OW-IM, the zero sequence voltage (ZSV) which is the source of ZSC is mainly caused by the differences of CMVs between two inverters. If the CMVs decided by the modulation scheme keep identical in every switching cycle, the ZSC can be limited in this case [9] [13]. Meanwhile, the inverter nonlinearity is regarded as another ZSV disturbance source of inverter [23]. The above two disturbance sources can be attributed to the inverter system. As for OW-PMSM, except for the above two ZSV sources, the OW-PMSM may induce the ZSV in the back

electromotive force (EMF) which may be a pivotal disturbance source of motor [15][16]. In addition, the ZSV generated by the cross coupling effect in zero-sequence circuit is another disturbance source of motor [19]. So the ZSV disturbance sources for the dual inverter fed OW-PMSM is more complicated than the OW-IM generally, and it should take more effort to control ZSC for OW-PMSM.

In order to suppress the ZSC, the modulation scheme combined with the corresponding control method should be implemented. Considering the elimination of the major ZSV disturbance source caused by the modulation scheme, the special designed PWM schemes which generate two identical CMVs for each inverters can be utilized [9][12][13]. In this case, the simple and popular ZSV elimination schemes based on two-level three-phase inverter modulation schemes can be implemented, *e.g.* the traditional SVPWM (space vector PWM) and DPWM (discontinuous PWM) with PWM signal rotation [19]-[21]. With the elimination of the major ZSV source of inverters, the ZSC can be relatively easy to be suppressed. In order to further reduce the ZSC, the freedom of zero vector redistribution is often utilized to adjust the output CMVs of two inverters [15] [18]-[20] to counteract other ZSV disturbance sources.

The essential ideal of the most utilized ZSV elimination method based on the SVPWM scheme is SPWM (sinusoidal PWM) scheme with zero-sequence signal injection for one inverter [24] and the PWM signal rotation which can guarantee the same PWM signals for two inverters [15] [18]-[20]. However, with the manner of PWM signal rotation, the dual inverter composed of six phase-legs is only driven by three different PWM signals. In this case, the duty cycles for one stator winding connected two phase-legs are coupled and cannot changed separately. So the freedom of the dual inverter is relatively reduced which may degrade of the PWM relevant performance, for instance, the most concerned current ripple of phase current in motor. The current ripple not only generate the copper and iron loss, but also induce the high frequency harmonic magnetic fields and corresponding electromagnetic force which further produce the adverse effect of electromagnetic vibration and acoustic noise in PMSM drives [25-29]. So it is critical issue to reduce the current ripple and improve the synthetic performance of motor.

Actually, the duty cycles can be controlled separately for each phase-legs and the current ripple performance has the possibility to be optimized. For example, the unipolar SPWM scheme can control the duty cycles separately for each phase-legs and fully utilize the freedom which has the potential to obtain the double frequency effect. What's more, the three-phase unipolar SPWM scheme for dual inverter can keep the average CMV of each inverter zero naturally, so it has the possibility to coordinate with the OW motor, the only problem is the six PWM signals taking the symmetric manner and generating the instantaneous ZSV pulses. So the modified method could be considered to eliminate the high frequency ZSV pulses. Since the phase-shift of voltage pulse is an optional freedom which can adjust the position of PWM signal in one switching cycle [30], the unipolar double frequency SPWM scheme can coordinate with proper phase-shift to eliminate the average and instantaneous ZSV [31] as well as optimize the current ripple of phase current. This paper is based on the above thinking and provides a complete scheme for the OW-PMSM with common dc bus.

The rest of this paper is organized as follows: in part II, the mathematical model of OW-PMSM with common dc bus is analyzed, and the zero-sequence equivalent circuit with the synthetic disturbance model is analyzed. In part III, the conventional ZSV elimination scheme based on the SVPWM is briefly investigated, and the principle of the novel ZSV elimination method based on the proposed modulation scheme is introduced and compared with the conventional SVPWM based method. In part IV, the OW-PMSM control method which includes the zero voltage vector adjustment based on the proposed ZSV elimination scheme and quasi proportional resonant (PR) controller is presented. The experimental results and validation are presented in part V. Conclusions are made in part VI finally.

II. The Mathematic Model of OW-PMSM with Common DC Bus

A. The Mathematic Model of OW-PMSM

Based on the topology shown in Fig. 1(b), the phase voltage equations of the OW-PMSM can be expressed as

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \boldsymbol{R_S} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \frac{d}{dt} \begin{bmatrix} \psi_a \\ \psi_b \\ \psi_c \end{bmatrix}. \tag{1}$$

where u_k, i_k, Ψ_k (k = a, b, c) are three phase voltages, currents and back EMFs, respectively. R_S is the stator resistance.

The back-EMF of OW-PMSM usually contains the zero-sequence harmonics (especially the third harmonic component) caused by the corresponding flux linkage harmonics. For a non-salient OW-PMSM, considering the dominated fundamental and third harmonic components of the rotor flux linkage, the flux equations can be expressed as

$$\begin{aligned} \begin{bmatrix} \psi_a \\ \psi_b \\ \psi_c \end{bmatrix} &= \begin{bmatrix} L_{m1}+L_{s\sigma} & M & M \\ M & L_{m1}+L_{s\sigma} & M \\ M & M & L_{m1}+L_{s\sigma} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \\ &+ \psi_f \begin{bmatrix} \cos(\omega_e t) \\ \cos(\omega_e t - 2\pi/3) \\ \cos(\omega_e t + 2\pi/3) \end{bmatrix} + \psi_{3f} \begin{bmatrix} \cos(3\omega_e t - \theta_1) \\ \cos(3\omega_e t - \theta_1) \\ \cos(3\omega_e t - \theta_1) \end{bmatrix}. \end{aligned} \tag{2}$$

where L_{m1} and $L_{s\sigma}$ represent the excitation inductance and leakage inductance of stator separately, M is the mutual inductance between two phase windings which is with negative value in three-phase symmetric PMSM, Ψ_f and Ψ_{3f} are the amplitudes of fundamental and third harmonic flux linkage, ω_e is electrical angular speed of motor, and θ_1 is the initial angle difference between the fundamental and third harmonic flux linkage.

With the transformation matrix from the three-phase stationary *abc* coordinate frame to the synchronous rotating *dq*0 coordinate frame in (3),

$$\boldsymbol{T}_{3s/3r}=\frac{2}{3}\begin{bmatrix}\cos(\omega_e t) & \cos(\omega_e t-2\pi/3) & \cos(\omega_e t+2\pi/3)\\ -\sin(\omega_e t) & -\sin(\omega_e t-2\pi/3) & -\sin(\omega_e t+2\pi/3)\\ 1/2 & 1/2 & 1/2\end{bmatrix} \quad (3)$$

the flux linkage in the *dq*0 frame can be represented as

$$\begin{bmatrix}\psi_d\\ \psi_q\\ \psi_0\end{bmatrix}=\boldsymbol{T}_{3s/3r}\begin{bmatrix}\psi_a\\ \psi_b\\ \psi_c\end{bmatrix}=\begin{bmatrix}L_{m1}+L_{s\sigma}-M & 0 & 0\\ 0 & L_{m1}+L_{s\sigma}-M & 0\\ 0 & 0 & L_{m1}+L_{s\sigma}+2M\end{bmatrix}\begin{bmatrix}i_d\\ i_q\\ i_0\end{bmatrix}.$$
$$+\begin{bmatrix}\psi_f\\ 0\\ \psi_{3f}\cos(3\omega_e t-\theta_1)\end{bmatrix}=\begin{bmatrix}L_d & 0 & 0\\ 0 & L_q & 0\\ 0 & 0 & L_0\end{bmatrix}\begin{bmatrix}i_d\\ i_q\\ i_0\end{bmatrix}+\begin{bmatrix}\psi_f\\ 0\\ \psi_{3f}\cos(3\omega_e t-\theta_1)\end{bmatrix} \quad (4)$$

where the subscripts *d*, *q*, and 0 represent the components in *dq*0 frame, respectively. So in the OW-PMSM, the *d*- and *q*-axis inductances keep identical as $L_{m1}+L_{s\sigma}-M$, while the total 0-axis inductance is $L_{m1}+L_{s\sigma}+2M$. Since the mutual inductance *M* is negative, the 0-axis inductance is obviously reduced by mutual inductance which results in smaller inductance comparing to the *d*- and *q*-axis inductances, so ZSC is relatively easy to be excited by the ZSV disturbance source.

Thus, the voltage equation in dq0 frame can be written as:

$$\begin{bmatrix}u_d\\ u_q\\ u_0\end{bmatrix}=\boldsymbol{T}_{3s/3r}\begin{bmatrix}u_a\\ u_b\\ u_c\end{bmatrix}=\boldsymbol{T}_{3s/3r}\left(\boldsymbol{R}_S\begin{bmatrix}i_a\\ i_b\\ i_c\end{bmatrix}+\frac{d}{dt}\begin{bmatrix}\psi_a\\ \psi_b\\ \psi_c\end{bmatrix}\right).$$
$$=\begin{bmatrix}R_S & -\omega_e L_q & 0\\ \omega_e L_d & R_S & 0\\ 0 & 0 & R_S\end{bmatrix}\begin{bmatrix}i_d\\ i_q\\ i_0\end{bmatrix}+\begin{bmatrix}L_d & 0 & 0\\ 0 & L_q & 0\\ 0 & 0 & L_0\end{bmatrix}\frac{d}{dt}\begin{bmatrix}i_d\\ i_q\\ i_0\end{bmatrix}+\begin{bmatrix}0\\ \omega_e\psi_f\\ -3\omega_e\psi_{3f}\sin(3\omega_e t-\theta_1)\end{bmatrix} \quad (5)$$

where u_d, u_q, u_0 represent *d*-, *q*-axis and zero-sequence voltages, i_d, i_q, i_0 represent *d*-, *q*-axis and zero-sequence currents respectively. In addition, with the above transformation matrix $T_{3s/3r}$, the modulated ZSV u_0 and ZSC i_0 can be easily deduced and expressed as

$$\begin{cases}u_0=(u_a+u_b+u_c)/3\\ i_0=(i_a+i_b+i_c)/3\end{cases}. \quad (6)$$

It can be seen that the ZSV and ZSC are the average value of three phase voltage and current, respectively. What's more, with the existence of ZSC and $L_d=L_q$, the electromagnetic torque [15][16] in OW-PMSM can be expressed as

$$T_e=\frac{3}{2}n_p\left[\psi_f i_q-6\psi_{3f}\sin(3\omega_e t-\theta_1)i_0\right]=T_1+T_{ripple}. \quad (7)$$

$$\begin{cases}T_1=\frac{3}{2}n_p\psi_f i_q\\ T_{ripple}=-9n_p\psi_{3f}\sin(3\omega_e t-\theta_1)i_0\end{cases}. \quad (8)$$

where n_p is pole pairs of motor, T_1 is the torque produced by *q*-axis current, and T_{ripple} is the torque ripple produced by ZSC. With the existence of third order harmonic current in ZSC, the six times fundamental frequency torque ripple will be generated which causes adverse effect for motor. Moreover, the ZSC also generates power fluctuation, induce the extra power loss for the system, and influences the full utilization of the VSI (voltage source inverter) capacity [15]-[17]. Therefore, it is a critical issue for OW-PMSM with common dc bus to suppress the ZSC.

B. The Analysis of Zero-Sequence circuit model in OW-PMSM with Common DC Bus

In order to suppress the ZSC, the different ZSV disturbance sources should be recognized. The ZSV caused by the inverter system is first considered. For dual two-level three-phase inverter fed OW-PMSM, when taking the DC link middle point O as reference shown in Fig. 1(b), the pole voltage of all phase–legs can switch between $U_{dc}/2$ and $-U_{dc}/2$ with the DC link voltage of U_{dc}. Generally, the CMV of VSI is the instantaneous average voltage of all phase-legs. So the CMVs of VSI1 and VSI2 can be defined in (9),

$$\begin{cases}U_{cm1}=(V_{A1O}+V_{B1O}+V_{C1O})/3\\ U_{cm2}=(V_{A2O}+V_{B2O}+V_{C2O})/3\end{cases}. \quad (9)$$

where U_{cm1} and U_{cm2} are the CMVs of the two VSIs correspondingly, and V_{A1O}, V_{A2O}, V_{B1O}, V_{B2O}, V_{C1O}, V_{C2O} are the output instantaneous pole voltages. So the modulated ZSV disturbance source caused by the inverter system can be deduced as

$$u_{0\_PWM}=U_{cm1}-U_{cm2}. \quad (10)$$

Since u_{0_PWM} is the difference between the two CMVs of VSIs and decided by the modulation scheme, it has the possibility to be zero if two VSIs generate the identical CMV. Moreover, the inverter nonlinearity caused by the voltage drop of switching device and dead time effect can induce another ZSV disturbance source [23] which is also attributed to the inverter system. This ZSV disturbance source has strong correlation with the three-phase currents which can be modeled as the current control voltage source (CCVS) [19] and expressed as $u_{0\_nonlinearity}=f_n(i_a,i_b,i_c)$. In addition, the motor side ZSV disturbance source should also be considered. The first obvious ZSV disturbance source is the third harmonic $-3\omega_e\Psi_{3f}\sin(3\omega_e-\theta_1)$ in back-EMF. The other ZSV disturbance source in motor side is the cross coupling voltages in zero-sequence circuit caused by the d- and q-axis currents [19] which also have the CCVS characteristic and can be represented as $u_{0\_id}=f_d(i_d)$ and $u_{0\_iq}=f_q(i_q)$. The detailed principle and expressions for the three CCVSs $u_{0\_nonlinearity}$, u_{0_id} and u_{0_iq} can be found in literature [17] and [19].

Based on the above analysis, the zero-sequence equivalent circuit model can be set up and shown in Fig. 2. The dual inverter generates two ZSV disturbance sources: u_{0_PWM} and $u_{0\_nonlinearity}$, while the OW-PMSM induces the two kind ZSV disturbance sources: $-3\omega_e\Psi_{3f}\sin(3\omega_e-\theta_1)$, u_{0_id} and u_{0_iq}. As shown in (4), the zero sequence impedance based on L_0 usually has small value, so the big ZSC can be easily induced by the ZSV disturbance sources.

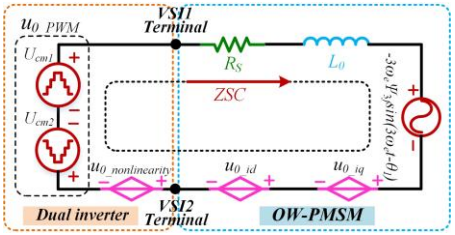


Fig. 2 The zero-sequence equivalent circuit model of OW-PMSM with common dc bus

In order to suppress the ZSC, the promising controllable ZSV disturbance source should be determined. Generally, all the ZSV disturbance sources except u_{0_PWM} are uncontrollable, but their amplitude could be limited with the optimal design of motor and compensation approach of inverter nonlinear. Contrary, u_{0_PWM} is a directly controllable ZSV disturbance source decided by modulation scheme, and the amplitude can be controlled large enough to counteract others ZSV disturbance sources. So u_{0_PWM} can be recognized as the promising ZSV disturbance source. With above analysis, in order to eliminate the ZSC, the core mentality is to modulate u_{0_PWM} to zero with appropriate modulation scheme [26] first, and then counteract with other ZSV disturbance sources by fine-tuning the u_{0_PWM} based on the ZSC closed-loop control.

III. The Novel PWM Scheme for OW-PMSM with Common DC Bus

In this part, the principle of conventional SVPWM based ZSV elimination scheme is first introduced; then the novel ZSV elimination modulation scheme based on the SPWM scheme and phase-shift manner is proposed; what's more, the characteristic and performance of the two schemes are investigated to make fair comparison finally.

For dual two-level inverter, each VSI can generate the same eight space voltage vectors shown in Fig. 3(a) and (b). The eight space voltage vectors have four CMV values totally, the peak value are $U_{dc}/2$ and $-U_{dc}/2$ corresponding to the voltage vectors V_7(111) and V_0(000), the voltage vectors V_1(100), V_3(010)and V_5(001) have the same CMV value of $-U_{dc}/6$, and the voltage vectors V_2(110), V_4(011)and V_6(101) have the same CMV value of $U_{dc}/6$.

Based on the combination of different voltage vectors for each VSI, the modulated ZSV of all voltage vector combinations can be calculated which has seven kinds of values shown in Table. I. For example, V_{15}' means utilizing the voltage vector V_1 of VSI1 and voltage vector V_5' of VSI2 to synthesize the zero ZSV voltage vector because both VSIs generate the same CMV of $-U_{dc}/6$. From Table I, it can be seen that there are total twenty voltage vector combinations which can realize the zero ZSV. These synthesized voltage vectors can be divided into two kinds: the zero voltage vectors which have no effect to synthesis of reference vector, and the effective voltage vectors which can be used to synthesize the reference vector. The all chosen zero ZSV voltage vectors in dual two-level inverter and the relationship to basic two-level inverters' voltage vectors can be drawn and shown in Fig. 4. In this case, zero ZSV can be realized if taking suitable arrangement of these special voltage vectors in every switching period.

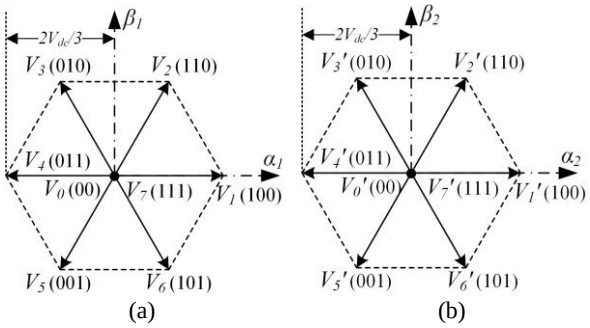


Fig. 3 The space voltage vectors of individual VSIs: (a) VSI1, (b) VSI2

TABLE I
RESULTED ZSV OF DIFFERENT VECTOR COMBINATIONS

Combinations of switching states	ZSV
V_{70}'	U_{dc}
V_{71}', V_{73}', V_{75}', V_{20}', V_{40}', V_{60}'	$2U_{dc}/3$
V_{72}', V_{74}', V_{76}', V_{10}', V_{30}', V_{50}', V_{21}', V_{23}', V_{25}', V_{41}', V_{43}', V_{45}', V_{61}', V_{63}', V_{65}'	$U_{dc}/3$
V_{00}', V_{11}', V_{22}', V_{33}', V_{44}', V_{55}', V_{66}', V_{77}', V_{24}', V_{26}', V_{42}', V_{46}', V_{62}', V_{64}', V_{13}', V_{15}', V_{35}', V_{31}', V_{51}', V_{53}'	***0***
V_{27}', V_{47}', V_{67}', V_{01}', V_{03}', V_{05}', V_{12}', V_{32}', V_{52}', V_{14}', V_{34}', V_{54}', V_{16}', V_{36}', V_{56}'	$-U_{dc}/3$
V_{17}', V_{37}', V_{57}', V_{02}', V_{04}', V_{06}'	$-2U_{dc}/3$
V_{07}'	$-U_{dc}$

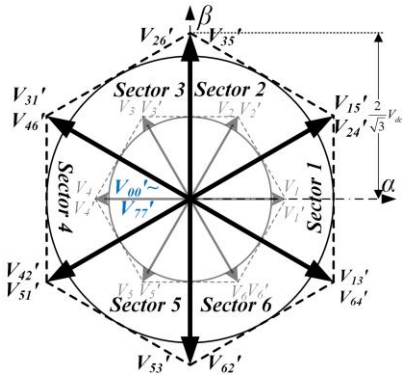


Fig. 4 The zero ZSV voltage vectors for dual-inverter

A. Principle of Conventional SVPWM Based ZSV Elimination Scheme

The conventional ZSV elimination modulation scheme for dual-inverter can be deduced from SVPWM scheme. The principle is based on the PWM signals rotation which ensures VSI1 and VSI2 taking the same three PWM signals and generates the identical CMVs. Without losing generality, assuming the three-phase duty cycle in VSI1 satisfies the relationship that $d_{a1}>d_{b1}>d_{c1}$. By exchanging the sequence of PWM signals for VSI1, the corresponding PWM signals for VSI2 can be generated shown in Fig. 5, where G_{a1}, G_{b1}, G_{c1} and G_{a2}, G_{b2}, G_{c2} are the three-phase PWM signals for VSI1 and VSI2, respectively. T_S is the switching cycle. In this case, the CMVs of different VSIs can keep identical, and the combined voltage vectors in one switching cycle are V_{00}'-V_{13}'-V_{24}'-V_{77}'-V_{24}'-V_{13}'-V_{00}' which naturally satisfies the requirement of utilizing zero ZSV voltage vectors, so the ZSV

generated by modulation scheme can be eliminated in ideal condition.

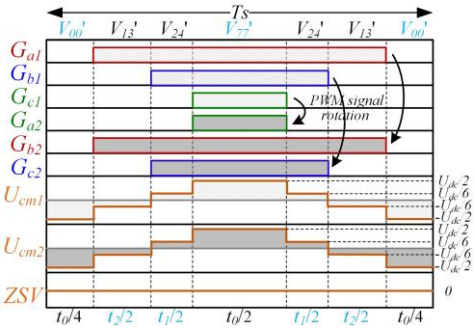


Fig. 5 Conventional SVPWM based ZSV elimination modulation scheme

Considering the average output pole voltage, the above schemes satisfy the equations:

$$\boldsymbol{V_{A1O}=V_{B2O}\quad V_{B1O}=V_{C2O}\quad V_{C1O}=V_{A2O}}. \tag{11}$$

The space voltage vectors $\overrightarrow{V_{ref1}}$ and $\overrightarrow{V_{ref2}}$ can be represented as:

$$\begin{cases}\overrightarrow{\boldsymbol{V_{ref1}}}=\boldsymbol{V_{A1O}}+\boldsymbol{V_{B1O}}e^{j2\pi/3}+\boldsymbol{V_{C1O}}e^{-j2\pi/3}\\ \overrightarrow{\boldsymbol{V_{ref2}}}=\boldsymbol{V_{A2O}}+\boldsymbol{V_{B2O}}e^{j2\pi/3}+\boldsymbol{V_{C2O}}e^{-j2\pi/3}\\ \quad=\boldsymbol{V_{C1O}}+\boldsymbol{V_{A1O}}e^{j2\pi/3}+\boldsymbol{V_{B1O}}e^{-j2\pi/3}=e^{j2\pi/3}\overrightarrow{\boldsymbol{V_{ref1}}}\end{cases}. \tag{12}$$

The included angle of the two voltage vectors is 120 °, and the output resultant space vector $\overrightarrow{V_{ref}}$ can be expressed as:

$$\overrightarrow{\boldsymbol{V_{ref}}}=\overrightarrow{\boldsymbol{V_{ref1}}}-\overrightarrow{\boldsymbol{V_{ref2}}}=\overrightarrow{\boldsymbol{V_{ref1}}}-e^{j2\pi/3}\overrightarrow{\boldsymbol{V_{ref1}}}=\sqrt{3}e^{-j\pi/6}\overrightarrow{\boldsymbol{V_{ref1}}}. \tag{13}$$

So the resultant voltage vector $\overrightarrow{V_{ref}}$ lags behind the synthetic voltage vector $\overrightarrow{V_{ref1}}$ with 30 °while the amplitude is $\sqrt{3}$ times of synthetic voltage vector for single VSI.

B. Principle of Novel ZSV Elimination Scheme Based on SPWM and Phase-Shift

In conventional symmetrical SPWM scheme (symmetrical sampling with one update of modulation signal per switching period), the three-phase duty cycles of VSI1 can be expressed as:

$$\begin{cases}\boldsymbol{d_{a1}}=\left(1+\boldsymbol{m}\cos\boldsymbol{\theta}\right)/2\\ \boldsymbol{d_{b1}}=\left[1+\boldsymbol{m}\cos\left(\boldsymbol{\theta}-2\pi/3\right)\right]/2\\ \boldsymbol{d_{c1}}=\left[1+\boldsymbol{m}\cos\left(\boldsymbol{\theta}+2\pi/3\right)\right]/2\end{cases}. \tag{14}$$

where d_{a1}, d_{b1} and d_{c1} are the three phase duty cycles, respectively; m is the modulation index within the range of (0, 1); θ is the instantaneous angle for phase A_1. The above equations can deduce the identical equation

$$\boldsymbol{d_{a1}+d_{b1}+d_{c1}=3/2}. \tag{15}$$

Since the phase voltage is the difference of the two phase-leg voltages, the corresponding two phase-leg voltages in one phase should keep the same modulation index and opposite phase to obtain the maximum output phase voltage, so the duty cycles of the corresponding two phase-legs should keep complementary. In this case, the relationship of duty cycles for each phase can be expressed as follows:

$$\boldsymbol{d_{a1}+d_{a2}=1\quad d_{b1}+d_{b2}=1\quad d_{c1}+d_{c2}=1}. \tag{16}$$

Thus, the three-phase duty cycles for VSI2 also satisfies the identical equation

$$\boldsymbol{d_{a2}+d_{b2}+d_{c2}=3/2}. \tag{17}$$

Under above conditions, without losing generality, assuming d_{a1} is maximal in six phase-legs which can deduce d_{a2} is minimal, and $d_{b1}>d_{c1}$, $d_{b2}<d_{c2}$, so the six PWM signals, CMVs and ZSV for conventional symmetrical SPWM scheme can be drawn and shown in Fig. 6(a). It can be found that the rising and falling edges of PWM signals are in different positions which generate different instantaneous CMVs for the two VSIs. Moreover, though the summation of three-phase duty cycles for the two VSIs always keep identical which can eliminate the average ZSV, the instantaneous CMVs difference generate the high frequency ZSV pulses which lose the function of eliminating ZSV and induce the high frequency ZSC. This phenomenon is owing to the symmetric manner for conventional SPWM scheme. If appropriate phase-shift used, the rising and falling edges have the ability to be aligned correspondingly.

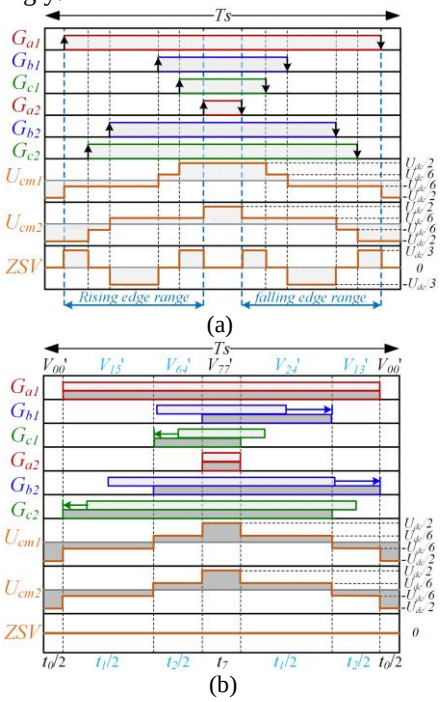


Fig. 6 The PWM signals, CMVs and ZSV for conventional symmetric SPWM scheme and novel phase-shift SPWM scheme in one switching period: (a) the conventional symmetric SPWM scheme, (b) the novel phase-shift SPWM scheme

In fact, setting the maximum and minimum duty cycle in symmetric PWM scheme can prescribe limits to the range of rising and falling edges. With this specified edge ranges, the phase-shift can be implemented in this edge ranges and avoid the spillover problem which can promise to add no extra switching actions in one switching cycle. Fig. 6(b) show the principle of the proposed phase-shift scheme to eliminate the instantaneous ZSV in one switching period. In this scheme, the PWM signals of phase A which has the maximum or minimum duty cycle keeping symmetric while the PWM

signals of phase B and C taking the phase-shift manner. When the rising edge of C_2 PWM signal aligned with the rising edge of A_1 PWM signal with left side phase-shift, and the falling edge of B_2 PWM signal aligned with the falling edge of A_1 PWM signal with right side phase-shift, the state transition of ZSV caused by A_1 PWM signal can be cancelled out with cooperation of B_2 and C_2 PWM signals. Similarly, the rising edge of B_1 PWM signal and the falling edge of C_1 PWM signal can be aligned with the rising and falling edges of A_2 with proper phase-shift. The above phase-shift manner can keep the rising edges and falling edges stay in the corresponding position range.

What's more, the left rising and falling edge positions should be taken into account, such as the falling edges of B_1 and C_2 PWM signals, the rising edges of C_1 and B_2 PWM signal. These edge positions can be calculated by the duty cycle and the length of phase-shift. The positions of remaining PWM edges can be expressed as:

$$\begin{cases} Ep_{B1\_f} = Ep_{B1\_r} + d_{b1} = Ep_{A2\_r} + d_{b1} = (1-d_{a2})/2 + d_{b1} \\ Ep_{C1\_r} = Ep_{C1\_f} - d_{c1} = Ep_{A2\_f} - d_{c1} = (1+d_{a2})/2 - d_{c1} \\ Ep_{B2\_r} = Ep_{B2\_f} - d_{b2} = Ep_{A1\_f} - d_{b2} = (1+d_{a1})/2 - d_{b2} \\ Ep_{C2\_f} = Ep_{C2\_r} + d_{c2} = Ep_{A1\_r} + d_{c2} = (1-d_{a1})/2 + d_{c2} \end{cases} . \quad (18)$$

where Ep_{B1_f}, Ep_{C2_f}, Ep_{B2_r} and Ep_{C1_r} are the rising and falling edge positions correspondingly. Considering (15), (16) and (17), the rising edges and falling edges can be proved to be equal shown in (19) and (20).

$$\begin{aligned} Ep_{B1\_f} &= (1-d_{a2})/2 + d_{b1} = d_{a1}/2 + d_{b1} = (1-d_{a1})/2 + d_{a1} + d_{b1} - 1/2 \\ &= (1-d_{a1})/2 + 1 - d_{c1} = (1-d_{a1})/2 + d_{c2} = Ep_{C2\_f} \end{aligned} \quad (19)$$

$$\begin{aligned} Ep_{C1\_r} &= (1+d_{a2})/2 - d_{c1} = 1 - d_{a1}/2 - d_{c1} = (1+d_{a1})/2 - d_{a1} - d_{c1} + 1/2 \\ &= (1+d_{a1})/2 + d_{b1} - 1 = (1+d_{a1})/2 - d_{b2} = Ep_{B2\_r} \end{aligned} \quad (20)$$

In this case, all of the rising edges and falling edges can keep aligned for the conventional SPWM scheme with the combination of proper phase-shift, so the CMVs of two VSIs can keep identical and eliminate the ZSV shown in Fig. 6(b). Considering the voltage vectors combination, it can be found that all combined voltage vectors are changed to zero ZSV voltage vectors, while the time segment of this combined voltage vectors changes to asymmetrical which is different from the SVPWM based ZSV elimination scheme. According to the characteristic of the above manner, this modified scheme can be called as PS_SPWM (phase-shift SPWM) method.

In addition, considering the average output pole voltages, the above scheme satisfies the equations:

$$V_{A1O} = -V_{A2O} \quad V_{B1O} = -V_{B2O} \quad V_{C1O} = -V_{C2O} . \quad (21)$$

The relationship of synthetic voltage vectors for each VSI can be deduced that $\overrightarrow{V_{ref1}}$ and $\overrightarrow{V_{ref2}}$ have the same amplitude and opposite directions.

$$\begin{aligned} \overrightarrow{V_{ref2}} &= V_{A2O} + V_{B2O}e^{j2\pi/3} + V_{C2O}e^{-j2\pi/3} \\ &= -\left(V_{A1O} + V_{B1O}e^{j2\pi/3} + V_{C1O}e^{-j2\pi/3}\right) = -\overrightarrow{V_{ref1}} . \end{aligned} \quad (22)$$

The included angle of the two voltage vectors is 180°, and the output resultant space vector $\overrightarrow{V_{ref}}$ can be expressed as:

$$\overrightarrow{V_{ref}} = \overrightarrow{V_{ref1}} - \overrightarrow{V_{ref2}} = \overrightarrow{V_{ref1}} + \overrightarrow{V_{ref1}} = 2\overrightarrow{V_{ref1}} . \quad (23)$$

Thus, considering reference voltage combination for these ZSV elimination schemes, the different principles are shown in Fig. 7. For conventional SVPWM scheme, the relationship among the synthetic voltage vectors for each VSI $\overrightarrow{V_{ref1}}$, $\overrightarrow{V_{ref2}}$ and resultant voltage vector $\overrightarrow{V_{ref}}$ has been deduced in (12) and (13), so the relative position for these voltage vectors can be drawn and shown in Fig. 7(a). As for the proposed PS_SPWM scheme, the relationship can be deduced in (22) and (23), and relative position for the synthetic voltage vectors are shown in Fig. 7(b). It can be clearly seen that the principle of voltage vector synthesis for this two methods have distinct difference.

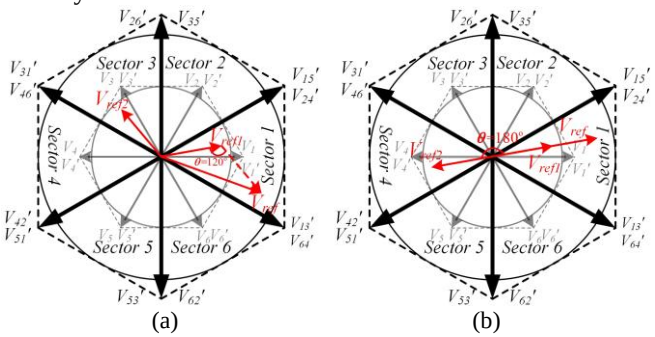


Fig. 7 The reference voltage combination for two ZSV elimination schemes: (a) the conventional SVPWM with signal rotation scheme, (b) the novel PS_SPWM scheme

In this case, the modulation index range for this two ZSV elimination schemes should make comparison. Fig. 8 shows the normalized phase and pole voltages for phase A (with the $U_{dc}/2$ as reference) at the maximal modulation index for the two schemes. For conventional SVPWM scheme, the pole voltages are non-sinusoidal by injecting the zero-sequence component and the maximal modulation index can increase to 1.15. With the operation of signal rotation to cancel out the zero-sequence component, though the phase voltage can keep sinusoidal, the peak value of phase voltage only reaches the $\sqrt{3}$ times of pole voltage which is the value of U_{dc}. So the actually maximal modulation index of phase voltage is 2 in this case. As for the novel PS_SPWM scheme, the phase-shift manner has no effect on duty cycle as well as the modulation index range, so there is no zero-sequence component injected in the pole voltage and the maximal modulation index is also kept 1 for the novel SPWM scheme. So the maximal modulation index of phase voltage can also reach the maximal value 2 which has the same value comparing to conventional scheme which proves the proposed PS_SPWM scheme would not reduce the modulation index range for dual inverter.

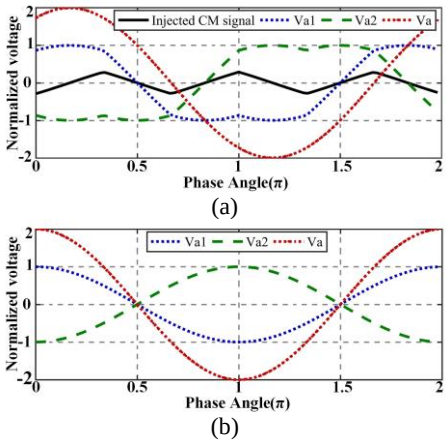


Fig. 8 The normalized phase and pole voltages of phase A for two ZSV elimination schemes: (a) the conventional SVPWM with signal rotation scheme, (b) the novel PS_SPWM scheme

What's more, the total harmonic distortion (THD) for this two ZSV elimination schemes should be considered. Fig. 9 shows the modulation index scanning result of phase voltage normalized switching harmonic for the two schemes. For conventional SVPWM scheme shown in Fig. 9(a), the phase voltage contains abundant odd and even switching harmonics. The dominated odd 1st switching harmonic is monotonically increased which reaches the peak value 0.7359 at the maximum modulation index, while the dominant even 2nd switching harmonic is non-monotonic with the peak value of 0.9667 at about half modulation index. As for the novel PS_SPWM scheme shown in Fig. 9(b), the phase voltage mainly contains the even switching harmonics and almost eliminate the odd switching harmonics. The dominated even 2nd switching harmonic is also non-monotonic with the peak value of 1.066 which is close to the peak value of 2nd switching harmonic for conventional SVPWM scheme.

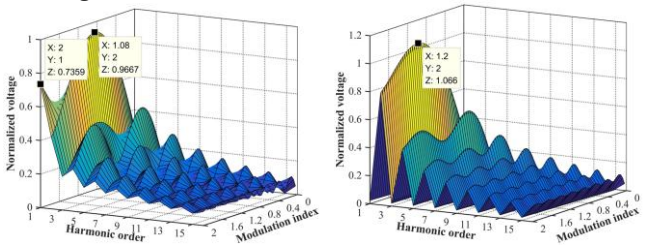


Fig. 9 The normalized phase voltage spectrum for the two ZSV elimination schemes: (a) conventional SVPWM with signal rotation scheme, (b) the novel PS_SPWM scheme

Considering the fact that the normalized phase voltage spectrum cannot directly judge the superior of the proposed PS_SPWM scheme, the equivalent current THD which is a universal indicator regardless the undetermined parameters can be calculated based on the normalized phase voltage spectrum and the corresponding harmonic orders, *i.e.*

$$\boldsymbol{THD} = \sqrt{\sum_{\boldsymbol{n}=1,2,3,\cdots}^{\infty} \left(\frac{\boldsymbol{V_n}}{\boldsymbol{n}}\right)^2}. \qquad (24)$$

Where n is the switching harmonic order. The result of the dominant equivalent switching harmonic currents and equivalent current THD are shown in Fig. 10. It can be seen that the equivalent current THD of the two schemes are close to each other when the modulation index is lower than 0.6, so the current THD reduction effect for the PS_SPWM scheme can be neglected in this range. When the modulation index is further increased, the equivalent current THD of the PS_SPWM scheme is smaller than the conventional SVPWM scheme, obviously in high modulation index range. The equivalent current THD of the SVPWM scheme is monotonically increased which reaches the peak value of 0.7738 at the maximum modulation index, while the equivalent current THD of the PS_SPWM scheme is non-monotonic and the value is only 0.4184 at the maximum modulation index which means the equivalent current THD can reduce 45.93% comparing to the conventional SVPWM scheme theoretically. So it is obvious that the proposed PS_SPWM scheme has better performance than the conventional SVPWM scheme in high frequency current ripple reduction.

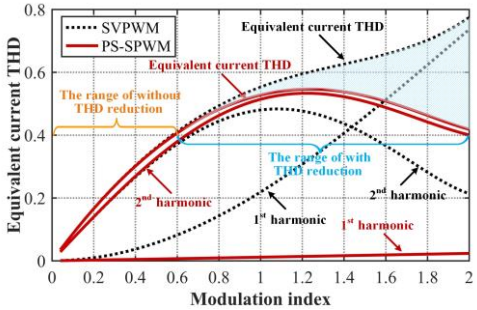


Fig. 10 The equivalent current THD and the equivalent dominant switching harmonic currents comparison

IV. The OW-PMSM Control Method Based on PS_SPWM Scheme

With the above PS_SPWM scheme, the dominated ZSV caused by the modulation scheme can be eliminated in ideal condition, but the other ZSV disturbance sources which influence the ZSC should be considered. In this part, the ZSC closed-loop control method based on the zero voltage vectors adjustment for the proposed PS_SPWM scheme is introduced; then the corresponding OW-PMSM control method is proposed and summarized.

A. The ZSC Control Method Based on the Zero Voltage Vector Adjustment

In general, both the active and zero voltage vectors can affect the average output CMV. Based on the volt-second equivalent principle, the active voltage vectors with the corresponding dwell times are utilized to synthetize the reference voltage vector, so the dwell times of active voltage vectors are not suitable to adjust to change the average CMV. Contrary, the zero voltage vectors (000) and (111) are often utilized to fill the remaining time of the switching cycle, and the dwell times are adjustable, so the zero voltage vector

adjustment is a freedom to control the average output CMV for VSI.

For conventional SVPWM, the dwell times of two zero voltage vectors are equally divided. In order to suppress the ZSC in OW-PMSM, the dwell times of zero voltage vectors should be further adjusted in two VSIs to satisfy the requirement of reference ZSV [15][18]-[20]. Considering the PS_SPWM scheme that the two zero voltage vectors are also utilized in two VSIs, the similar method can also be implemented. Fig. 11 shows the principle and effect of zero voltage vector adjustment for the proposed PS_SPWM scheme. For example, the dwell time of zero voltage vector (111) for VSI1 is adjusted to add ΔT while the dwell time of zero voltage vector (000) is adjusted to subtract ΔT shown in Fig. 11(a), so the three-phase PWM signals change from G_{a1}, G_{b1}, G_{c1} to G_{a1}', G_{b1}', G_{c1}' which all increase the duty cycles. In this case, the dwell time of active voltage vectors keeps unchanged, while the CMV is changed from U_{cm1} to U_{cm1}' which leads to the voltage-second added. Fig. 11(b) shows the opposite situation for VSI2 which leads to the total voltage-second reduced. Fig. 11(c) shows the effect of zero voltage vectors adjustment for the output ZSV. With the switching edges adjustment for different phase-legs, the six narrow ZSV pulses can be generated with the same dwell time of ΔT.

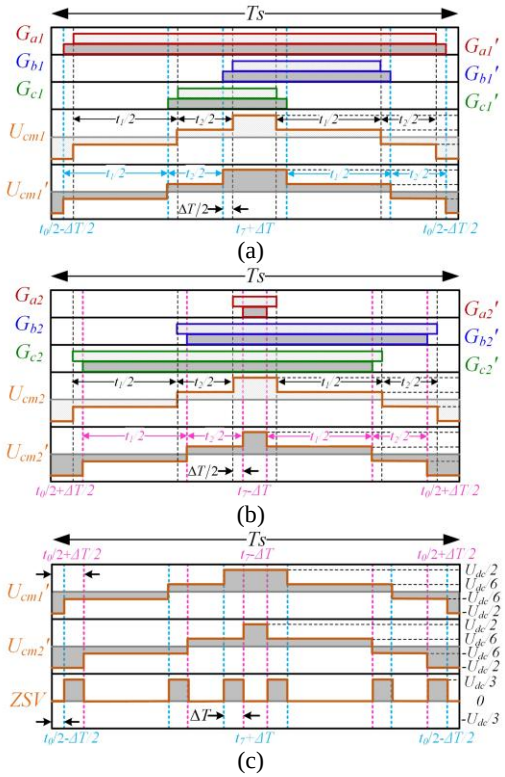


Fig. 11 The principle and effect of zero voltage vectors adjustment: (a) the zero voltage vectors adjustment for VSI1 to increase the volt-second, (b) the zero voltage vectors adjustment for VSI2 to reduce the volt-second, (c) the effect of zero voltage vectors adjustment for the output ZSV

In this case, the relationship between the output reference average ZSV and the adjusted dwell time of zero voltage vector can be deduced

$$u_{0\_ref} = 6 \times \frac{U_{dc}}{3} \times \frac{\Delta T}{T_S} = \frac{2U_{dc}\Delta T}{T_S}. \tag{25}$$

where u_{0_ref} is the output reference average ZSV, ΔT is the adjusted dwell time of zero voltage vector, and T_S is the switching cycle of PWM.

Based on the above analysis, the detailed modulation algorithm realization process can be drawn and shown in Fig. 12. After adopting the transformation *dq/abc*, the three phase voltage reference U_{a_ref}, U_{b_ref}, U_{c_ref} can be calculated and divided to the two VSIs, and the conventional symmetric SPWM scheme can be easily implemented to generate the original six modulation signals G_{a1}, G_{b1}, G_{c1}, G_{a2}, G_{b2}, G_{c2}. Thus, the phase-shift operation can be utilized and the symmetric SPWM scheme is upgraded to the asymmetric PS_SPWM scheme which can cancel out the ZSV in ideal condition. In addition, the 0-axis voltage reference U_{0_ref} generated by the ZSC controller is considered to adjust the time of zero voltage vectors with ΔT, then the final six PWM signals which drive dual VSI can be obtained with the updating the switching edges of the PWM signals.

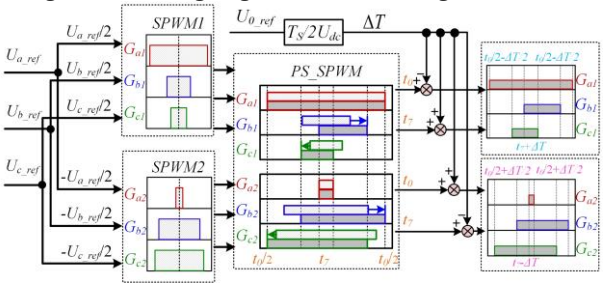


Fig. 12 The detailed modulation algorithm realization process

B. OW-PMSM Control Method Based on PS_SPWM Scheme

In order to efficiently suppress the ZSC, the closed-loop controller of ZSC should be added in the motor control system. The reference ZSC i_{0_ref} is set as zero, and the actually feedback ZSC i_0 is one third of the sum of sampled three phase currents which mainly contains triple frequency ac component, so the conventional PI controller cannot be efficaciously utilized to eliminate the tracking error. The proportional-resonant (PR) controller which the gain is large enough at selected frequency can track the actual ac trajectory and guarantee the tracking accuracy. Considering the frequency fluctuation even in steady state of motor control process, the quasi PR controller is more suitable to be implemented to guarantee the enough large gain in the near resonant frequency range. The typical transfer function quasi PR controller is shown in (26)

$$G(s) = K_p + \frac{K_r \omega_c s}{s^2 + 2\omega_c s + \omega_0^2}. \tag{26}$$

where k_p and k_r are the proportional and resonant gains of PR regulator, respectively. ω_c is the cut-off frequency, while ω_0 is the resonant frequency. In order to suppress the main triple frequency ZSC, ω_0 is selected as the third fundamental frequency, and ω_c can be selected as 2−5 rad/s [15].

With the aforementioned content, the proposed complete control method for the OW-PMSM system can be summed up

and shown in Fig. 13. The control diagram consists of one speed-loop and three current-loops, and the control strategy is similar with conventional field oriented control for conventional three-phase motor. The different part are the special designed PS_SPWM scheme and the extra ZSC closed-loop regulator. The actual speed of motor can be deduced with the encoder. The DC-link voltage and three-phase currents are sampled in real-time to provide the feedback calculating information. The q-axis reference current i_{q_ref} is given by speed error through the speed PI regulator, while the d-axis and 0-axis reference current i_{d_ref} and i_{0_ref} are directly set to be zero in general. The q-axis and d-axis feedback current (i_q, i_d) can be regulated with the corresponding PI regulator, while the 0-axis current i_0 should be regulated with the additional PR regulator to suppress the ac harmonic current.

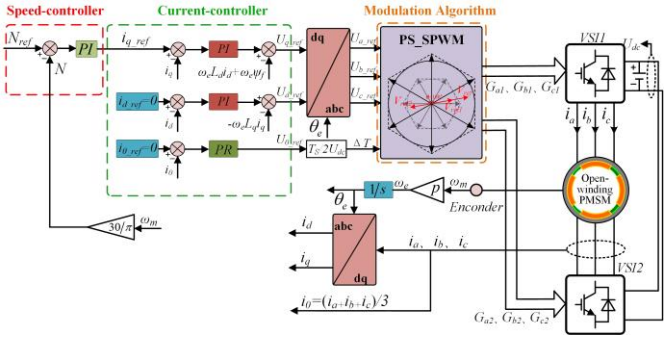


Fig. 13 The control block diagram of the OW-PMSM drive system

V. Experimental Results and Discussion

A. System Implementation

In order to verify the effect of the proposed PS_SPWM method and compare with other modulation schemes, experiments have been done in an experimental platform with a prototype 12/16 three-phase OW-PMSM shown in Fig. 14. The parameters of the machine are listed in Table. II of Appendix. The platform consists of a control board with a DSP TMS320F28335 which can generate twelve PWMs to drive dual inverter simultaneously; a power board with two integrated power modules (IPM: 6MBP20RH060, 600 V, 20 A, FUJI) which connect the common DC bus. The DC bus voltage is selected as 75V to meet the back EMF requirements. In addition, the high resolution oscilloscope Rohde & Schwarz RTE1024 with 5GSa/s sampling rate and the high bandwidth current probe RT-ZC20 are utilized to capture the date and make sure the precision of time domain waveform. The multi-channel oscilloscope Yokogawa DL850E is used to test the multi-channel signals and record the long time scale waveform. The other related equipment are used to provide the DC power and generate the braking torque.

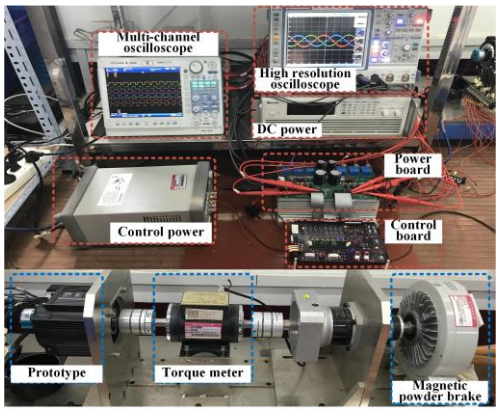


Fig. 14 Experimental platform

B. The Current Ripple Related Performance Comparison for Different Modulation Schemes

First, in order to verify the different PWM algorithms, the six PWM signals of upper switching devices for different schemes are tested and recorded by the multi-channel oscilloscope shown in Fig. 15. The 5 kHz switching frequency is selected to obtain the relatively big current ripple in phase current. In this case, the switching period for different schemes are measured to be 200μs which accords with the demand. Fig. 15(a) shows the symmetrical SPWM scheme. The PWM signals deduced two CMVs are different which can produce the high-frequency ZSV pulses. Fig. 15(b) shows the scheme of conventional SVPWM with signal rotation. In this case, the two CMVs generated by the dual inverter can be identical and keep symmetrical in one switching cycle. Fig. 15(c) gives the result of the proposed PS_SPWM scheme. It can be found that the two asymmetrical CMVs generated by the dual inverter keep identical with proper phase-shift which can cancel out the modulated ZSV disturbance source theoretically.

Based on the above modulation schemes, the performance of phase current's current ripple is first taken into consideration and make comparison. Since the fundamental current has little influence on the current ripple, the no load test of three-phase currents and ZSC at low and high rotation speeds (*i.e.* with low and high modulation index) are implemented to make clear comparison for the concerned current ripple. Fig. 16 shows the three-phase currents and ZSC at 150 RPM (round per minute) and without the ZSC closed-loop control for the three different schemes. In Fig. 16(a), the conventional SPWM scheme is utilized and obvious high frequency ZSC generates which is caused by the high frequency ZSV pulses. This high frequency ZSC which superimposes in phase current can increase the current ripple of phase current. In addition, though the conventional SPWM scheme does not produce low frequency ZSV theoretically, the low frequency ZSC (mainly the triple harmonic current) still exists in phase current which is caused by other ZSV

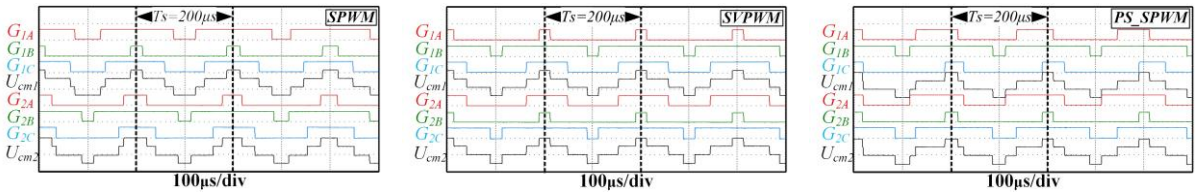


Fig. 15 The whole PWM signals of upper switching devices for different schemes: (a) the conventional SPWM scheme, (b) the conventional SVPWM with signal rotation scheme, (c) the proposed PS_SPWM scheme

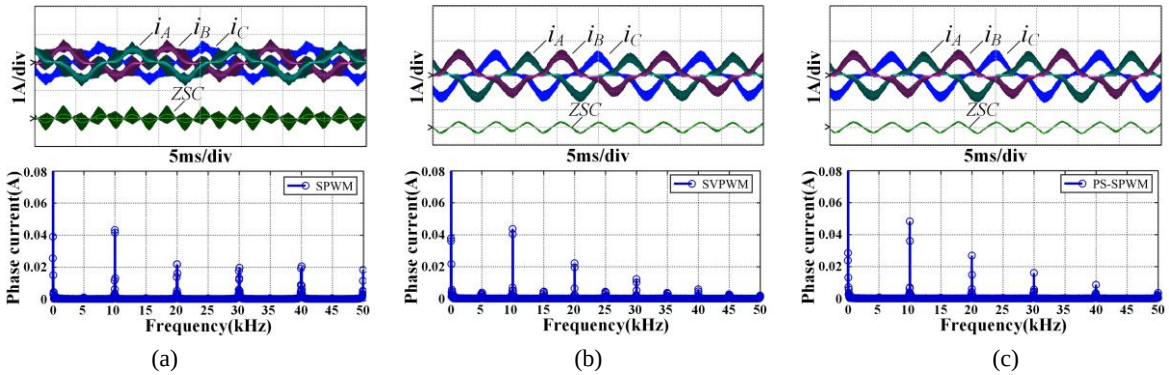


Fig. 16 The phase current and ZSC comparison for the three different schemes at 150RPM: (a) the symmetrical SPWM scheme, (b) the conventional SVPWM scheme, (c) the proposed PS_SPWM scheme

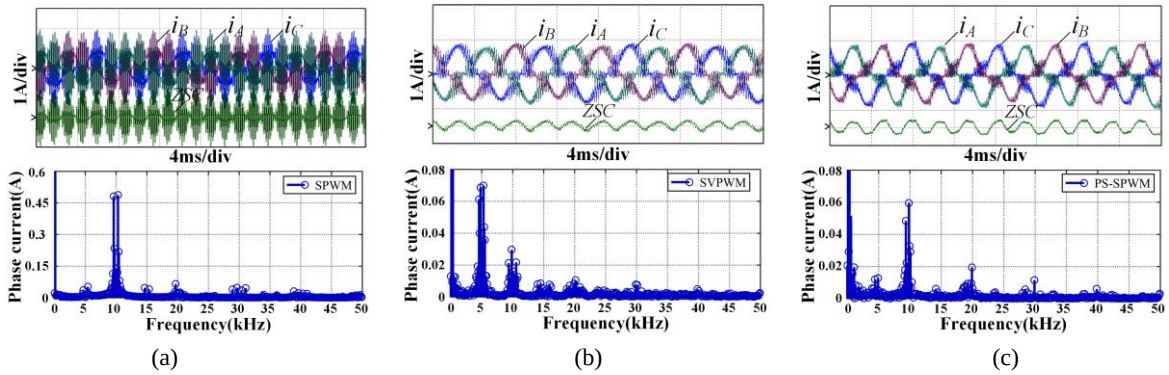


Fig. 17 The phase current and ZSC comparison for the three different schemes at 900RPM: (a) the conventional SPWM scheme, (b) the conventional SVPWM scheme, (c) the proposed PS_SPWM scheme

disturbance sources. Fig. 16(b) and (c) shows the performance of SVPWM and PS_SPWM schemes, respectively. It can be found that the high frequency ZSC is eliminated, and only low frequency triple harmonic ZSC exist in this case.

To further investigate the current ripple of different schemes, the frequency domain analysis of phase current is also implemented and shown in Fig. 16, respectively. Comparing to the conventional SVPWM scheme which both the odd and even switching harmonics exist, it can be seen that the phase current of SPWM scheme and proposed PS_SPWM scheme have the double frequency effect. Nevertheless, the high frequency ZSC superposed in phase current palpably increases the THD value for the SPWM scheme. The RMS (root mean square) value of the switching frequency current for the SPWM scheme is 0.105A, while the value is reduced to 0.075A for conventional SVPWM scheme, and the proposed PS_SPWM scheme has the minimum value of 0.073A. Since the conventional SVPWM scheme have little odd switching harmonics comparing to the even switching harmonics in low modulation index condition, the double frequency effect of the proposed PS_SPWM scheme can only reduce little RMS value which coincides with the theoretical analysis shown in Fig. 10.

Fig. 17 shows the three-phase currents and ZSC at 900 RPM for the three different schemes. In Fig. 17(a), the high frequency ZSC is further increased for the conventional SPWM scheme which lead to the fundamental current submerging by the current ripple, and the RMS value of the switching harmonics is also significantly increased to 0.838A. Fig. 17(b) and (c) show the phase current performance for the SVPWM and PS_SPWM schemes. It can be seen that the current ripple of SVPWM scheme is obviously larger than the proposed PS_SPWM scheme in time domain. The current ripple RMS value of the two modulation schemes are 0.154A and 0.107A correspondingly. This effect can be explained with the FFT analysis in frequency domain. For the SVPWM scheme, the 1st switching frequency harmonics are

dramatically increased and become the dominant part of current ripple in high modulation index. As for the proposed PS_SPWM scheme, even the 2nd switching frequency harmonics slightly increased, the amplitude is smaller than the 1st switching frequency harmonics of SVPWM scheme, and it can obviously suppress the 1st switching frequency current which finally reduce the RMS value comparing to the SVPWM scheme. The above result is also coincided with the theoretical analysis shown in Fig. 10.

To investigate the variation tendency of the high frequency current ripple RMS value for the three different schemes, the speed scan is implemented and the result is illustrated in Fig. 18. It can be seen that the conventional SPWM scheme induces the severest high frequency switching current in the whole speed range. This phenomenon is caused by the duration increase of ZSV pulses with the modulation index raise. So the conventional SPWM scheme is not suitable for the occasion of OW motor drive which does not discuss in the following content. The proposed PS_SPWM scheme can overcome the ZSV pulse induced high frequency ZSC problem, and the performance is better than the conventional SVPWM scheme in all working conditions shown in the enlarge view, especially in high speed range. For example, when the motor speed is at 900RPM, the proposed PS_SPWM scheme can decrease 30.53% of the current ripple RMS value comparing to the conventional SVPWM scheme without adding extra switching actions which show the superiority of current ripple reduction effect for the proposed PS_SPWM scheme. What's more, the tendency of curves is coincided with the theoretical calculation result shown in Fig. 10. So the proposed PS_SPWM scheme has the potential to reduce the THD of phase current when the high frequency current ripple is not negligible.

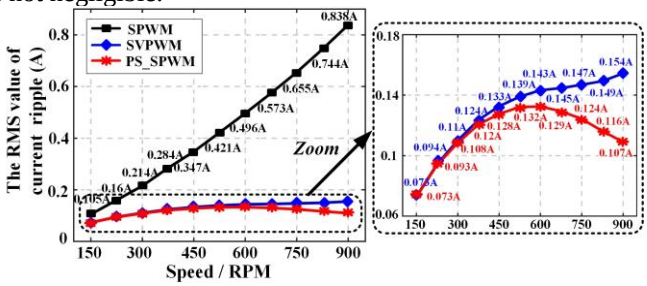


Fig. 18 The RMS value of switching frequency current ripple comparison for different schemes

Moreover, the high frequency motor vibration and acoustic noise which are important indicators in actual motor drive application are directly related to the current ripple and should be concerned. To further verify the performance of the two different schemes, the motor vibration and acoustic noise have been tested. The vibration acceleration signals are measured by the accelerometer (PCB TLD352C03) and acquired by a data acquisition module (LMS SCADAS Mobile Front-End SCM202). The frequency domain vibration result at 900 RPM is illustrated in Fig. 19. It is obvious that the vibration is mainly induced by the 1st switching frequency harmonic currents for the conventional SVPWM scheme and the maximum vibration acceleration is 0.895m/s^2, while the dominant vibration is caused by the 2nd switching frequency harmonic currents for proposed PS_SPWM scheme and the maximum vibration acceleration is reduced to 0.47m/s^2. This two vibration acceleration spectrums are both coincided with the phase current spectrum shown in Fig. 17(b) and (c) in this case. What's more, the total vibration acceleration are measured as 1.072 m/s^2 and 0.592 m/s^2 for the two different schemes. So the motor vibration can be reduced with the utilization of the proposed scheme.

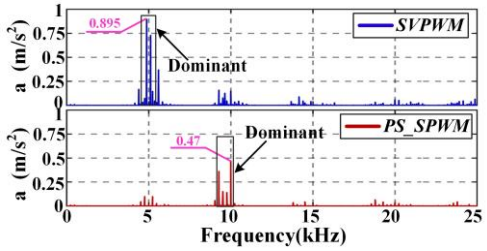


Fig. 19 The motor vibration comparison for the two different schemes at 900 RPM

In addition, the motor acoustic noise test is also implemented. The acoustic noise is measured by the noise sensor (Bruel & Kjaer Microphone Unit Type 4189-A-021), and the frequency domain performance at 900 RPM is illustrated in Fig. 20. It can be seen that the two acoustic noise spectrums are almost coincided with phase current spectrum in logarithmic coordinates and the obvious noise peak reduction can be realized for the proposed PS_SPWM scheme. Moreover, the weighted acoustic noise are calculated as 72.52 dB(A) and 66.1 dB(A) for the two methods which means the proposed PS_SPWM scheme can reduce the weighted acoustic noise to 22.81% of the conventional SVPWM scheme. So obvious acoustic noise performance improvement can be realized which is advantageous in actual application occasions.

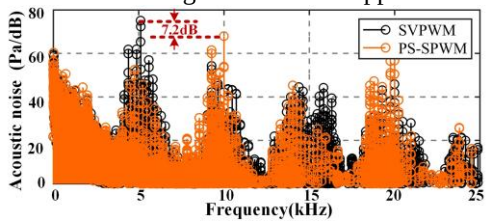


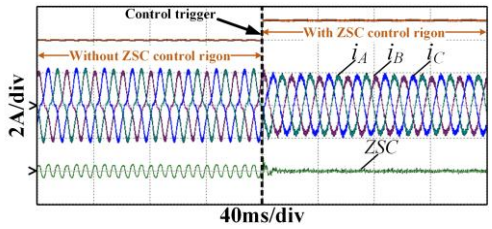
Fig. 20 The motor acoustic noise comparison for the two different schemes at 900 RPM

From the above experimental comparison, it can be seen that the PS_SPWM scheme has better performance comparing to the conventional SVPWM scheme, including the current ripple reduction, the motor vibration and the acoustic noise suppression. So the PS_SPWM scheme can relieve the current ripple related adverse effect and improve the corresponding performance of motor drive.

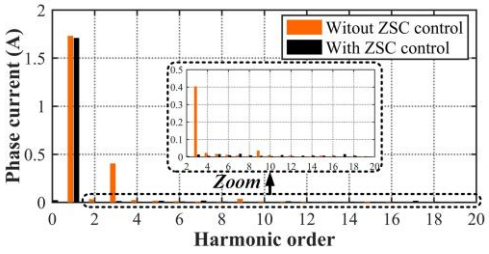
C. Current Control Performance Comparison for Different Modulation Schemes

In this part, the switching frequency is increased to 10 kHz to obtain the fast and accurate control performance. In order to verify the low frequency ZSC suppression effect for the proposed PS_SPWM scheme, Fig. 21 shows the dynamic

process from the condition of without ZSC control to with ZSC control at 0.375 rated speed and 0.2 load. From Fig. 21(a), it can be seen that though the proposed PS_SPWM scheme can eliminate the modulated ZSV disturbance source, the phase current still takes a rich content of triple harmonics without the ZSC control. This phenomenon is owing to that others ZSV disturbance sources induce the ZSC current. Without ZSC control, the peak value of phase current reaches 2.3A, and the ZSC's peak value is 0.4A. After adding the ZSC closed-loop control, the peak value of phase current is reduced to 1.9A, and the ZSC's peak value is less than 0.1A. So the proposed ZSC closed-loop control can effectively suppress the ZSC and reduce the peak value of phase current. With the FFT analysis for the phase current shown in Fig. 21(b), the THD of phase current is 24.1% without the ZSC control, while it can be reduced to 6.09% with the ZSC control. As for other triple harmonics, like the 9th and 15th harmonics, the amplitude are small enough to be neglected.



(a)



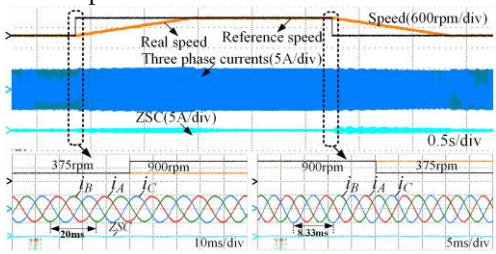
(b)

Fig. 21 The current waveform for the proposed PS_SPWM method: (a) the dynamic process from without ZSC control to with ZSC control, (b) the frequency domain analysis

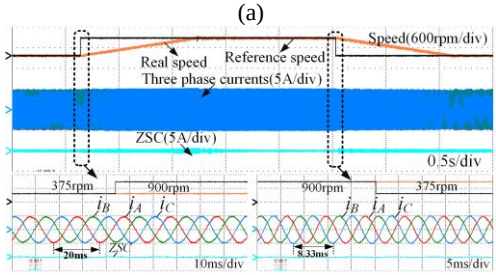
Moreover, to further verify the dynamic response for the proposed PS_SPWM scheme and compare with the conventional SVPWM scheme, the speed step experiments have been done, and the experimental results are shown in Fig. 22(a) and (b). It can be seen that the proposed PS_SPWM scheme has nearly identical performance comparing to the conventional SVPWM scheme under the same control condition. The ZSC can be well suppressed in different rotation speed and the phase current can keep sinusoidal in this case.

Finally, the torque variation experiments have been done to verify the current dynamic response for the two schemes. The experimental results of torque variation process are shown in Fig. 23(a) and (b) for the two schemes. It can be seen that the proposed PS_SPWM scheme has similar current regulation performance comparing to the conventional SVPWM scheme with the same control parameter. The phase current can also keep sinusoidal and the ZSC can be well suppressed with different output torque whether in steady state or dynamic process.

Considering the experimental results of Fig. 22 and Fig. 23, it can be seen that the proposed PS_SPWM scheme has no performance degradation comparing to the conventional SVPWM scheme which is owing to that the proposed scheme only optimize the current ripple and has no influence on the fundamental output current.

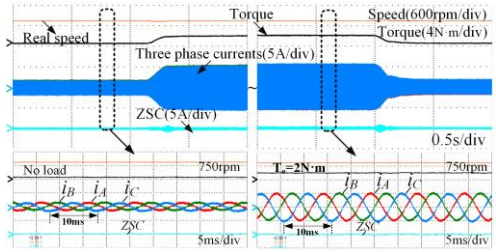


(a)

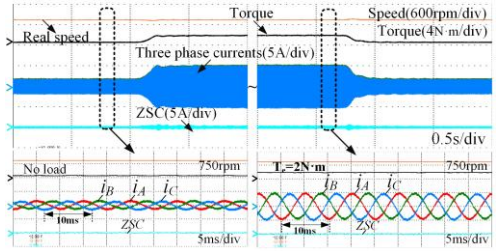


(b)

Fig. 22 The speed step experiments for the conventional SVPWM and the proposed PS_SPWM methods: (a) the conventional SVPWM method, (b) the proposed PS_SPWM method



(a)



(b)

Fig. 23 The torque variation experiments for the conventional SVPWM and the proposed PS_SPWM methods: (a) the conventional SVPWM method, (b) the proposed PS_SPWM method

VI. Conclusions

This paper introduces a novel PS_SPWM scheme for OW-PMSM fed by two VSIs with the common DC bus. The proposed PS-SPWM method is based on the adjustment of

location of voltage pulses in two inverters. Only by conventional SPWM scheme associated with suitable phase-shift, the dominated ZSV disturbance source of inverter can be eliminated in ideal condition. The following conclusions can be derived:

1. The zero sequence impedance of the OW-PMSM is often with small value because of the weaken effect by mutual inductance. Without control of ZSV, obvious ZSC can be found in the motor and brings corresponding problems. The proposed PS_SPWM method can help to cancel the modulated ZSV disturbance source.
2. The proposed PS_SPWM scheme has the same DC bus utilization with conventional SVPWM scheme regardless the principle difference.
3. The proposed PS_SPWM scheme can fully utilize the freedom of dual inverter and maintain the double frequency effect which can almost eliminate the odd switching frequency harmonics in phase current and reduce the high frequency current ripple. Meanwhile, the motor vibration and acoustic noise can be suppressed.
4. After adding the ZSC regulator in the control system for the proposed PS_SPWM scheme, the ZSC can be obviously suppressed whether in steady state and dynamic process which has similar performance comparing to conventional SVPWM scheme.

The experimental results show that the proposed method is effective to be utilized in the dual inverter fed OW-PMSM with common DC bus and has better performance comparing to the conventional SVPWM scheme.

APPENDIX

TABLE II
PARAMETERS OF THE PROTOTYPE OW-PMSM

Parameters	Value
PM flux linkage	0.023Wb
stator inductance	2.4mH
Phase resistance	0.3Ω
Rated rotation speed	1000RPM
Rated fundamental frequency	133.3Hz
Rated line voltage	150V
Rated line current	8.5A
Rated torque	8.3Nm

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Zewei Shen (S'17) was born in Hubei, China, in 1990. He received the B.S. degree in automation from the Department of Automation, Huazhong University of Science and Technology, Wuhan, China, in 2012. He is currently working toward the Ph.D. degree in electrical engineering at Huazhong University of Science and Technology, Wuhan, China.
His current research interests include paralleled converters and high power density motor drive.

Dong Jiang (S05'-M12'-SM16') received B.S and M.S degrees in Electrical Engineering from Tsinghua University, Beijing, China, in 2005 and 2007 respectively. He received his PhD degree in University of Tennessee in Dec. 2011. He was with United Technologies Research Center (UTRC) in Connecticut as a Senior Research Scientist/Engineer from Jan 2012 to July 2015. He has been with Huazhong University of Science and Technology (HUST) in China as a professor since July 2015. Dong Jiang's major research area is power electronics and motor drives, with more than 40 published IEEE journal and conference papers in this area. He has two best paper awards in IEEE conferences. He is an associate editor of IEEE Transactions on Industry Applications.

Lei Zhu (S'17) received B.S degree in Electrical and Electronic Engineering from Huazhong University of Science and Technology, Wuhan, China, in 2017. He is currently working toward the M.S degree in Electrical and Electronic Engineering at Huazhong University of Science and Technology, Wuhan, China.
His current research interests include power hardware in-the-loop simulation and motor control.

Yunsong Xu (S' 18) received the B.S. degree in Electrical Engineering from Southwest Jiaotong University, Chengdu, China in 2018. He is currently working towards the M.S. degree in Electrical Engineering at the Huazhong University of Science & Technology, Wuhan, China.
His current research interests include the vibration and noise of electric machines.

Tianjie Zou (S'15-M'18) was born in Hubei, China, in 1991. He received the B.Sc. degree in 2013 in electrical and electronic engineering, and Ph.D. degree in electrical engineering in 2018, both from Huazhong University of Science and Technology, Wuhan, China. He joined the University of Nottingham, U.K. in 2018, and is currently working as a research fellow within the Power Electronics, Machines and Control (PEMC) Group.
His main research interests include design, analysis, and intelligent control of permanent-magnet machines. Dr. Zou was the recipient of the Best Paper Award in the 22nd International Conference on Electrical Machines (ICEM 2016).

Zicheng Liu (M'18) was born in Shandong, China, in 1989. He received the B.S. degree in Hydropower Engineering from Huazhong University of Science and Technology (HUST), Wuhan, China, in 2011, and the Ph.D. degree in Electrical Engineering from Tsinghua University, Beijing, China, in 2016. During Otc. 2014 to Mar. 2015, he was a Visiting Student at Purdue University, West Lafayette, IN, USA. During Jun. 2016 to Sep. 2018, he was a postdoc researcher at Beijing Jiaotong University, Beijing, China. He is currently an associate professor at HUST. His research interests include multiphase motor control systems and transportation electrification.

Ronghai Qu (S'01–M'02–SM'05–F'18) was born in China. He received the B.E.E. and M.S.E.E. degrees in electrical engineering from Tsinghua University, Beijing, China, in 1993 and1996, respectively, and the Ph.D. degree in electrical engineering from the University of Wisconsin-Madison, in 2002. In 1998, he joined the Wisconsin Electric Machines and Power Electronics Consortiums as Research Assistant. He became a Senior Electrical Engineer with Northland, a Scott Fetzer Company in 2002. Since2003, he had been with the General Electric (GE) Global Research Center, Niskayuna, NY, as a Senior Electrical Engineer with the Electrical Machines and Drives Laboratory. He has authored over 50 published technical papers and is the holder of over 40 patents/patent applications. From 2010, he has been a professor with Huazhong University of Science &Technology, Wuhan, China. Prof. Qu is a full member of Sigma Xi. He has been the recipient of several awards from GE Global Research Center since 2003, including the Technical Achievement and Management Awards. He also is the recipient of the 2003 and 2005 Best Paper Awards, third prize, from the Electric Machines Committee of the IEEE Industry Applications Society at the 2002 and2004 IAS Annual Meeting, respectively.