Unified Cost Function Model Predictive Control for a three-stage Smart Transformer

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Abstract— The massive integration of power electronics-based renewable energy sources has profoundly changed the electrical grid. In this scenario, the smart transformer, which is a solid-state transformer with advanced control and communication features, has been proposed as one of the solutions to offer new grid services, while mitigating electrical grid issues, including voltage/frequency disturbance, harmonics, voltage instability, and to pave the way towards dc grids. The commonly proposed topology for ST is the three-stage ac-dc-dc-ac converter, due to the availability of the dc link at both medium- and low-voltage sides. The control design usually relies on the well-known techniques of pole/zero placement and each conversion stage is considered separately. This paper proposes a unified predictive control of the three stages of the ST that allows to control all the variables with a single cost function. Simulation results show the effectiveness of the proposed solution in guaranteeing excellent current tracking performance and good disturbance rejection.

Keywords—predictive control, solid state transformer, dc microgrids, smart transformer

I. INTRODUCTION

The recent advances in the electrical and electronics engineering fields have drastically changed the devices connected to the electrical grids. Renewable energy exploitation, especially PV and large on- and off-shore wind farms, electric vehicle charging stations and power electronics interfaced electrical machines are nowadays widespread and their number and power has been increasing. Due to this high penetration of power electronics interfaced load and system with reduced inertia, issues within the electrical grid are increasing [1]: voltage and frequency violations, harmonics, over/under frequency leading to blackouts etc. Among the proposed technologies to address the aforementioned problems, the Smart Transformer [2] is a key actor. The Smart Transformer does not simply act as a replacement of the conventional medium-to-low voltage distribution transformer, adapting the voltage from medium- to low-voltage, but it offers additional services, upgrading the power distribution with more controls and communication elements.

In addition to performing voltage/frequency control [3], the ST can offer dc connectivity for medium- and low-voltage grids, loop connection of parallel ac grids [4], as well as offering a series of grid identification [5] and support services. Classical control schemes for ST considers the independent control of each conversion stage (i.e., ac-dc, dc-dc, dc-ac). In the current literature [6], these stages are controlled applying the classical linear control theory, that involves the use of static or rotating reference systems with controllers, such as proportional-integral or proportional-resonant ones. Although these controllers offer simple tuning and well-known stability-assessment tools, they cannot optimize the overall control performance of the ST, due to the independent tuning of each stage.

At the same time, predictive control is often considered for power converters considering the several advantages it can provide such as high bandwidth, inclusion of non-linearities and constraints, straightforward digital implementation. Among the several MPC techniques that have been proposed, Finite Control Set Model-Predictive-Control (FCS-MPC) is often considered in power electronics, as an example for AC/DC, DC/AC and AC/AC power conversion [7]–[12]. However, FCS-MPC is rarely applied to DC/DC power converters which are often present in the isolation stage of a ST. Between the few reported application of FCS-MPC in DC/DC power conversion, the MDCS-MPC technique is proposed for use in the boost converter with receding horizon [13], [14] where it demonstrated fast dynamics.

This paper deals with an optimized control structure of a three-stage smart transformer, applying a predictive control paradigm for the whole ST structure. In contrast with the conventional approached that considers standard regulators and separate control structure, the proposed one (presented in [15] for two stages) allows with a single cost function to control all the AC (medium- and low-voltage) and DC variables in the ST structure.

II. SMART TRANSFORMER: TOPOLOGY MODELLING AND CONTROL TARGETS

The basic structure of a three-stage ST is depicted in **Error! Reference source not found.**, where a three-stage architecture is shown [16]. A basic control structure implies:

1. The MV stage implements a current controller for the MV ac grid (and the active/reactive power) as well as the MV dc link.
2. The dc-dc converter controls the power flow from MV to LV and the LV dc link
3. The LV dc-ac stage controls the LV ac voltage.

Depending on the specific topology, additional controls as the cell balancing [17] should be considered. At higher level, a series of ancillary controls [2], [16], [18], which include reverse power flow control, load identification, storage control, harmonics suppression and constant power load instability mitigation, have been proposed. The proposed control consists in a Finite Control Set Model Predictive Control (FCS-MPC) control for the for the ST power conversion system in a single control loop, comprising an unified cost function which control the power flow and regulate the inner DC voltage. As a term of comparison, a classical PI control implementation from the ST under exam is also described.

In this section, the design process of current controller and voltage controller for the ST is presented. Considering that the filter of grid-connected inverter has inductance of L_f and resistance of R_f, the admittance of filter can be given as

$$G_f(s) = \frac{1}{L_f s + R_f} \tag{1}$$

The current controller can be expressed as

$$G_c(s) = k_{pc} + \frac{k_{ic}}{s} = \frac{k_{pc}s + k_{ic}}{s} \tag{2}$$

where k_{pc} and k_{ic} are the proportional gain and integral gain. Then, the transfer function of current control loop can be given as

$$G_{c,cl}(s) = \frac{G_c(s)G_f(s)}{G_c(s)G_f(s)+1} = \frac{\frac{k_{pc}s+k_{ic}}{L_f s+R_f}}{\frac{k_{pc}s+k_{ic}}{L_f s+R_f}+s} \tag{3}$$

It is easy to observe that the above transfer function is first-order. Hence, by canceling the poles and zeros in numerator and denominator, the equation can be simplified as

$$G_{c,cl}(s) = \frac{\omega_c}{\omega_c+s} = \frac{1}{1+s/\omega_c} \tag{4}$$

where ω_c is the desired bandwidth of current controller. The parameters of current controller can be determined as

$$G_c(s) = k_{pc} + \frac{k_{ic}}{s} = \omega_c L_f + \frac{\omega_c R_f}{s} \tag{5}$$

The voltage controller can be expressed as
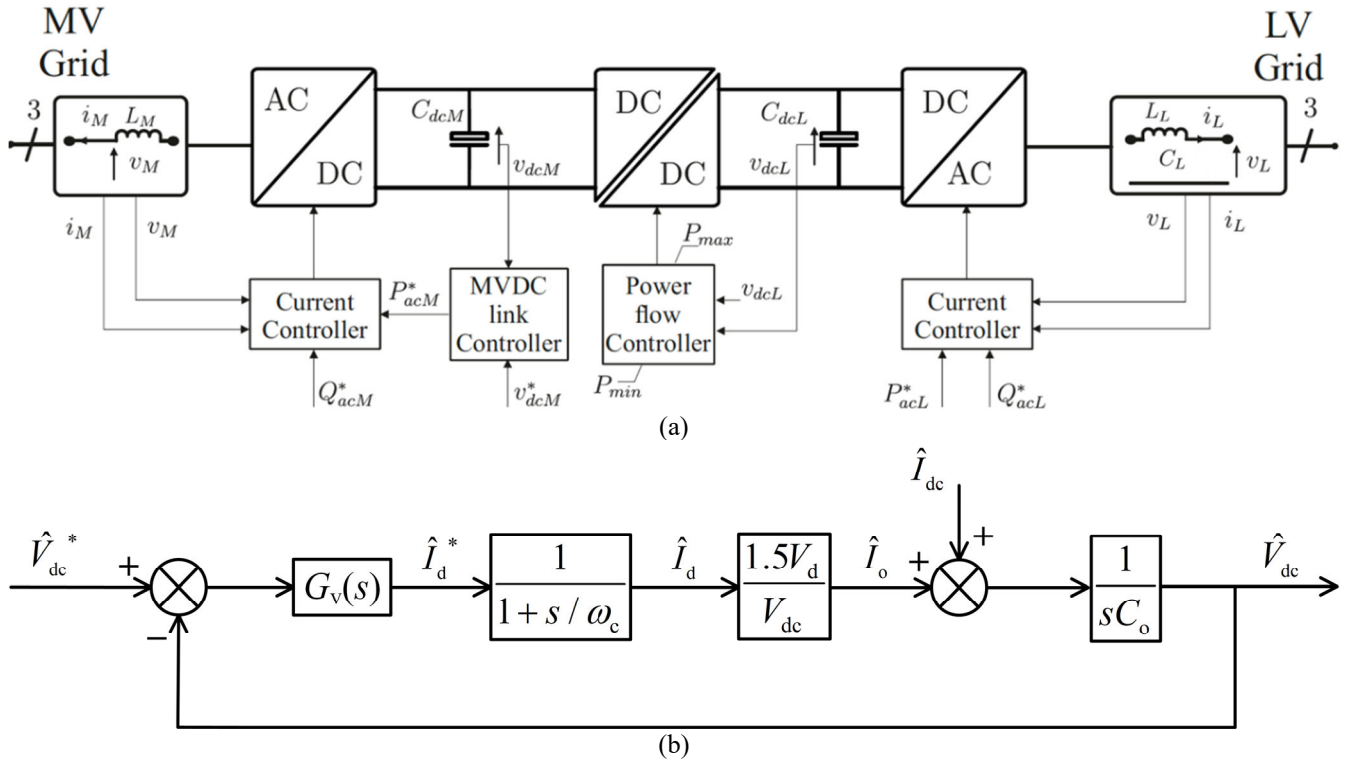
$$G_v(s) = k_{pv} + \frac{k_{iv}}{s} \tag{6}$$

Fig. 1. Conventional control of the ST. Block scheme of the separate controls of each stage (a). Equivalent block diagram for the voltage control of the MV stage (b).

The transfer function block scheme of voltage control loop is shown as Fig. 1. The open loop gain of voltage control can be obtained as

$$G_{v,ol}(s) = \frac{1.5V_d k_{iv}}{V_{dc}C_o} \frac{\frac{k_{pv}}{k_{iv}}s+1}{s^2(1+s/\omega_c)} = A\frac{\frac{k_{pv}}{k_{iv}}s+1}{s^2(1+s/\omega_c)} \qquad (7)$$

where A represents the control gain. In this case, the technique of symmetrical optimum [17] can be used to maximize the phase margin of open loop gain, the frequency at maximum phase margin can be given as

$$\omega_o = \sqrt{\omega_c \omega_v} \qquad (8)$$

where ω_o is the frequency at maximum phase margin, ω_v is the desired bandwidth of voltage controller. Considering that the open loop gain will be unity at ω_o, it exists

$$|G_{v,ol}(\omega_o)| = 1 = \frac{A}{\omega_c \omega_v}\sqrt{\frac{1+\frac{\omega_c}{\omega_v}}{1+\frac{\omega_v}{\omega_c}}} \qquad (9)$$

Hence, the integral gain of voltage controller can be calculated as

$$k_{iv} = \frac{V_{dc}C_o}{1.5V_d}\omega_v\sqrt{\omega_c \omega_v} \qquad (10)$$

and the proportional gain of voltage controller can be calculated as

$$k_{pv} = k_{iv}/\omega_v = \frac{V_{dc}C_o}{1.5V_d}\sqrt{\omega_c \omega_v} \qquad (11)$$

Several proposals for the dc-dc converter for smart transformer applications can be found in the scientific literature. Among the most adopted ones, the Dual Active Bridge (DAB) converter, proposed in [19] and the LLC Series Resonant Converter (recent ST applications in [20], [21]) are of great interest due to the soft-switching characteristics and, especially the DAB, the ease of implementation of the power flow control. Extensions of these topology to multi-port structures have also been proposed for ST applications, allowing to increase the fault tolerance and implement advanced thermal management [22], [23].
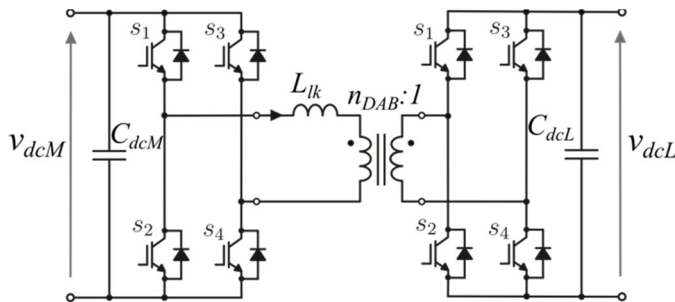

Fig. 2.   Circuit diagram of the DAB

Considering the intrinsic bi-directional operation of the ST, the focus of this paper will be on the DAB-type converters, whose circuit diagram is shown in Fig. 2. The single-phase DAB will be considered for simplicity's sake, although the three-phase solution [19] would be beneficial in terms of power density.

The main assumption is to consider the linearized model of the DAB operated under the single-phase shift modulation, reported in Fig. 3.
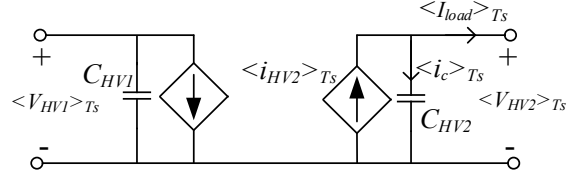

Fig. 3.   The averaged model of a DAB converter

It can be seen that the power processed by the DAB follows a non-linear dependency on the phase shift between the two square-wave signals generated by the two H-bridges (d is the phase shift angle normalized to 2π) and is related to the medium- and low-voltage dc links (V_{dcM} and V_{dcL}), the transformer turn ratio n, the switching frequency f_{sw-DAB} and the transformer series inductance L_{lk}.

$$P_{DAB} = \frac{nV_{dcM}V_{dcL}}{f_{sw-DAB}L_{lk}}d(1-2|d|) \qquad (12)$$

Once the characteristic of the DAB power transfer is linearized, the same tuning procedure for the voltage control of the MV stage can be followed, considering $\omega_c = 2\pi f_{sw-DAB}$ and substituting the converter gain with equation (12) linearized around d_0, i.e.

$$\frac{1.5V_d}{V_{dc}} = \frac{nV_{dcM}V_{dcL}}{f_{sw-DAB}L_{lk}}(1-4|d_0|) \qquad (13)$$

III. Unified FCS-MPC for the ST

The proposed control structure is shown in Fig. 4, where the control variables are the active and reactive power in the MV and LV grids and the dc link voltages. The active rectifiers have a similar control, and the possible states are the voltage space vectors (SVM_i) that can be applied by the dc-ac converters. For the sake of simplicity, two-level converters are considered, although this can be extended to more levels. The dc-dc converter considered is a Dual Active Bridge (DAB) and its predictive control is based on the discretization to finite states of the phase shift d [13], [24]. It is to be noted that only one of the active power references P^*_{acM} or P^*_{acL} can be controlled independently, since the active power flow through the ST (considering both dc grids and ac grids) must sum to zero. It is considered in the following that the independent variable is the active power reference in the LV side $P^*_{acL.}$.

The ST AC interfaces control the ac currents, in amplitude and phase and contribute to the DC voltage control considering the formulation in [25], [26].
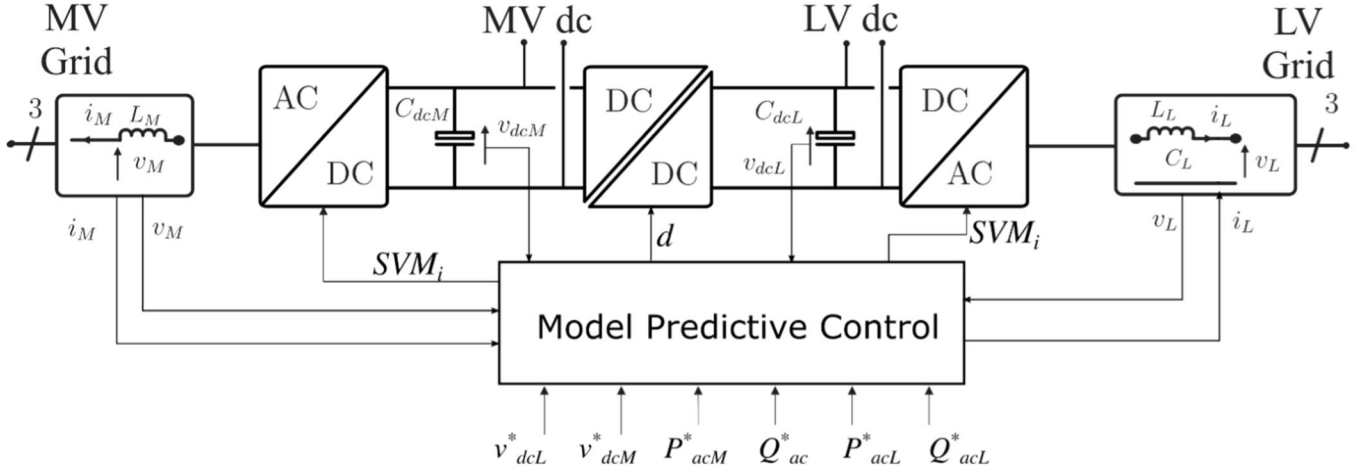
Fig. 4. Proposed predictive control control of the ST.

Firstly, the active and reactive power on both MV and LV ST AC interfaces are calculated as follows

$$P_{acM}(t) = v_{aM}(t)i_{aM}(t) + v_{bM}i_{bM}(t) + v_{cM}i_{cM}(t) \quad (14)$$

$$Q_{acM}(t) = \frac{1}{\sqrt{3}}[v_{bcM}(t)i_{aM}(t) + v_{caM}(t)i_{bM}(t) + v_{abM}(t)i_{cM}(t)] \quad (15)$$

$$P_{acL}(t) = v_{aL}(t)i_{aL}(t) + v_{bL}i_{bL}(t) + v_{cM}i_{cL}(t) \quad (16)$$

$$Q_{acL}(t) = \frac{1}{\sqrt{3}}[v_{bcL}(t)i_{aL}(t) + v_{caL}(t)i_{bM}(t) + v_{abL}(t)i_{cL}(t)] \quad (17)$$

where the AC currents and voltages are directly measured, using delta-star equations if necessary to obtain the line to neutral voltages. For control design purposes the AC voltages are discretized and predicted using a first order Lagrange extrapolator:

$$v_i(k + n) = 2v_i(k + n - 1) - v_i(k + n - 2) \\ i = aM, bM, cM, aL, bL, cL \quad (18)$$

A classical two-level three-phase converter is considered for the AC interfaces. In case multilevel topologies are considered, the control has to be modified accordingly. In the case under study the active and reactive power predictions can be calculated from (14)-(17) considering the voltage predictions of (18) and the following current predictions:

$$i_{aM}(k + 1) = K_1[s_{aM}(k)V_{dcM}(k) - v_{aM}(k)] + K_2 i_{aM}(k) \\ i_{bM}(k + 1) = K_1[s_{bM}(k)V_{dcM}(k) - v_{bM}(k)] + K_2 i_{bM}(k) \quad (19) \\ i_{cM}(k + 1) = K_1[s_{cM}(k)V_{dcM}(k) - v_{cM}(k)] + K_2 i_{cM}(k)$$

$$i_{aL}(k + 1) = K_3[s_{aL}(k)V_{dcM}(k) - v_{aL}(k)] + K_4 i_{aL}(k) \\ i_{bL}(k + 1) = K_3[s_{bL}(k)V_{dcM}(k) - v_{bL}(k)] + K_4 i_{bL}(k) \quad (20) \\ i_{cL}(k + 1) = K_4[s_{cL}(k)V_{dcM}(k) - v_{cL}(k)] + K_2 4_{cL}(k)$$

where K_1, K_2, K_3 and K_4 are constants dependent of the sampling time Ts and the filter parameters on the LV and MV interfaces:

$$K_1 = \frac{T_s}{L_M} \quad , \quad K_2 = 1 - \frac{R_M T_s}{L_M} \quad (21)$$

$$K_3 = \frac{T_s}{L_L} \quad , \quad K_4 = 1 - \frac{R_L T_s}{L_L} \quad (22)$$

Similarly, the DC voltage equation can be derived by the MV and LC capacitor equations when a parallel load is considered on both DC/DC converter sides, R_{dcM} and R_{dcL}, respectively:

$$V_{dcM}(k + 1) = K_5 V_{dcM}(k) + K_6[i_{dabM}(k) + \sum_{i=a,b,c} s_{iM}(k)i_{iM}(k)] \quad (23)$$

$$V_{dcL}(k + 1) = K_7 V_{dcL}(k) + K_8[-i_{dabL}(k) + \sum_{i=a,b,c} s_{iL}(k)i_{iL}(k)] \quad (24)$$

$$K_5 = 1 - \frac{T_s}{R_{dcM}C_{dcM}} \quad , \quad K_6 = \frac{T_s}{C_{dcM}} \quad (25)$$

$$K_7 = 1 - \frac{T_s}{R_{dcL}C_{dcL}} \quad , \quad K_8 = \frac{T_s}{C_{dcL}} \quad (26)$$

It is worth mentioning that these equations can be iterated to get the prediction at a desired time instant. The DAB, of which its schematic is shown in Fig. 3, using the currents, i_{dabM} and i_{dabL}, which can be derived from its linearized converter model of Fig. 3 as follows, when Single Phase Shift (SPS) modulation is considered [27]:

$$i_{dabM}(k) = \begin{cases} \frac{V_{dcL}(k)}{f_{sw-DAB}L_{lk}}d(k)[1 - d(k)], & -0.5 \le d(k) < 0 \\ \frac{V_{dcM}(k)}{f_{sw-DAB}L_{lk}}d(k)[1 + d(k)], & 0 \le d(k) \le 0.5 \end{cases} \quad (27)$$

$$i_{dabL}(k) = \begin{cases} \frac{V_{dcL}(k)}{f_{sw-DAB}L_{lk}}d(k)[1 - d(k)], & -0.5 \le d(k) < 0 \\ \frac{V_{dcM}(k)}{f_{sw-DAB}L_{lk}}d(k)[1 + d(k)], & 0 \le d(k) \le 0.5 \end{cases} \quad (28)$$

where d is the phase shift between primary and secondary transformer waveform, normalized between -0.5 and 0.5, as shown in Fig.5.

In order implement the control of the DAB in an FCS-MPC fashion, the phase shift is quantized as follows

$$d(k) = d(k - 1) \pm i\Delta \quad , \quad i = -\gamma, \dots, 0, \dots, \gamma \quad (29)$$

with λ being a tuning parameter, which represents the number of values to evaluate at each control iteration. Moreover,

the step of the phase-shift Δ is adaptive, according to the distance from the actual voltage value and the reference one.

$$\Delta = \begin{cases} \Delta_{min}[1 + \lambda(v_{dcL}{}^* - v_{dcL}(k))] & , v_{dcL}{}^* - v_{dcL}(k) \leq V_{max} \\ \Delta_{min}[1 + \lambda V_{max}] & , v_{dcL}{}^* - v_{dcL}(k) > V_{max} \end{cases} \quad (30)$$

A minimum phase shift variation, Δ_{min}, is defined as well as the maximum voltage variation in one sampling interval, V_{max}. More details of the implementation are given in [13], [27].

The proposed control then evaluates all the possible two-level converter states and values of phase shift under consideration and apply for the whole sampling intervals the solution which minimizes the following cost function:

$$G = G_{acM} + G_{acL} + w_{DAB}G_{DAB} + \alpha_1 G_{dc1} + \alpha_2 G_{dc2} \quad (31)$$

which is composed of several terms. The first two terms, G_{acM} and G_{acL}, regulates active and reactive power flow through the ST to desired values:

$$G_{acM} = \sqrt{[P_{acM}(k + 2) - P_{totM}^*]^2 + [Q_{acM}(k + 2) - Q_{acM}^*]^2} \quad (32)$$

$$G_{acL} = \sqrt{[P_{acL}(k + 2) - P_{acL}^*]^2 + [Q_{acL}(k + 2) - Q_{acL}^*]^2} \quad (33)$$

On the other hand, the term G_{DAB} regulate the active power flow through the DAB to the desired reference:

$$G_{DAB} = \sqrt{[v_{dcL}(k + 2)i_{DAB-L}(k + 2) - P_{DAB}^*]^2} \quad (34)$$

Finally, the terms G_{dc1} regulates the DC voltage on both MV and LV DC-Links to the desired value

$$G_{dc1} = w_{dcM}[v_{dcM}(k + 2) - v_{dcM}(k + 2)]^2$$
$$+ w_{dcL}[v_{dcL}(k + 2) - v_{dcL}(k + 2)]^2 \quad (35)$$

while G_{dc2} limits the variation of voltage in one sampling interval:

$$G_{dc2} = w_{dcM}[v_{dcM}(k + 2) - v_{dcM}^*]^2$$
$$+ w_{dcL}[v_{dcL}(k + 2) - v_{dcL}^*]^2 \quad (36)$$

In order to evaluate the cost function in (31) proper reference values must be derived. In fact, while reactive power reference can be chosen freely by the user, the active power references must balance the power flowing through the ST. In particular the power necessary to keep the DC voltage on the MV and LV side respectively are defined as follows:

$$P_{dcM}^*(k) = \frac{1}{2}\frac{C_{dcM}}{KT_s}\left[V_{dcM}^2(k) - V_{dcM}^{*2}(k)\right] - \frac{V_{dcM}^2(k)}{R_{dcM}} \quad (37)$$

$$P_{dcL}^*(k) = \frac{1}{2}\frac{C_{dcL}}{KT_s}\left[V_{dcL}^2(k) - V_{dcL}^{*2}(k)\right] - \frac{V_{dcL}^2(k)}{R_{dcL}} \quad (38)$$

and the medium voltage active power reference is defined as the sum of the active power consumed by the MV loads, LV loads and the DC-Link as follows:

$$P_{totM}^* = P_{acM}^* + P_{dcM}^*(k) + P_{acL}^* \quad (39)$$

Finally, the DAB active power reference is set to be equal to the power necessary on the LV ST side as follows:

$$P_{DAB}^* = P_{acL}^* + P_{dcL}^*(k) \quad (340)$$

IV. RESULTS

A simulation has been run to show the effectiveness of the proposed control. The parameters are listed in Table I. and the simulation results are given in Fig. 5, Fig. 6 and Fig. 7 for the MV side, LV side and DAB converter, respectively.

TABLE I.   SIMULATION PARAMETERS

Parameter	Symbol	Value	Unit
Medium Voltage Filter Inductance	L_M	10	mH
Medium Voltage Filter Resistance	R_M	0.05	W
Low Voltage Filter Inductance	L_L	10	mH
Low Voltage Filter Resistance	R_L	0.05	W
MV ac-dc converter rated Power	P_M	500	kW
MV ac-dc converter equivalent switching frequency	f_{sw-M}	10	kHz
MV line-to-neutral RMS voltage	v_M	1700	V
MV Voltage Control – Proportional Gain	K_{p-M}	10	
MV Voltage Control – Integral Gain	K_{i-M}	3000	
Dc-dc Control – Proportional Gain	K_{p-L}	0.02	
Dc-dc Control – Integral Gain	K_{iLM}	10	
MV dc rated voltage	V_{dcM}	4500	V
LV dc rated voltage	V_{dcL}	750	V
DAB Leakage Inductance	L_{lk}	300	mH
DAB Transformer Turn Ratio	n_{DAB}	6	
DAB Switching Frequency	f_{sw-DAB}	10	kHz
MV dc link capacitance	C_{dcM}	11	mF
LV dc link capacitance	C_{dcL}	3.3	mF
Predictive control weight (MV dc link)	w_{dcM}	50	
Predictive control weight (LV dc link)	w_{dcL}	10	
Predictive Control weight (DAB)	w_{DAB}	1000	
DC power reference delay (active rectifier)	K	25	
Predictive Control weight (DAB)	α_1	10	
Predictive Control weight (DAB)	α_2	50	
Minimum value of discretized phase shift (DAB)	Δ_{min}	50e-6	
Maximum variation of voltage in one sampling interval (DAB)	V_{max}	1000	
Adaptive phase shift step tuning parameter (DAB)	λ	1	
Number of phase shift steps, ±, evaluated at each sampling interval (DAB)	γ	1	

It is assumed that ideal constant power loads are connected to the dc lines and the result on the system performance is discussed. Both the ac current tracking performance and the dc bus will be analyzed. As the set of parameters, the active rectifier has been size for 500 KVA, of which 400 kW maximum for the MV dc line and 200 kW for the LV dc line. A sizeable value of the MV dc capacitor has been chosen for the MV side, to take into account that this converter would need to perform some services, as reverse power flow prevention, harmonic/unbalance stabilization and voltage sag ride through, so enough energy storage is envisaged [2].
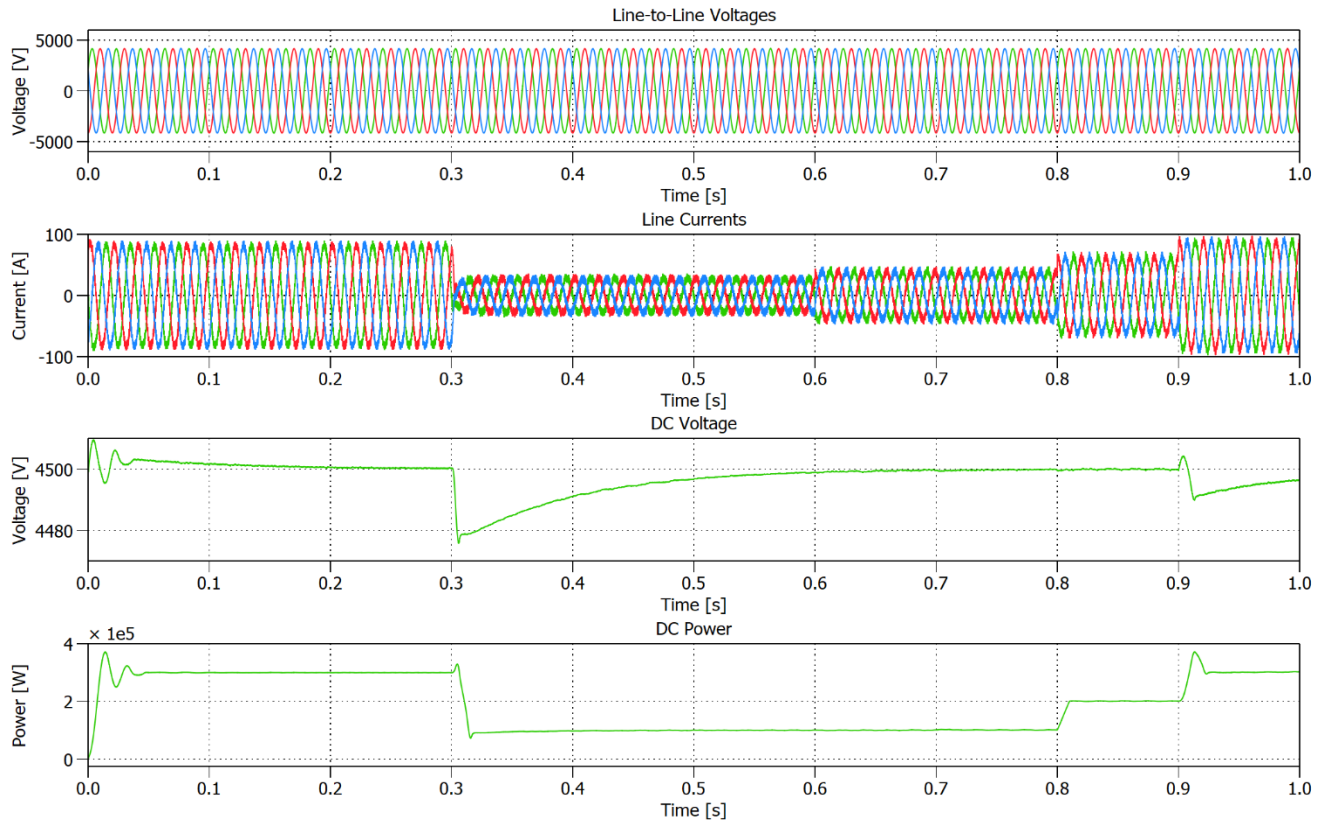
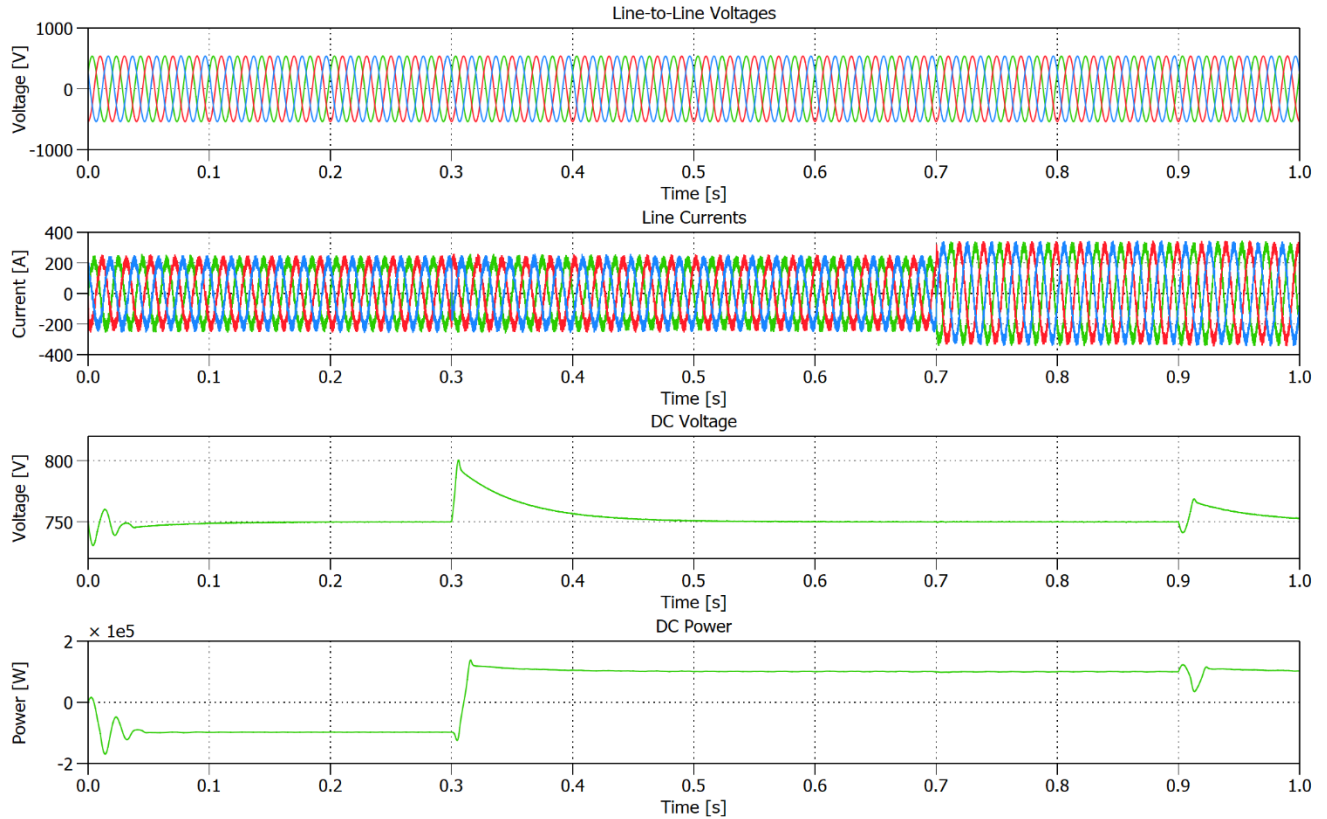Fig. 5. Simulation results for the MV converter.

Fig. 6. Simulation results for the LV converter.

The control is evaluated in the following conditions:
1. Initial conditions: a 100 kW resistive load on each of the dc link is connected. The LV inverter has a power reference to be transferred to the LV grid of 100 kW.
2. At t = 0.3 s a reverse power flow is asked from the LV stage, which starts absorbing 100 kW from the LV grid.
3. At t = 0.6 s a 100 KVAr reactive power step increase is demanded from the MV ac grid.
4. At t = 0.7 s a 100 KVAr reactive power step increase is demanded from the LV ac grid.
5. At t = 0.8 s a 100 kW power step increase is demanded from the MV dc grid.
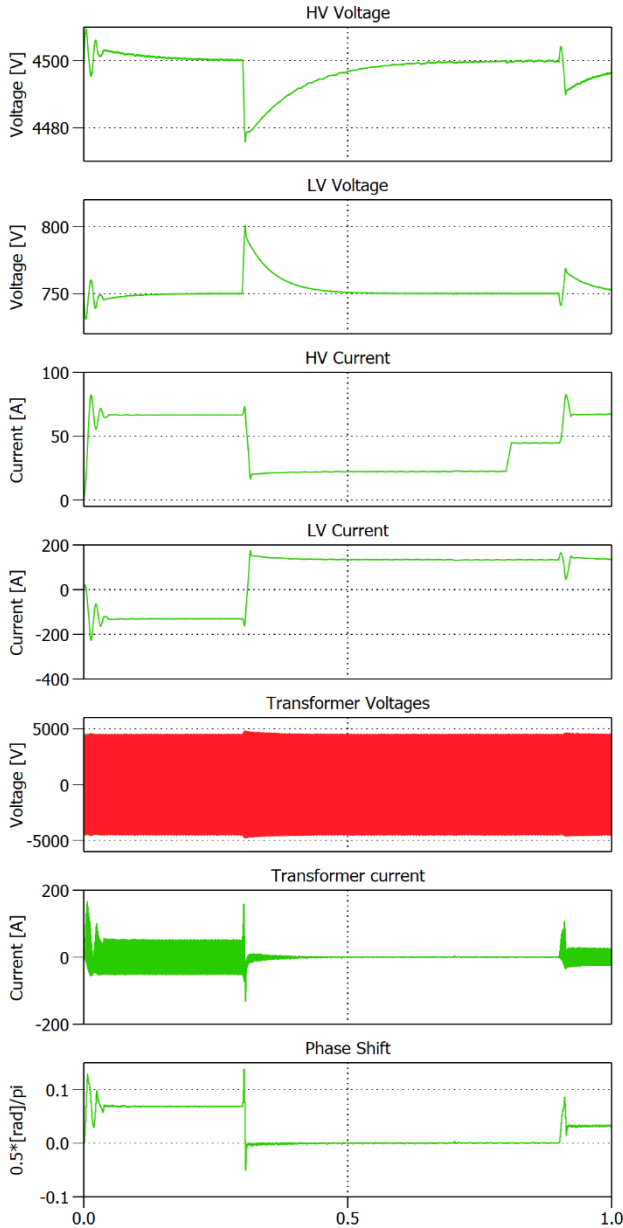6. At t = 0.9 s a 100 kW power step increase is demanded from the LV dc grid.

Some comments can be made to draw the attention to the peculiar features of the proposed control. Firstly, the current control of the ac stages has an excellent dynamic. It is evident from Fig. 5 that the reverse power flow happens as soon as the command is issue in the LV stage. The dynamic appears slower in the MV stage, but that is the desired behavior, since the reference current for the MV stage also considers the dynamics of the capacitors. Moreover, as can be noted from Fig. 6, the active power of the LV stage is always controlled at the desired value of 100 kW. In Fig.7 the DAB performance can be appreciated. In particular, during the time interval 0.3 s < t < 0.9 s the power balance requires no power processing through the DAB, which correctly handles the situation (transformer current and phase shift equals to zero). Finally, the transients in the dc lines are recovered fast, although the reverse power flow condition still causes a 8% overshoot.

V. CONCLUSION

In this paper, complete control of the three stages of a smart transformer has been implemented. A predictive control which performs the multi-objective optimization with a single cost function is developed instead of the standard control paradigm which uses PI controls. Numerical simulations showed that the proposed control allows obtaining excellent dynamic performance in terms of power transfer and a good disturbance rejection when loads are connected to the medium- or low-voltage dc links.

Fig. 7. Simulation results of the DAB converter.

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