# A Stable and Robust DC Power System for More Electric Aircraft

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Abstract-'More Electric Aircraft' (MEA) is a trend for medium and long haul airliners, in which all functions except propulsion are powered by engine-driven electrical generators. Power systems for MEA are in the process of rapid development. Constant Power Loads (CPL) pose a big challenge for power system stability. This paper proposes a concept of a MEA power system with a common DC bus, where power sharing between generators is achieved without droop or explicit communication. The paper shows how a coordinated response can be achieved by multiple DC-DC converters under PI current control, based on the local current measurements only. It utilises advanced control concepts, including feedforward and multiple degrees-offreedom design. The paper demonstrates stability of the proposed power system with respect to any load type, including CPL. The findings of the paper are validated by detailed simulations and preliminary experimental results.

*Index Terms*—More Electric Aircraft, DC microgrid, Interleaved DC/DC converter, Power system stability.

# I. INTRODUCTION

Within the transport sector, aviation is the fastest growing contributor to global emissions and oil consumption [1]. While road transport has various viable alternatives to oil available, the aviation sector is facing much bigger challenges, due to on-board storage limitations. While electric power train is more efficient than combustion engines, specific energy of batteries is currently only 2% percent that of liquid fuel. This currently limits application of the AEA concept to small manned and unmanned air vehicles only. For medium and long haul airliners, the most feasible concept accepted worldwide is 'More Electric Aircraft' (MEA).

In a conventional aircraft, engines generate power from fuel. The bulk of the power is used for propulsion. The remainder is transformed to hydraulic, pneumatic, mechanical, and electrical power to supply different loads in the aircraft [2]. Pneumatic power is used for environmental control and anti-icing. Hydraulic energy is used to power flight controls and landing gear. Mechanical systems are driven by mechanical power through gearboxes. Electrical power is used for lighting, avionics, and commercial loads. In the MEA concept all of these functions, save for propulsion, will be powered by engine-driven electrical generators [3].

There exist a number of electrical standards for a large civilian aircraft, including DC and AC power. Avionics uses 28 Vdc, while larger loads are supplied from 270(+/-135) Vdc or 115 Vac at 400Hz [4]. To reduce the current and the cable weight, emerging higher voltage standards of 540(+/-270) Vdc or 230 Vac have been introduced. In the first versions of a large civilian MEA, a mix of these standards were used within a multiple-bus electric systems [2], [4]. Since then, a steady shift has been observed towards a single DC bus power system [5]–[7]. An example of such a system is illustrated in Fig.1.

In the common DC bus electric system, power is generated by Starter/Generators coupled to the aircraft engines. After



Fig. 1: Common DC bus system for MEA.

rectification, electric power in DC form feeds the High Voltage DC (HVDC) bus. AC loads, such as anti-icing systems, environmental control systems (ECS), electro-mechanical actuators (EMA), etc., are supplied via DC/AC converters. DC loads, such as avionics and in-flight entertainment, are supplied via DC/DC converters. The advantages of such a system over a multiple bus or standard power system include economy of weight and efficiency, and the ease of integration of battery storage and renewable energy sources [8].

Essentially, such an electric power system (EPS) is similar to a DC microgrid, allowing the same control principles to be applied. Note that power available to different generators from the aircraft engines is not equal and dynamically changes, necessitating a coordinated control of power sharing. The common drawback of active power sharing methods [9] is their dependence on telecommunication, which introduces a single point of failure into the system. Passive or decentralized power sharing methods, such as droop control, are free of this drawback and are thus given a preference. Various types of droop control for DC-bus systems are known and have been studied [10], including voltage mode (V/I, V/P) and current mode (I/V, P/V) control strategies, with and without a battery storage. Generally, the DC bus voltage is affected by the droop control and needs a restoration or compensation [8].

The biggest challenge to a DC-bus EPS stability is the presence of Constant Power Loads (CPL). As mentioned before, the two main types of loads for MEA EPS are: DC loads powered via DC/DC converters and AC drives powered via DC/AC converters. Both power converter driven loads have feedback loops around them, to keep their output power unchanged in the presence of DC bus voltage variations. If the input voltage increases by  $\Delta V_{in}$ , the input current has to decrease by  $\Delta I_{in}$  to keep the input power  $P_{in}$  constant.

$$\frac{d}{dt} \begin{bmatrix} i_{S1} \\ i_{S2} \\ \vdots \\ i_{SN-1} \\ i_{SN} \end{bmatrix} + \begin{bmatrix} \frac{K_1}{L_1} & 0 & \dots & 0 & 0 \\ \frac{K_2}{L_2} D_2 & \frac{K_2}{L_2} & \dots & 0 & 0 \\ \vdots & \vdots & \ddots & 0 & 0 \\ \frac{K_{N-1}}{L_{N-1}} D_{N-1} & \frac{K_{N-1}}{L_{N-1}} D_{N-1} & \dots & \frac{K_{N-1}}{L_N} 0 \\ \frac{K_N}{L_N} D_N & \frac{K_N}{L_N} D_N & \dots & \frac{K_N}{L_N} D_N & \frac{K_N}{L_N} \end{bmatrix} \begin{bmatrix} i_{S1} \\ i_{S2} \\ \vdots \\ i_{SN-1} \\ i_{SN} \end{bmatrix} = \begin{bmatrix} \frac{K_1}{L_1} D_1 \\ \frac{K_2}{L_2} D_2 \\ \vdots \\ i_{SN-1} \\ i_{SN} \end{bmatrix} i_1 \quad (1)$$



Fig. 2: Proposed DC microgrid for MEA.

Hence, while the instantaneous impedance  $V_{in}/I_{in}$  is positive, the incremental impedance given by  $\Delta V_{in}/\Delta I_{in}$  is negative. This negative incremental impedance of CPL, under certain circumstances, can cause a system to become unstable [11].

Stability of DC power systems with CPL has been studied by many researchers, including [10]–[12]. The main question for MEA is how to guarantee that its electric power system will not become unstable. This question was addressed in [10] by an accurate system modeling, detailed design and by allowing a substantial stability margin. Researchers in [13] used the  $\mu$ -based structural singular value method to improve robust stability. To date, stability of the DC electric power system of MEA remains an open question in world research.

The rest of the paper is organised as follows. Chapter 2 introduces the proposed power system based on a high-voltage DC-bus. It provides theory behind the proposed solution and explains how it achieves coordination between generator outputs, without using droop control or explicit communication. It also theoretically proves the exceptional stability of the proposed power system, with respect to any load type, including CPL. Chapter 3 explains how various control challenges are overcome in the proposed system, and illustrates its operation by detailed simulations. Chapter 4 presents preliminary experimental results. Chapter 5 provides conclusions and directions of future work.

### II. PROPOSED MEA POWER SYSTEM: THEORY

This paper proposes the use of a special form of connection of the DC sources and loads into a radial architecture, in which all loads are connected downstream with respect to all sources, as shown in Fig.2. The load-sharing distributed generators  $DG_j$  (where j = 1, ..., N) operate under closed loop current control, using current references that are derived as given shares  $D_j$  of the measured downstream currents. The leftmost  $DG_{N+1}$  (battery storage supported by capacitor) maintains the DC bus by a closed loop voltage control.

Under these conditions, an implicit communication can be established between the sources. Furthermore, the current controlled DGs can achieve identical and decoupled dynamics. Note that the proposed architecture is different from Master-Slave control, where references are passed from Master to Slave converters via high bandwidth communication. While eliminating explicit communication, the proposed architecture achieves similar simplicity and stability. Specifically, it is fundamentally stable in the presence of CPL. These principles are explored in the next sections.

### A. Implicit communication method and decoupled dynamics

As can be seen in Fig.2, all distributed generators (DGs) are connected via active rectifiers to the common DC bus. There are no loads connected between the generators, which is not an overly restrictive condition for a relatively short MEA microgrid. Each current controlled DG<sub>j</sub> (where j = 1, ..., N) is provided with measurements of its own current  $i_{Sj}$  and voltage  $v_j$  at the connection point, as well as measurement of the downstream current  $i_j$  (immediately to the right of the connection point as per Fig.2).

The corresponding control diagram is shown in the left section of Fig.3, where  $L_j$  denote coupling inductance and  $K_j$  denote control gain for each DG*j* converter. The same loop gain  $K_j/(sL_j)$  is achieved, for example, in a PI current control around an *RL* circuit, if  $k_p = K_j$  and  $\tau_i = L/R$ .

The corresponding dynamic model of the DG system is given by equations (1). Note that the leftmost  $DG_{N+1}$ , the battery storage, maintains the DC bus voltage near its set point value  $v_B$ . In doing so, it instantly supplies the transient difference between the load current and the total current supplied from the other DGs. Therefore, the corresponding current  $i_{SN+1}$  is given in (1) by a separate algebraic equation.

It is proposed that the measured downstream currents  $i_j$ multiplied by coefficients  $D_j$  are used as respective references  $i_{Sj}^*$  for the current control loops of the DG converters. To explain the underlying principle, say that the agreed and equitable shares of DGj (j = 1, ..., N) in the total load current is known and given by  $E_j$  where  $\sum_{j=1}^N E_j = 1$ . It is also possible to define the respective shares  $D_j$  of each DGj with respect to the downstream current. The difference between  $E_j$  and  $D_j$  definitions can be seen by comparing:

$$E_j = \frac{S_j}{\sum_{k=1}^N S_k} \quad \text{and} \quad D_j = \frac{S_j}{\sum_{k=j}^N S_k} \quad (2)$$

where  $S_j$  is the rating of the DG*j* rating, or available power, which may change over time. For example, say that 3 identical generators are sharing the total current equally, so that each of them supplies  $E_j = 1/3$  (j = 1, ..., 3). of the total current. Then generator DG<sub>1</sub> (the rightmost in Fig. 2) supplies  $D_1 = 1/3$ ; DG2 supplies  $D_2 = 1/2$ ; and DG<sub>3</sub> supplies  $D_3 = 1$ , or the entire downstream current that it measures. The battery (DG<sub>4</sub> in this case) would only supply transients and not share the steady state load.

It is not immediately obvious that, in the described system, the DGs will work in an autonomous manner. Thus a brief discussion is provided below to assist in understanding how



Fig. 3: Control diagram of the proposed DC microgrid and its simplification.

this implicit communication mechanism works. In the above example, the rightmost DG<sub>1</sub> whose reference  $(i_{S1}^* = D_1 i_L = E_1 i_L)$  depends only on the load current, can be solved for independently. Its transient response, to a step change of the load current (from the initial  $i_{L0}$  to a new steady state value  $i_{L\infty}$ ), is given by:

$$i_{S1}(t) = E_1 i_{L0} e^{-t/T_1} + E_1 i_{L\infty} \left( 1 - e^{-t/T_1} \right)$$
(3)

The downstream current measured by DG<sub>2</sub> now becomes  $(i_L - i_{S1}(t))$ . In other words, the dynamic response of DG<sub>1</sub> current will feed into the reference for DG<sub>2</sub> current. Then the dynamic response of DG<sub>2</sub> current will contain a component of the type  $te^{-at}$ . The more currents that are fed into the references for the next upstream currents, the more complex and non-linear dynamics  $(te^{2-at}, te^{3-at},...)$  may result. However, in the authors' recent publication [14] a special solution has been presented, which decouples the control of individual DGs. Specifically, it is possible to show that, by selecting the control gains  $K_j$  so that:

$$K_{j} = \frac{L_{j}}{L_{1}} K_{1} \frac{E_{j}}{D_{j}} = \frac{L_{j}}{L_{1}} K_{1} \sum_{k=j}^{N} S_{k} / \sum_{k=1}^{N} S_{k},$$
(4)

the dynamics of all DGs will be identical to that of DG<sub>1</sub> in (3), save that their own respective shares  $E_j$  are applied. With this selection of the control gains, when feeding the dynamic response of DG<sub>1</sub> into the DG<sub>2</sub> reference, the own response of DG<sub>2</sub> characterised by its own time constant  $T_2 = L_2/K_2$ , is suppressed. Instead, DG<sub>2</sub> mimics the dynamic response of DG<sub>1</sub>, with time constant  $T_1 = L_1/K_1$ . DG<sub>3</sub> mimics the dynamic response of DG<sub>2</sub>, and so on.

This mimicking of the right hand side neighbour is passed upstream, resulting in all current controlled DGs responding in a synchronised manner and with the same time constant  $T_1$ , as if they were externally coordinated. The equivalent control diagram appears in the middle section of Fig.3. The combined DG current  $i_{DG}$  has the behaviour of a single first order lag system, with the transfer function given by:

$$i_{DG} = \sum_{j=1}^{N} i_{Sj} = \sum_{j=1}^{N} E_j i_L \frac{1}{1+s\tau} = i_L \frac{1}{1+s\tau}$$
(5)

Current  $i_{N+1} = i_B$  of the leftmost, grid-forming,  $DG_{N+1}$  converter complements  $i_{DG}$  to the total load current  $i_L$ :

$$i_B = i_L - i_{DG} = i_L \frac{s\tau}{1 + s\tau} \tag{6}$$

Based on that, a further simplification of the control diagram is possible, which is shown in the right top section of Fig.3. The very simple equivalent microgrid has stable behaviour, as discussed below.

# B. Stability of the DC microgrid in the presence of loads (including CPL)

One of the most valuable properties of the proposed control scheme is its inherent stability in the presence of any type of load. This will be demonstrated with the help of the equivalent circuit of the power network under study, shown in the right bottom section of Fig.3. Since the combination of DGs behaves like a single first order block, it is replaced in the equivalent circuit by a single DG supplying the total load current  $i_{DG}$ .

Bus resistances between the points of connection of the DGs are accounted for by two resistances:  $R_B$  and  $R_{DG}$ . Resistance  $R_B$  corresponds to the bus segment between the energy storage (ES) and DG<sub>N</sub>. Resistance  $R_{DG}$  is the sum of all resistances  $R_1, R_2, \ldots, R_N$  to the right of the respective DG<sub>j</sub>. To account for the fact that different parts of the total DG current flow through different resistances to reach the load, a coefficient  $\alpha < 1$  is introduced so that:

$$R_1(E_1 + \dots + E_N) + R_2(E_2 + \dots + E_N) + \dots + R_N E_N$$
  
=  $\alpha(R_1 + \dots + R_N) = \alpha R_{DG}$  (7)

Under these conditions, it can be shown that the load voltage  $v_L$  is given by:

$$v_L = v_B - (R_B + R_{DG})i_B - \alpha R_{DG}i_{DG} \tag{8}$$

where  $v_B$  is the tightly controlled voltage at the ES connection point. From the previous discussion, the dynamics of the DG current is described by:

$$T_1 \frac{di_{DG}}{dt} + i_{DG} = i_L \tag{9}$$

The model for the load current  $i_L$  depends on the type of the load: (a) for constant current load (CCL) it is simply  $i_L$ ; (b) for constant impedance load (CIL) it is  $v_L/R_L$ ; and (c) for constant power load (CPL) it is  $\sqrt{P_L/R_L}$ , where  $R_L$  is load resistance. By solving equation (9) in the time domain for each load type, it has been shown by the authors in [15] that the responses of the DG current to a step change in the load current, in these 3 cases, are given by:

$$i_{DG}(t) = i_{L0} + (i_{L0} - i_{L\infty})e^{-t/\tau}$$
(10)







Fig. 5: DC microgrid for MEA.

where the initial  $i_{L0}$  and the new  $i_{L\infty}$  steady state values of the load current, as well as the time constant  $\tau$ , are determined differently in each case. For example, for CCL  $\tau = T_1$ ; for CIL  $\tau > T_1$ ; and for CPL  $\tau < T_1$ .

With respect to CPL, the following conclusion can be made. Although, in the case of CPL the currents and time constant are nonlinear functions of power  $P_L$ , under the proposed control scheme the distributed generator currents still exhibit first order dynamics described by (10), which is stable. The energy buffer current  $i_B$ , which complements  $i_{DG}$ to the total load current  $i_L$ , and the load voltage  $v_L$  calculated according to (8) are also stable.

The currents and voltages of interest are illustrated in Fig.4 for CCL, CIL and CPL, showing only marginal difference between the three cases.

## III. PROPOSED MEA POWER SYSTEM: SIMULATIONS

Theoretical principles described above have been validated by detailed simulations. The DC microgrid used in simulations and, later - in experiments, is illustrated in Fig.5. The ES unit is directly connected to the DC bus without a converter. It maintains the system bus voltage  $v_L$  around its nominal value and supplies the instant difference between the load current and the total DG current. Each DG converter would normally operate in current control mode but can switch into voltage control mode if the ES fails to support the system bus voltage.

Three DG converters (AC/DC) were implemented as threephase interleaved buck converters with diode rectifiers. This type of converters offers many advantages, including: high efficiency; reduced (up to 3 times) ratings of the semicon-



Fig. 6: 3-leg currents and total current for DG1.



ductor switches for the same current output; modularity; and reduced current ripple due to harmonic cancellation between the 3 legs.

The latter is illustrated in Fig.6 that shows the 3-leg currents  $(I_{DG1}^{a,b,c})$  and the total current  $(I_{DG1})$  for DG1. The individual leg currents are approximately at 5.5A with  $\pm 0.75A$  ripple (the DC level shift is due to different carrier shifts relative to the same sampling instance). The total current is at 16.5A with  $\pm 0.2A$  ripple. Thus the relative distortion of  $\pm 13.6\%$  in the leg currents reduces to the relative distortion of  $\pm 1.2\%$  in the total current.

Each DG converter uses only the locally measured information: its own current  $(i_{Sj})$  and its downstream current  $(i_j)$ . The DG current references are formed from the downstream currents as  $i_{Sj}^* = D_j i_j$ . It was intended that the three DGs share the load equally, resulting in  $D_1 = \frac{1}{3}$ ;  $D_2 = \frac{1}{2}$ ; and  $D_3 = 1$ . To regulate the output DG currents, PI controllers were utilised. According to (4), the controller gains should be set as  $K_1$ ;  $K_2 = \frac{2}{3}K_1$ ; and  $K_3 = \frac{1}{3}K_1$ .

When implementing the detailed simulation models, a number of design challenges were met, as discussed below.

Extension of the share equalisation principle to closed loop PI control: Fig.7 shows a detailed closed loop control diagram of one of the DGs (DG<sub>1</sub>, as an example). It includes a PI controller with output saturation (marked as PI), feedforward  $(d_{ff})$  branch, power electronic converter (PE block) modeled as a simple gain, and the coupling inductor  $L_1$ (plant). Current  $i_{S1}$  in inductor  $L_1$  depends on the difference



Fig. 8: Simulation results for DC microgrid.

between the converter voltage and the DC bus voltage  $(V_L)$ .

As discussed in section II-A, the open loop gain of the system shown in Fig.7 can be simplified to  $K_1/(sL_1)$ , if the zero of the PI control is set to cancel the plant pole  $s = -R_1/L_1$  (where  $R_1$  is the coupling inductor resistance). However, this may not be a beneficial control solution. Instead, the current equalisation principle based on implicit communication, discussed in section II-A, can be extended to the control structure shown in Fig.7.

For simplicity, it will be assumed that the three DGs equally share the load current (extension to non-equal shares is straightforward). Then, temporarily ignoring filter  $F_1(s)$ , the open loop transfer function for the control structure in Fig.7 is  $\frac{K_1}{L_1\tau} \frac{(1+s\tau)}{s^2}$ . Assuming that  $i_{S1}^* = (1/3)i_L$ , closed loop transfer function from  $i_L$  to  $i_{S1}$  can be derived as:

$$i_{S1} = \frac{1}{3} \frac{\frac{K_1}{L_1 \tau} \left(1 + s\tau\right)}{s^2 + \frac{K_1}{L_1 \tau} \left(1 + s\tau\right)} i_L \tag{11}$$

DG<sub>2</sub> measures its downstream current  $i_2 = i_L - i_{S1}$ , and used  $(1/2)i_2$  as its reference. It follows from (11) that

$$i_{S2}^{*} = \frac{1}{2} \left( i_{L} - i_{S1} \right) = \frac{1}{2} \frac{s^{2} + \frac{2}{3} \frac{K_{1}}{L_{1}\tau} \left( 1 + s\tau \right)}{s^{2} + \frac{K_{1}}{L_{1}\tau} \left( 1 + s\tau \right)} i_{L}$$
(12)

 $DG_2$  current control has the same structure as shown in Fig.7, albeit different  $K_2$  and  $L_2$ . Therefore

$$i_{S2} = \frac{1}{2} \frac{s^2 + \frac{2}{3} \frac{K_1}{L_1 \tau} (1 + s\tau)}{s^2 + \frac{K_1}{L_1 \tau} (1 + s\tau)} \cdot \frac{\frac{K_2}{L_2 \tau} (1 + s\tau)}{s^2 + \frac{K_2}{L_2 \tau} (1 + s\tau)} i_L \quad (13)$$

If  $K_2$  is so selected that  $\frac{K_2}{L_2} = \frac{2}{3}\frac{K_1}{L_1}$ , then the first numerator in (13) cancels the second denominator. Then expression (13) for  $i_{S2}$  becomes identical to expression (11) for  $i_{S1}$ , as desired. Similar logic can be applied to DG<sub>3</sub>, resulting in a selection of  $K_3$  such that  $\frac{K_3}{L_3} = \frac{1}{3}\frac{K_1}{L_1}$ . Then all three DGs have identical dynamics, and can be represented by a single DG described by

$$i_{DG} = \frac{\frac{K_1}{L_1 \tau} (1 + s\tau)}{s^2 + \frac{K_1}{L_1 \tau} (1 + s\tau)} i_L \tag{14}$$

Unipolar PI controller output: Buck converter that connects DG with DC bus produces unipolar voltage. Consequently, the output of the PI controller in Fig.7 is limited between 0 and 1. Despite the anti-windup implementation of the PI controller, the unipolar limits may cause a problem.

Assume that, due to a small overshoot of the  $i_{DG}$  response, error e at the PI controller input in Fig.7 becomes negative. This causes the PI output to saturate at the lower limit 0. Then the difference  $(d_{ff}V_{dc} - V_L)$  is positive. This difference, integrated by the plant, is subtracted from the reference. This causes the negative error e to grow even further, and so on.

This problem was solved by using the feedforward signal  $d_{ff}$ . Instead of positive  $d_{ff}$ , that is logical for compensation of the negative disturbance  $-V_L$ , a small negative value of  $d_{ff}$  was applied. This value was so selected that the PI output does not hit the lower limit during the  $i_{DG}$  overshoot.

Two degrees-of-freedom control design: In the proposed control scheme, current references for each DG are obtained from downstream current measurement. These measurements can contain significant noise component and, therefore, need to be filtered. This is achieved by adding a filter on the reference signal - block  $F_1(s)$  in Fig.7. In order to achieve the identical DG current dynamics, the filter design needs to be an integral part of the entire control design.

Starting from this point, the entire control structure presented in Fig.7 is considered. The objectives are: to achieve effective rejection and fast response to disturbance (coming from the bus voltage  $V_L$ ), and to achieve a filtering effect (i.e. slow response) with respect to noise on the measured current  $i_L$ . This necessitates a two degrees-of-freedom control design.

The disturbance rejection is achieved by the PI controller. From Fig.7,

$$i_{S1} = \frac{F_1(s)\frac{K_1}{L_1\tau} (1+s\tau)}{s^2 + \frac{K_1}{L_1\tau} (1+s\tau)} i_L - \frac{\frac{1}{L_1}s}{s^2 + \frac{K_1}{L_1\tau} (1+s\tau)} V_L \quad (15)$$

The system poles can be determined by solving the characteristic equation

$$s^2 + \frac{K_1}{L_1}s + \frac{K_1}{L_1\tau} = 0 \tag{16}$$

If  $\frac{1}{\tau} \ll \frac{K_1}{L_1}$  then  $s_1 \approx -\frac{1}{\tau}$  and  $s_2 \approx -\frac{K_1}{L_1}$ . Then expression (15) can be rewritten as

$$i_{S1} \approx \frac{F_1(s)}{1 + \frac{L_1}{K_1}s} i_L - \frac{\frac{\tau}{K_1}s}{\left(1 + \frac{L_1}{K_1}s\right)(1 + s\tau)} V_L \tag{17}$$

If the reference filter is designed as  $F_1(s) = D_1 \frac{1+(L_1/K_1)s}{1+\tau_f s}$ (where  $D_1 = \frac{1}{3}$ ) then the first term in (17) reduces simply to  $i_{S1} = \frac{1}{1+\tau_f s} i_L$ , or the low-pass-filtered share (1/3) of the measured load current  $i_L$ . The second term in (17) provides an effective and fast rejection of disturbance  $V_L$ .

Now, applying the same share equalisation principle as before, the downstream current measured by  $DG_2$  equals

$$i_2 = i_L - \frac{1/3}{1 + \tau_f s} i_L = \frac{2/3 + \tau_f s}{1 + \tau_f s}$$
(18)

If the reference filter is designed as  $F_2(s) = D_2 \frac{1 + (L_2/K_2)s}{1 + (3/2)\tau_f s}$ (where  $D_2 = 1/2$ ) then



(a) Microgrid converters







Fig. 9: Experimental setup and plots.

BMS

$$i_{S2} = \frac{F_2(s)}{1 + \frac{L_2}{K_2}s} i_2 = \frac{1/3}{1 + \tau_f s} i_L \tag{19}$$

or identical to  $i_{S1}$ . Similarly, the reference filter for DG<sub>3</sub> has to be designed as  $F_3(s) = \frac{1+(L_3/K_3)s}{1+3\tau_f s}$ , to give  $i_{S3}$  identical to  $i_{S2}$  and  $i_{S1}$ .

Note that for practical purpose it suffices to set  $F_1(s) = \frac{1/3}{1+\tau_f s}$ ;  $F_2(s) = \frac{1/2}{1+(3/2)\tau_f s}$ ; and  $F_3(s) = \frac{1}{1+3\tau_f s}$ .

Simulation results: With the above design improvements in place, the DC microgrid shown in Fig.5 and consisting of three DGs and one ES, was simulated in Matlab/Simulink. The following parameters were used in the simulations:  $L_1 = L_2 = L_3 = 5m$ H;  $K_1 = 25$ ;  $\tau = 0.005$ s;  $\tau_f = 0.05$ s. Note that, since the share equalisation is now achieved at the reference filter level, the internal PI control of the three DG inverters can be identical.

Fig.8 presents the simulation results when using with three different types of load: CIL, CPL and CCL. The plots show the microgrid currents ( $I_{DG1,2,3}$ ,  $I_{ES}$ ,  $I_L$ ) and bus voltage ( $V_L$ ). Note that the simulation results in Fig.8 are very close to the theoretically expected results presented in Fig.4.

### IV. PROPOSED MEA POWER SYSTEM: EXPERIMENT

The experimental setup used in this study is shown in Fig.9a. It includes: DG power converters built from Semikron inverter modules; programmable SwitcherGear (Denki) controllers; passive and active loads. The battery storage is illustrated in Fig.9b. It consists of 60 LiFePO<sub>4</sub>-type batteries connected into a 96V, 72 A-hrs ES system.

Fig.9c shows experimental plots obtained under the following conditions: at time t = 1.1s the load (CIL in this case) undergoes a step change; and at t = 4.4s one of the DGs reduces its current output. It can be seen from Fig.9c that until t = 4.4s the two DGs have identical dynamics, while the ES only provides transient current. After t = 4.4s, the ES compensates for the DG output current reduction by providing the current deficit to the load.

The preliminary results provide the proof-of-concept for the proposed DC power system. More experiments will follow.

## V. CONCLUSIONS

The paper has presented a novel DC microgrid-based power system for MEA, in which coordination between distributed generators is achieved without droop control or explicit communication. The proposed power system is robust and stable with respect to any type of loads, including CPL. Effectiveness of the proposed scheme has been validated by simulation and preliminary experiments. Future work includes a thorough experimental validation.

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