Supercapatteries & Power Electronics

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Performance Evaluation of an Energy Storage System for Household Applications

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PEMC group Conference – 18 December 2014

Project Summary

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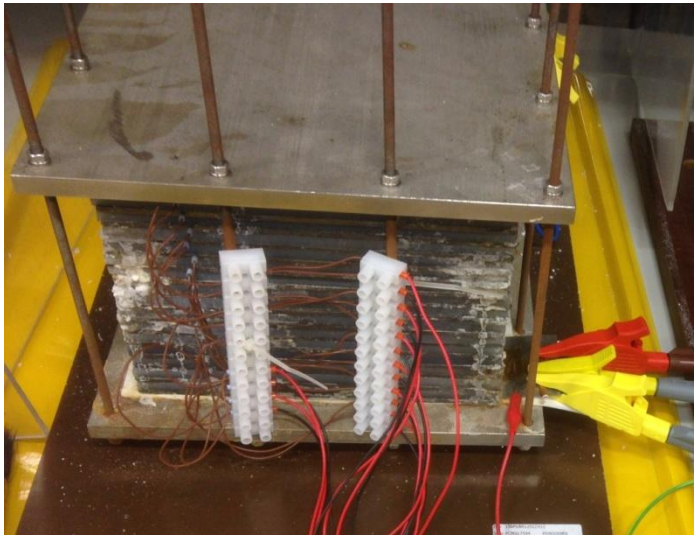
Future House

www.ferroamp.com/energyhub/benefits-for-consumers/

Project Aim: Develop an Energy Storage System based on the Supercapattery Device for household application : 1-2kWh / 2kW rated power

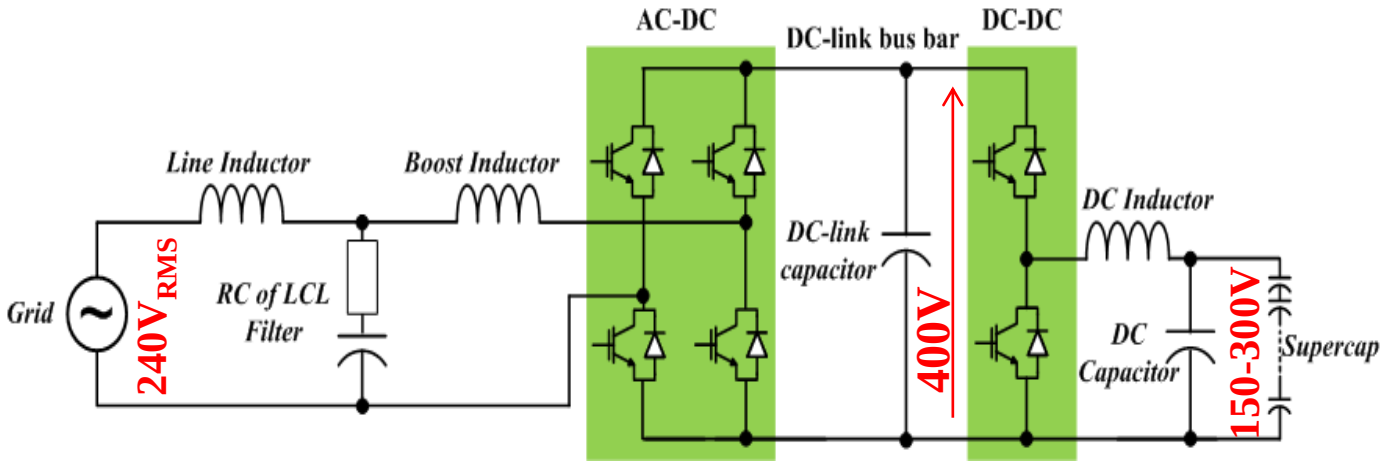


16 cell supercapattery stack (120F/20V)

Chemical Engineering Track (team led by Prof. G.Z.Chen):
- Develop novel materials with high specific capacitance (F/g)
- Develop full working cells (test materials)
- Develop full working stacks

Electrical Engineering Track (Dr.Kulsangcharoen&Klumpner)**:**
- Characterisation of Supercapattery stacks
- Cell voltage monitoring and estimation of individual cell performance
- Development of voltage equaliser
- Development of a Power Converter System
- Investigating the performance of converter using novel materials/advanced topologies

Proposed Converter System



- **Employ two-stage topology consisting of:**
  - **a half-bridge inverter topology for the DC variable (SC) to DC fixed voltage**
  - **a conventional H-bridge inverter topology for the DC/AC conversion**
- **The supercapacitor (SC) is operated between 150V to 300V (ratio 1:2) in order to utilise 75% of its maximum stored energy**
- **Fixed DC-link voltage allows for reduced switching losses and reduces size of the inductors (AC side and SC side)**
- **Design Aims: Maximum conversion efficiency at a reasonable cost**
  ⇒ use Trench/Fieldstop IGBT3 (Infineon) and metglas magnetic core material

Determine Breakdown of Power Losses

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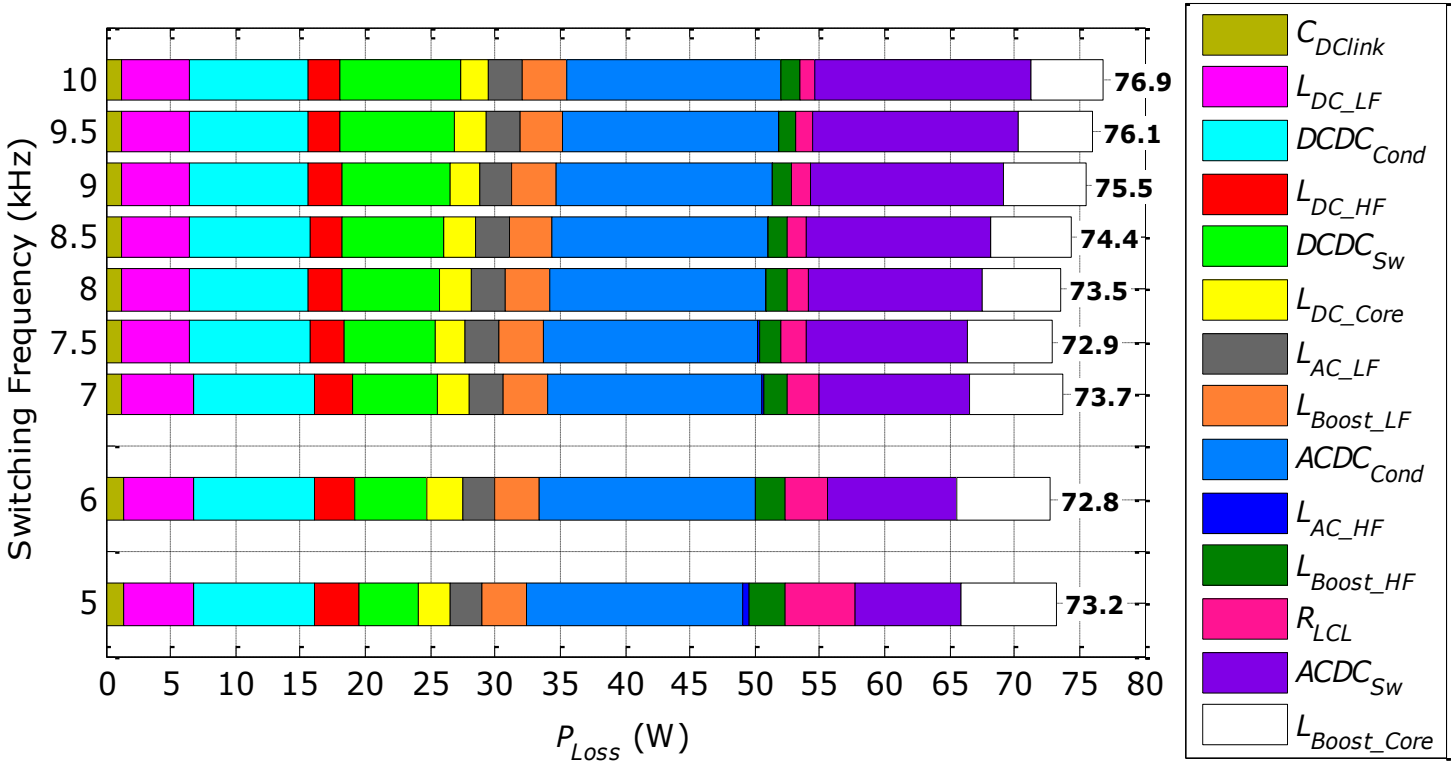
- Design of passive components based on standard switching ripple attenuation
- Selection of devices is based on reasonable current loading 30A IGBT, j_{CO}>2.5A/mm^2
- Simulation waveforms (time domain and FFT) used in conjunction with detailed loss models of semiconductors and inductors (ESR vs frequency)
- Breakdown of power losses performed at 0.5kW/1.0kW/1.5kW/2kW and 5-10kHz



Example of Power Loss breakdown at rated power (2kW) and fsw= 5-10kHz

Optimum Switching Frequency

The total system power loss is

$$P_{TLoss} = P_{Semi} + P_{LossLDC} + P_{LossLAC} + P_{LossLBoost} + P_{LossRLCL} + P_{LossDClink}$$

Where it is assumed current ripple is inverse proportional with switching frequency and ESR is constant or varies with frequency (curve fitting function)

$$P_{Semi} = P_{Cond} + \left\{P_{Sw\_10kHz} \cdot 10^4 / f_{sw}\right\}$$

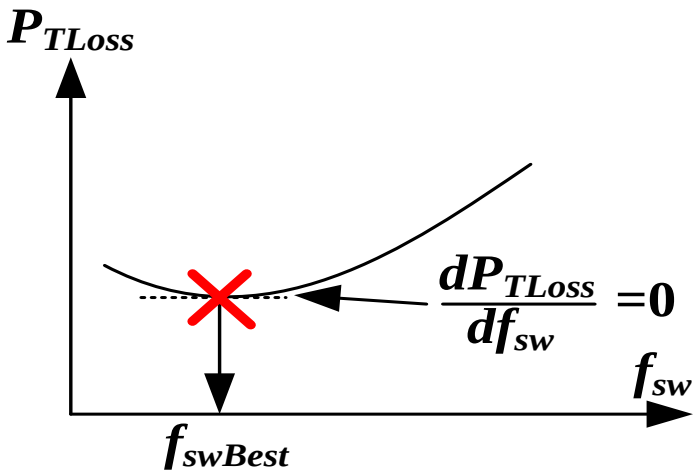
$$P_{LossLDC} = P_{LossLDC\_LF} + ESR_{LDC}(f_{sw})\left\{I_{LDC\_10kHz} \cdot 10^4 / f_{sw}\right\}^2$$

$$P_{LossLAC} = P_{LossLAC\_LF} + ESR_{LAC}(f_{sw})\left\{I_{LAC\_20kHz} \cdot 10^4 / f_{sw}\right\}^2$$

$$P_{LossLBoost} = P_{LossLBoost\_LF} + ESR_{LBoost}(f_{sw})\left\{I_{LBoost\_20kHz} \cdot 10^4 / f_{sw}\right\}^2$$

$$P_{LossRLCL} = P_{LossRLCL\_LF} + (R_{LCL})\left\{I_{LBoost\_20kHz} \cdot 10^4 / f_{sw}\right\}^2$$

LF ***HF***

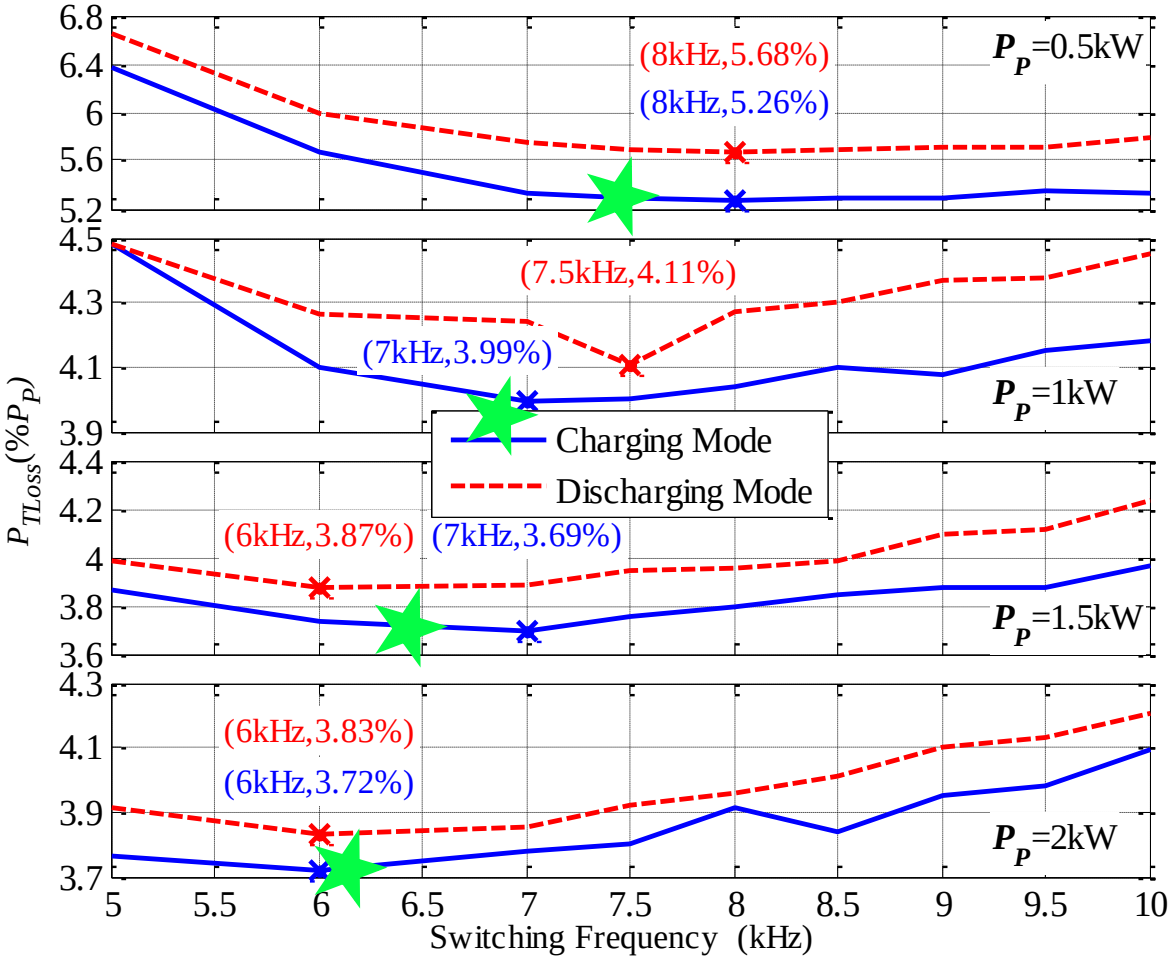


- **Perform a derivative on the P_{TLoss} against f_{sw} and set it to 0.**
- **Solve this new equation, the optimum f_{sw} can be determined (f_{swBest} where P_{TLoss} is at its minimum)**

Analytical Optimum f_{sw} vs Experimental

P_P (kW)	f_{swBest} (kHz)		
	Experimental		Analytical
	Charge	Discharge	Average
0.5	8	8	7.45
1	7	7.5	6.84
1.5	7	6	6.44
2	6	6	6.16

The analytical f_{swBest} is very close to the experimental



- The optimum switching frequency reduces as the processing power increases
- Achieve round-trip efficiency of 92.5% at 1.5-2kW (drops to 89%@0.5kW)

Breakdown of Power Loss @ PN

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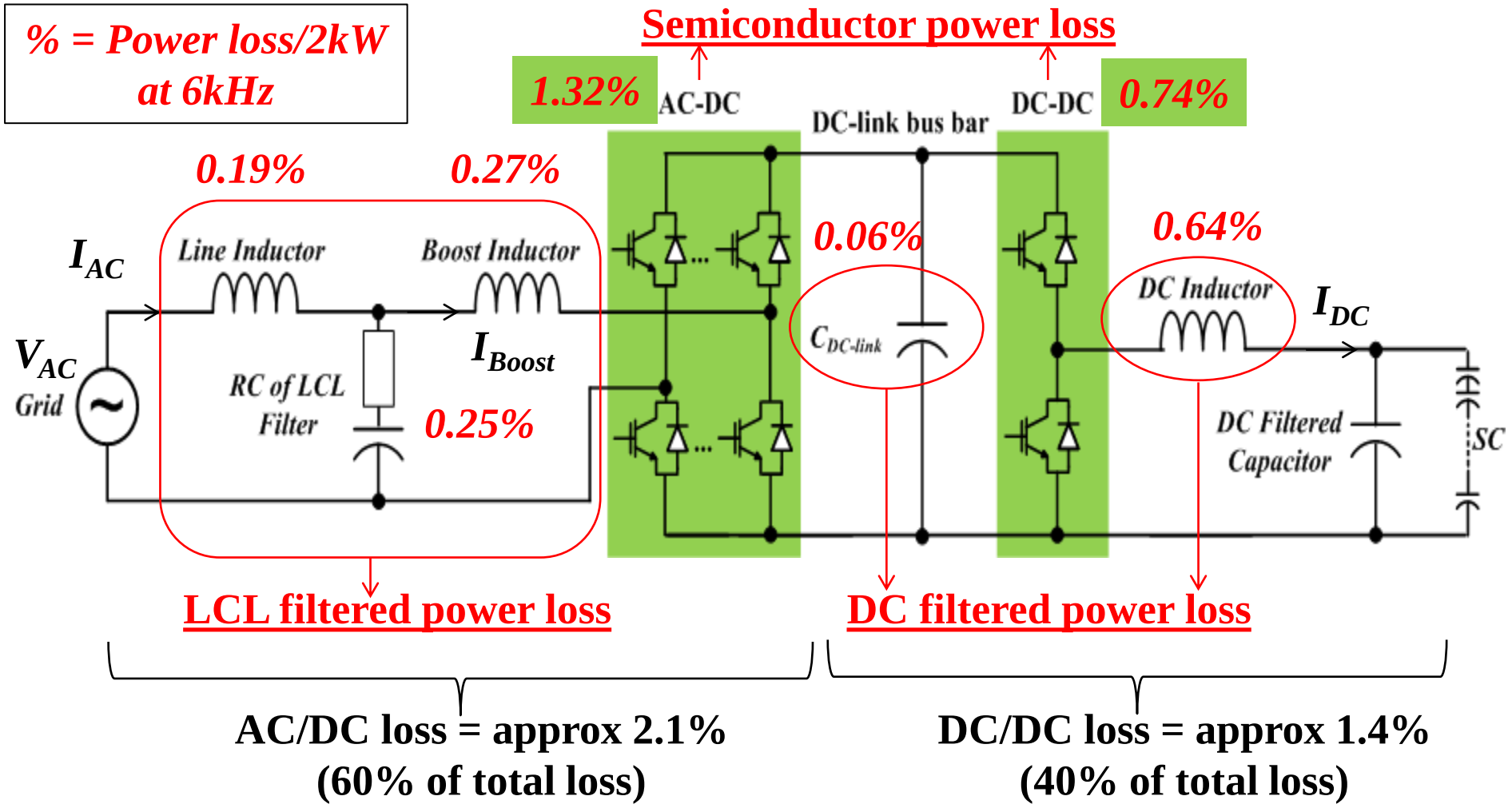
% = Power loss/2kW at 6kHz



Further investigation in improving efficiency of each stage is carried out
This includes new topologies and assumes the redesign of passive components

Inverter Improvements: Single Stage vs Two Stage Approach

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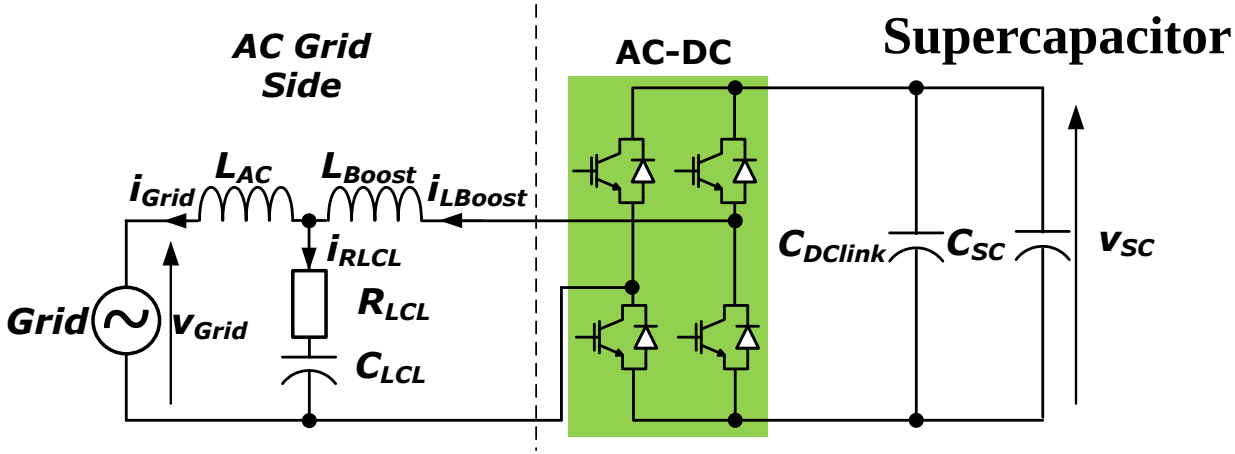
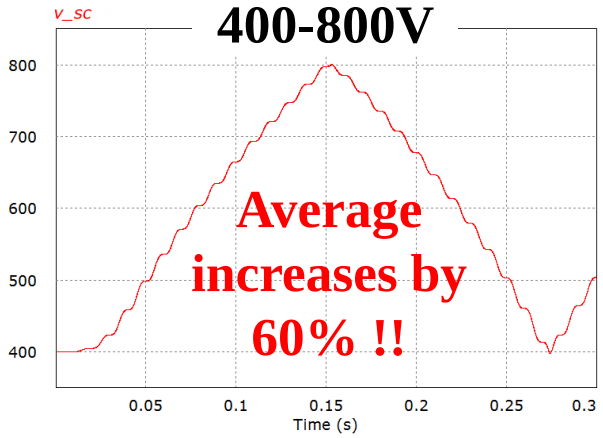
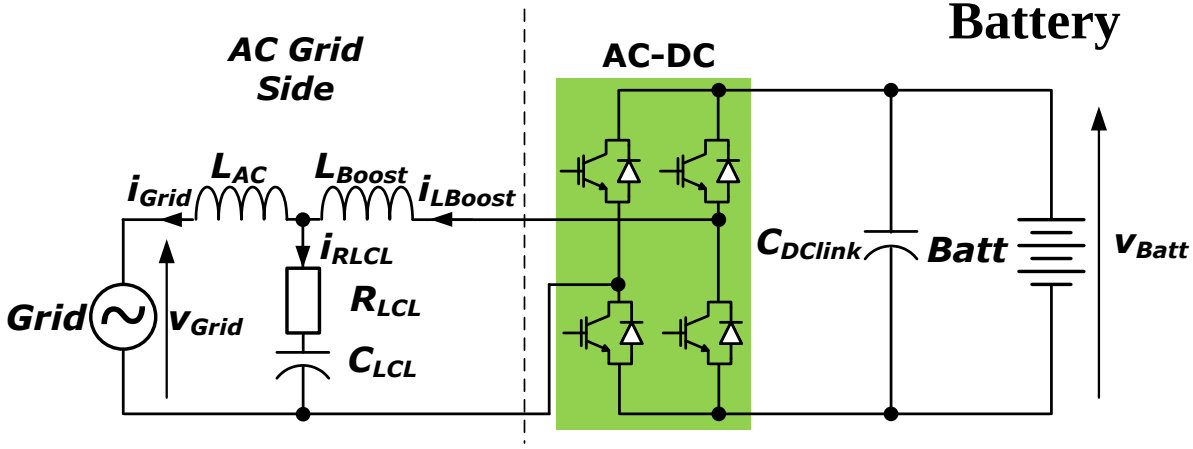
Potential Benefit: - removes losses associated with the DC/DC stage

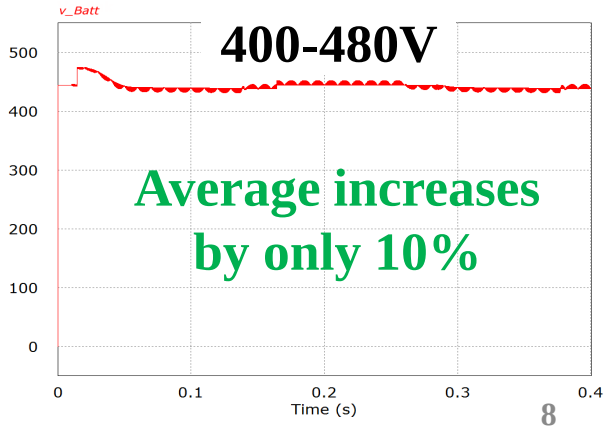
Potential Problem: - switching losses and core/high frequency loses in inductors of AC/DC inverter will increase







DC-link Voltage



Inverter Improvements: Asymmetric Leg & Modulation

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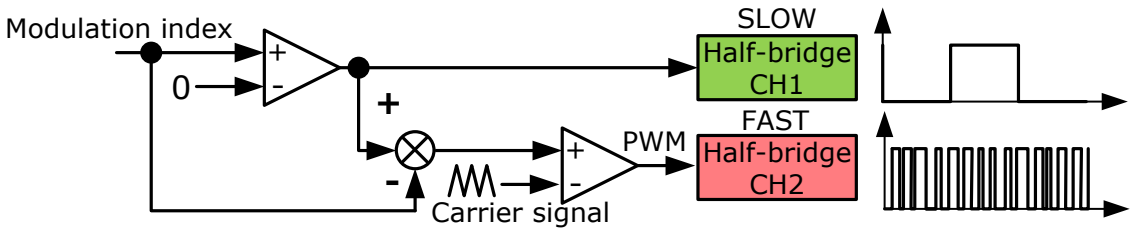
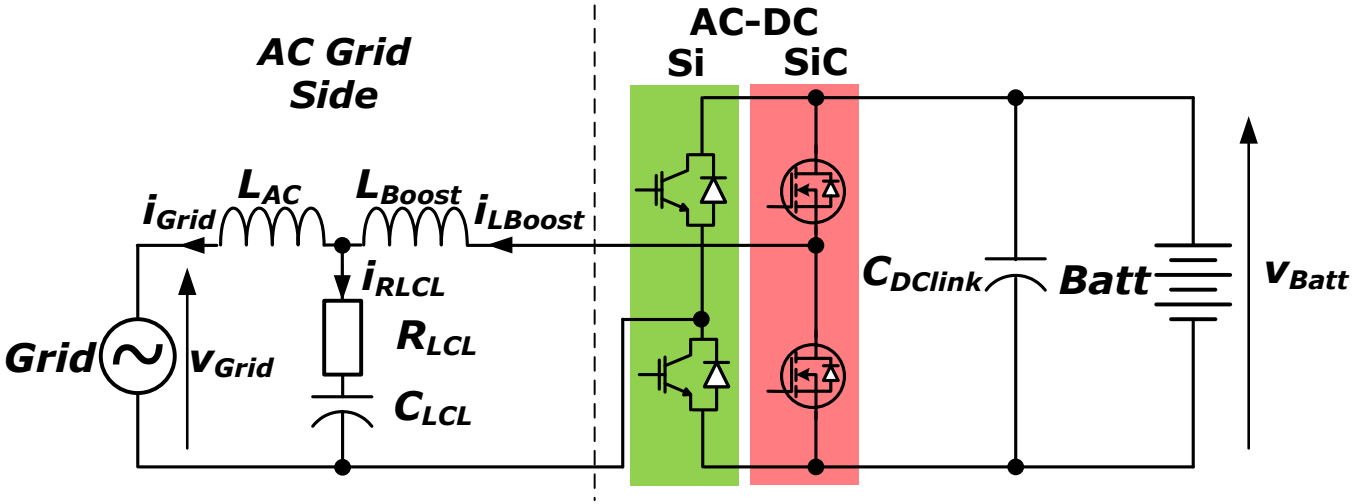
Potential Benefit: - moves all switching losses in one of the legs
- then SiC switches can be used in the stressed leg
- overall could save switching losses with smallest extra cost





Power Loss Comparison of AC/DC Inverter Improvements

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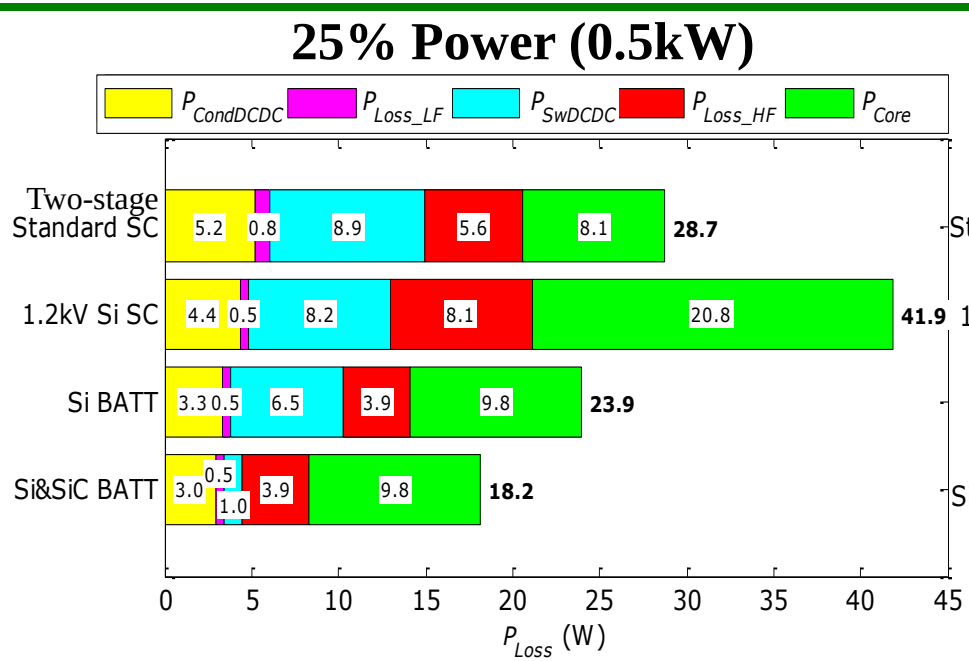

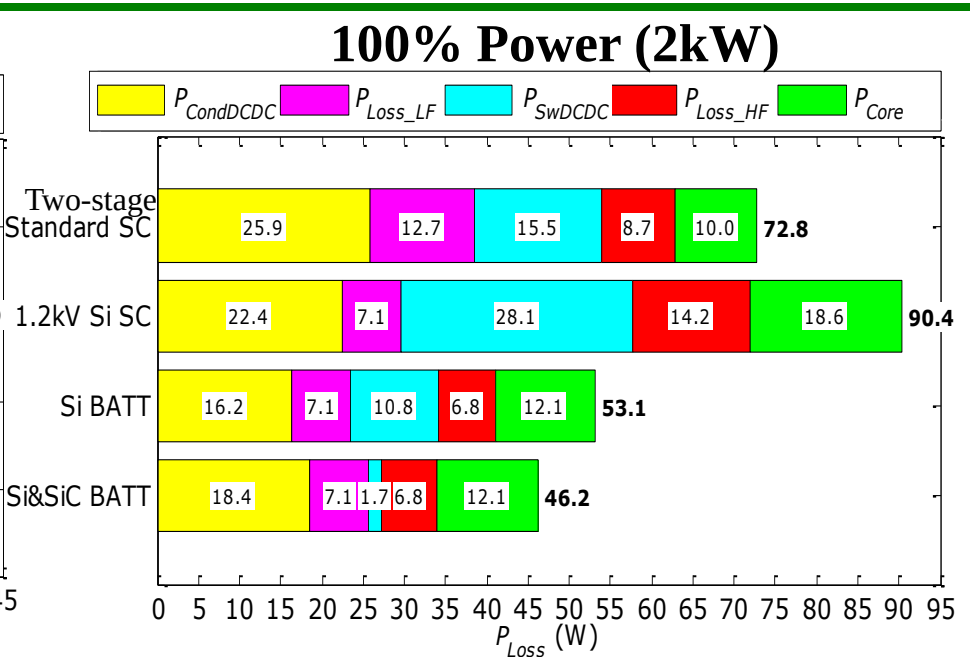

- Single stage + SC in DC-link experiences higher losses due to extra losses in passive components, whilst semiconductor losses in 1-stage/4 switches are in fact smaller than in 2-stage/6 switches
- Use of SiC in one leg (not shown) may further reduce switching losses by 20W making the single stage topology more efficient than 2-stage (70W compared to 73W)
- Use of a storage device with narrow voltage range (battery) may enable cheaper and/or more efficient conversion: silicon (53W) and SiC (46W) compared to 73W
- Advantage of SiC is not so obvious unless f_{sw} needs to be further increased

Improvement in the DC/DC Converter: Use Interleaving

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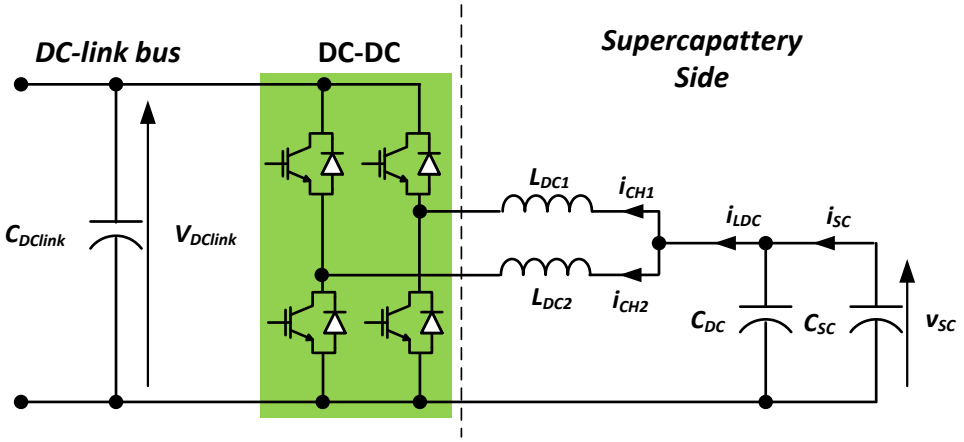
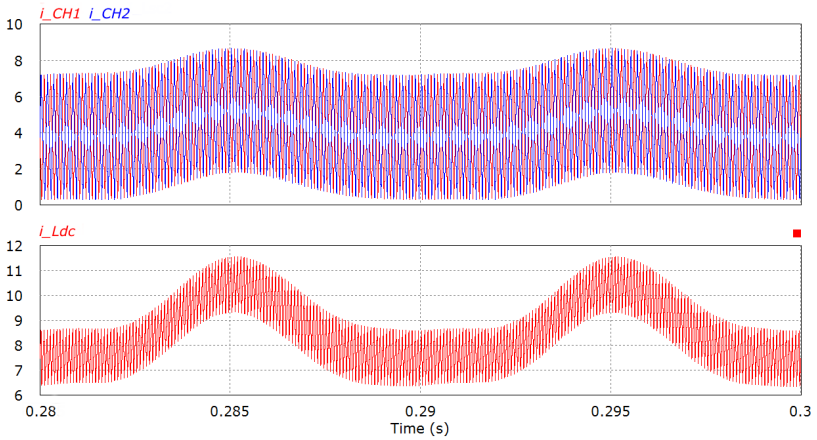
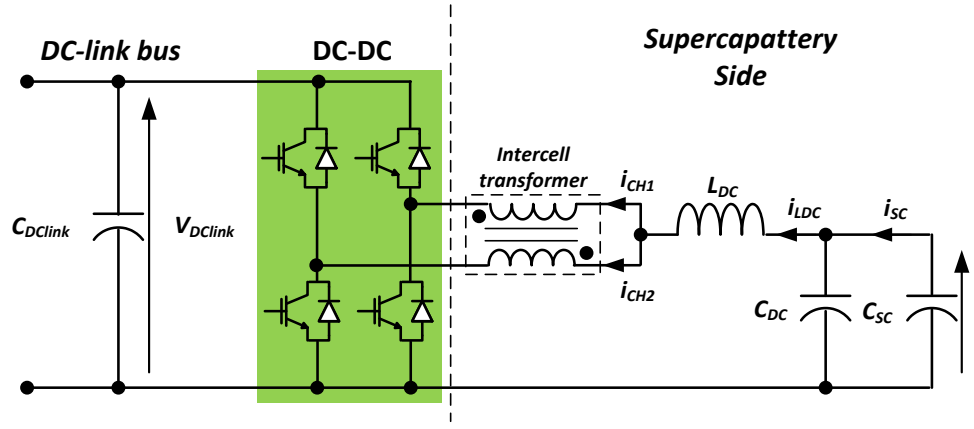
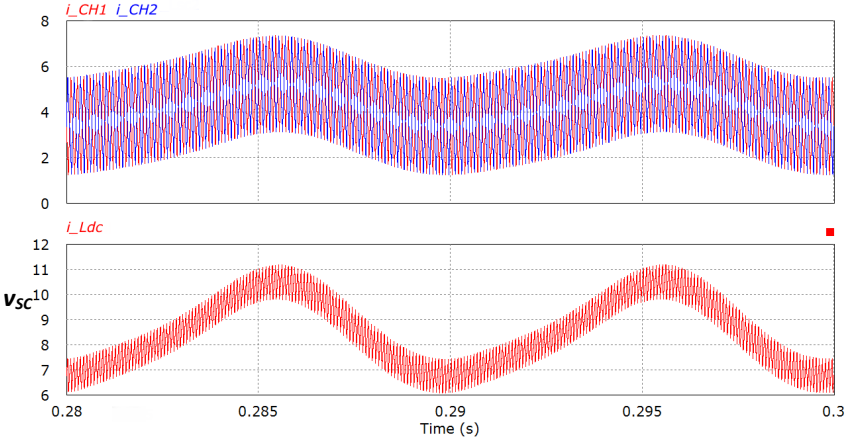
Potential Benefit: - size of L can be reduced w/o increasing fsw

Potential Problem: - current ripple in L will increase (higher HF losses in L)









Improvement in the DC/DC Converter: Use Multilevel DC/DC Converter

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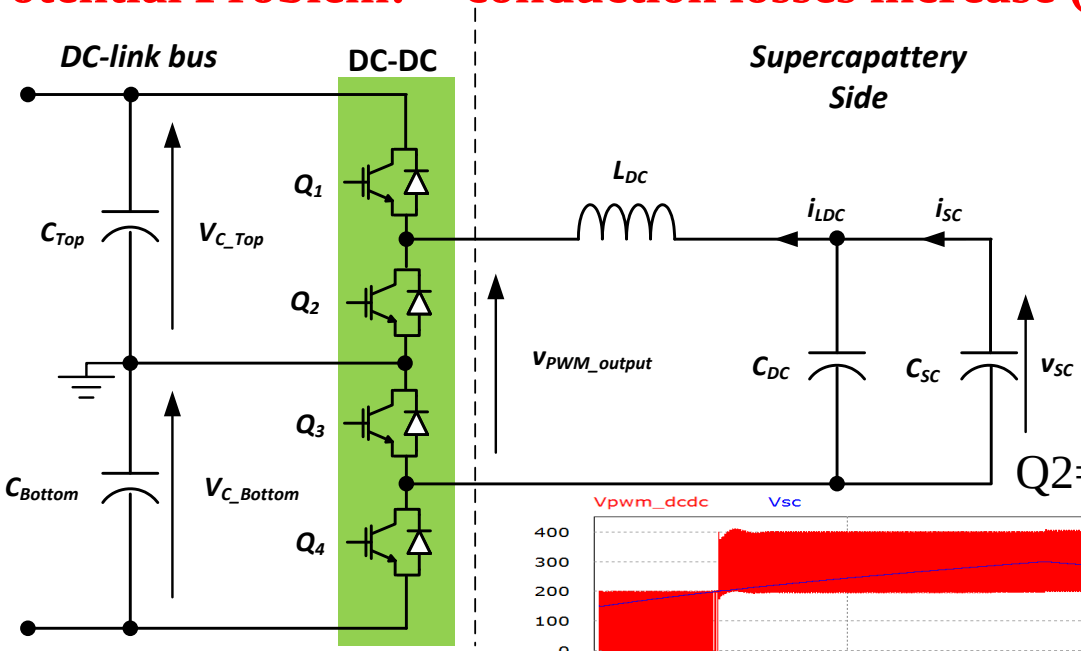
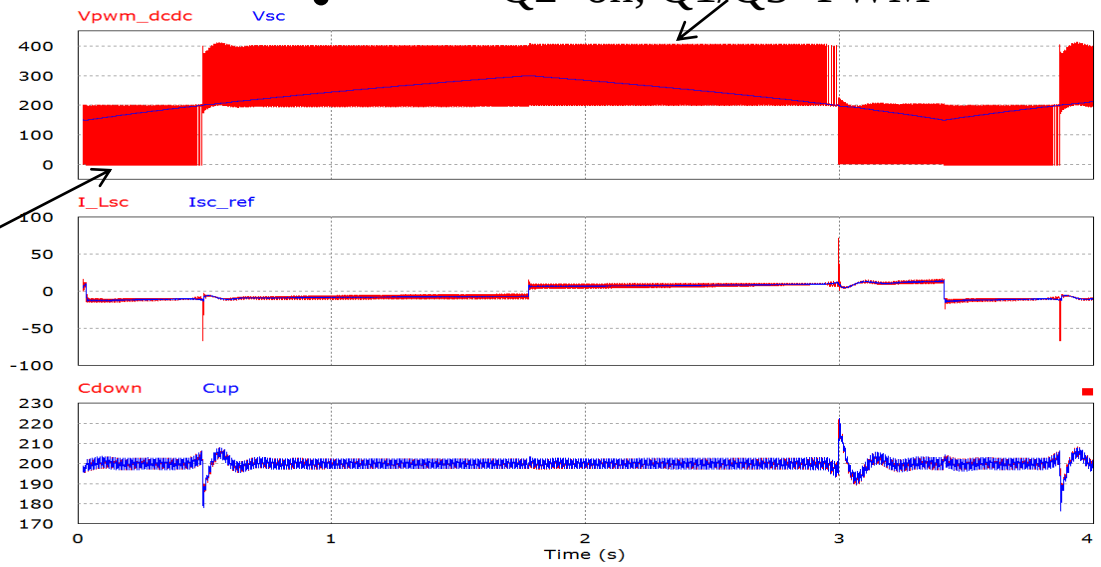
Potential Benefit: - size of L_{DC} and switching losses can be reduced (switch ½ Vdc)

Potential Problem: - conduction losses increase (additional devices in current path)



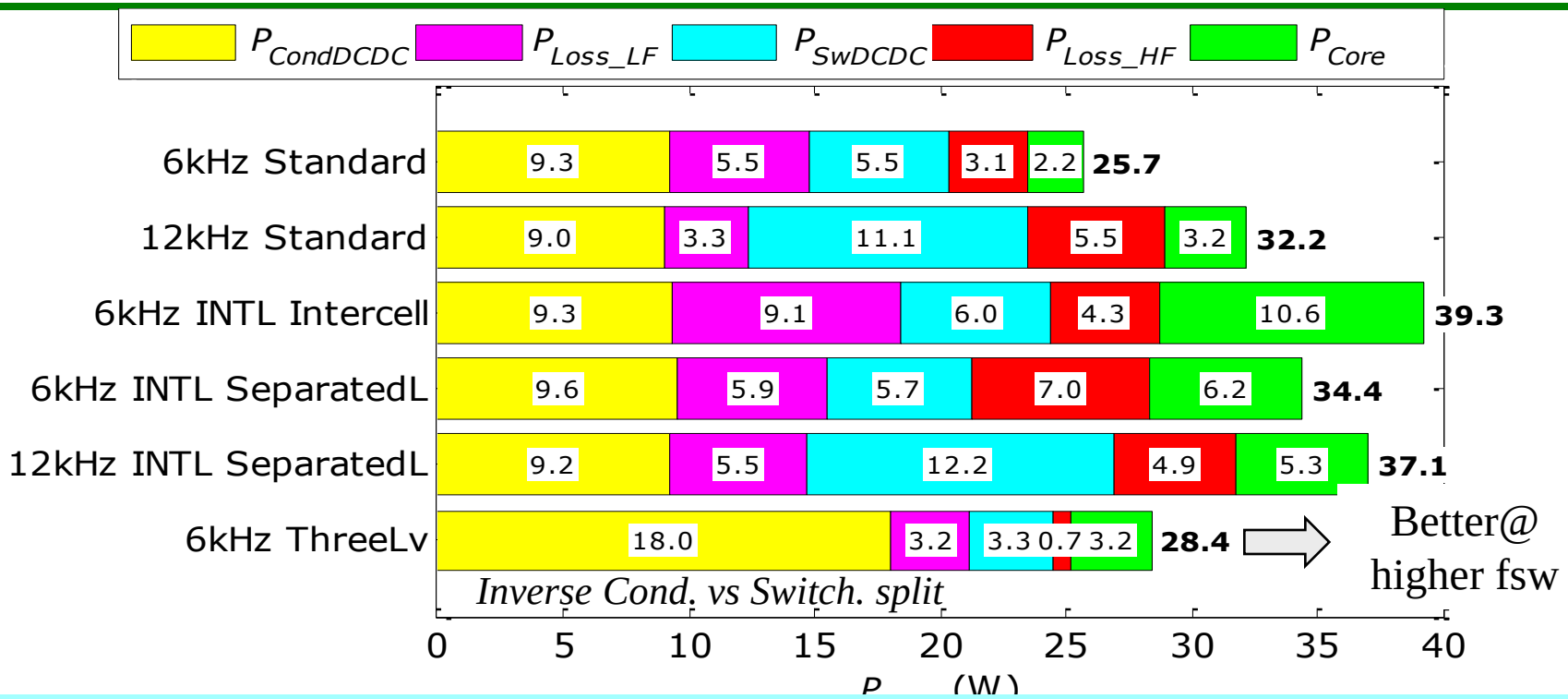
Q2=on; Q1/Q3=PWM

Q3=on; Q2/Q4=PWM



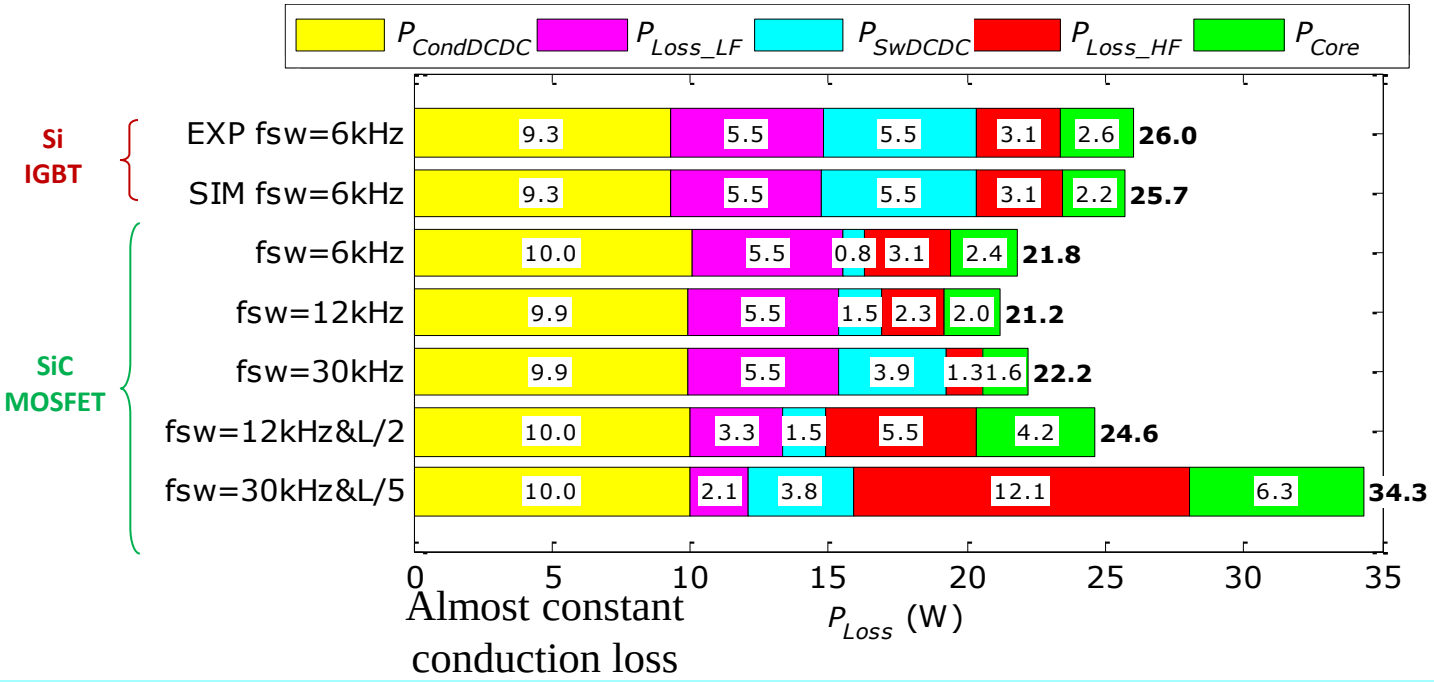
THREE voltage levels

DC/DC stage Power Loss Comparison



- The standard configuration remains the most efficient but currently has a problem DC/DC causes too much noise
- Increase Standard f_{sw} to 12kHz causes an increase of only 6.5W (0.3%) but still remain the most efficient at 12kHz
- If reduction in physical size is required (of Ldc), switching faster and adopting a more complex converter may be more efficient solution as well 3Lv@f_{sw}>12kHz

Use SiC devices in DC/DC converter



- SiC devices allow for a small decrease (-4W) of losses at low switching frequency; The switching stress will be insignificant and equivalent to oversizing the converter/poor utilisation of devices
- Choosing to sacrifice slightly efficiency (+8W loss) for the sake of increasing significantly the power density (much smaller 0.2L-size) can be an option
- Similar losses/efficiencies are achievable with moderate increase of f_{sw} (12-20kHz) and moderate decrease to 0.4-0.5 of L-size

Conclusions

- State of the art switches and converter technologies can provide reasonable cost & performance (η=92.5% RT) in energy storage apps
- Analytical models of losses can help find the switching frequency optimum at optimise losses at different loading levels
- Further improving the efficiency of the power converters have been investigated including:

- Employ new SiC semiconductor technology to reduce switching losses and by switching faster, to reduce magnetic component size
- Employ more complex topology (e.g. multi-level, interleaved, etc) to reduce filter size (smaller voltage ripple or period)
- Most approaches didn't actually reduced losses but may be the key to reduce physical size of the converter

Acknowledgement - The project this report is based on was funded by E.ON as part of the E.ON International Research Initiative. Responsibility for the content of this publication lies with the author.