Robust snubberless soft-switching power converter using SiC Power MOSFETs and bespoke thermal design

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Abstract

A number of harsh-environment high-reliability applications are undergoing substantial electrification. The converters operating in such systems need to be designed to meet both stringent performance and reliability requirements. Semiconductor devices are central elements of power converters and key enablers of performance and reliability. This paper focuses on a dc-dc converter for novel avionic applications and considers both new semiconductor technologies and the application of design techniques to ensure, at the same time, that robustness is maximised and stress levels minimised. In this respect close attention is paid to the thermal management and an approach for the heatsink design aided by finite element modelling is shown.

1. Introduction

As part of consistent EU activities targeting the development of more electric aircraft, higher voltage on board power distribution buses (e.g., 270 V_{DC}) are being considered [1]. A number of bi-directional DC-DC converters are needed to implement the interconnection between the two buses and allow power transfer between sources, storage elements and loads. In this work, reference is made to a dual-active bridge DC-DC converter topology rated at 1.2 kW, $270V_{IN}$-$28V_{OUT}$ intended for operation at ambient temperature of 75 ºC[2,3]. Fig. 1 shows the circuit schematic; its basic operation is broadly reported in the literature (see [4,5], for example). For this converter the representative waveforms are briefly reported in Fig. 2, and the efficiency is shown in Fig. 3. Latest generation 650V ROHM SiC MOSFETs are used at the primary side (270 V) and Infineon Opti-MOS transistors at the secondary side (28 V) [6,7]. The paper discusses design options aimed at ensuring robustness and reliability under tight operational conditions, as well as volume and weight constraints.

2. Design for robustness

2.1. Soft-switching techniques

Soft-switching techniques encompass Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS) methodologies. Both foresee the use of controlled resonance phenomena between inductive and capacitive elements to achieve non-dissipative (i.e., with either nearly zero current or voltage) turn-on or turn-off of the switching devices. Beyond being an extremely powerful solution for improving the efficiency of switching power converters, these techniques also enable a considerable reduction of the electro-thermal stress level affecting solid-state devices and thus are an important asset in circuit design for robustness and reliability. Typically ZVS is used to achieve non-dissipative turn-on; ZCS is used to bring along non-dissipative turn-off. The combination of both techniques in the same converter typically involves complications at topology level (e.g., fully resonant solutions).

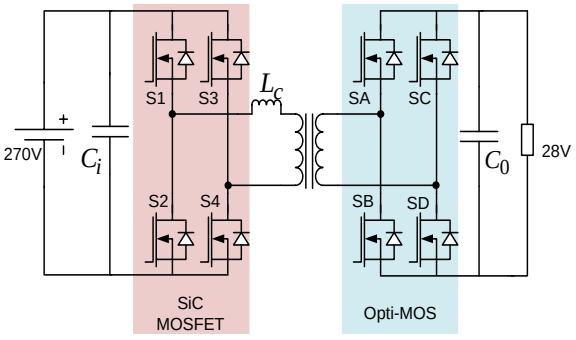

Fig. 1 Schematic of a resonant-transition Zero-Voltage-Switching dual-active bridge DC-DC converter.

For the present goals, only ZVS was implemented:

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the converter limits the resonant transition to the commutation events to realise ZVS at turn-on of the power MOSFETs.

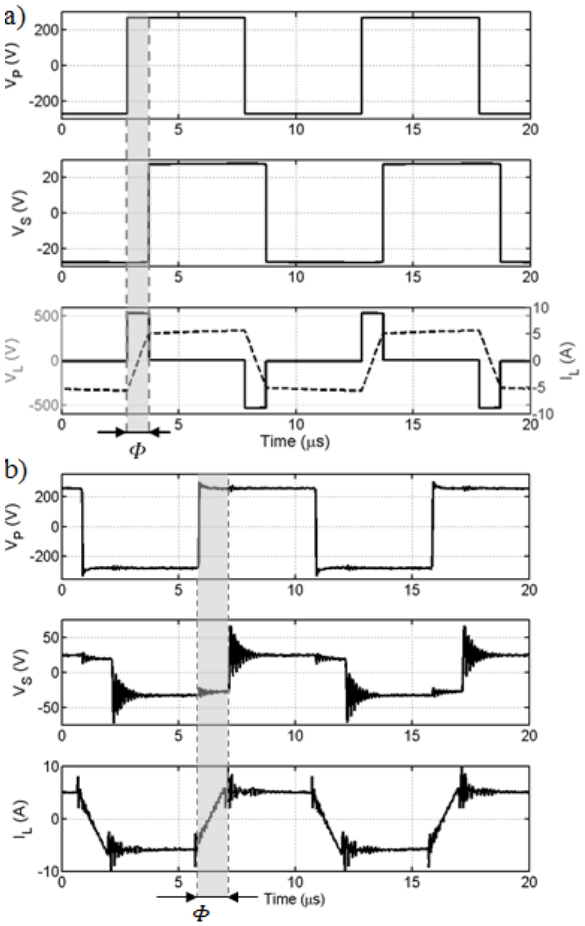

Fig. 2 Representative ideal, a), and experimental, b), waveforms of the DC-DC converter, highlighting the phase-shift, Φ between primary and secondary voltages.

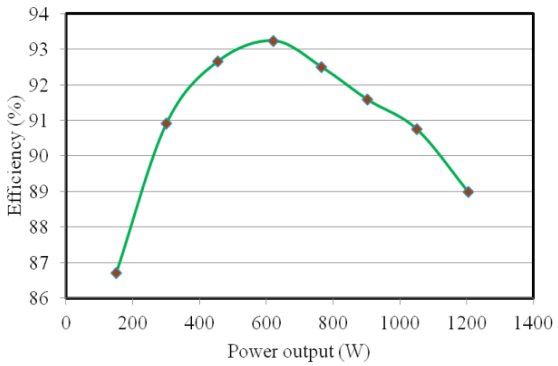

Fig. 3 Measured efficiency of the DC-DC converter.

The resonance involves the transformer leakage inductance and the intrinsic capacitance of the MOSFETs. The ZVS conditions can be kept down to a minimum value of the delivered output power, after which the current in the resonating inductor becomes too small to yield a full charge/discharge of the resonating capacitors. Fig. 4 a) and b) show the experimental drain-source and gate-source voltage waveforms for the primary-side and secondary-side MOSFETs, respectively: these results demonstrate turn-on switching under non-dissipative conditions. ZVS is maintained down to about 30% of the maximum load on the primary side and down to about 12% of the maximum load on the secondary side.

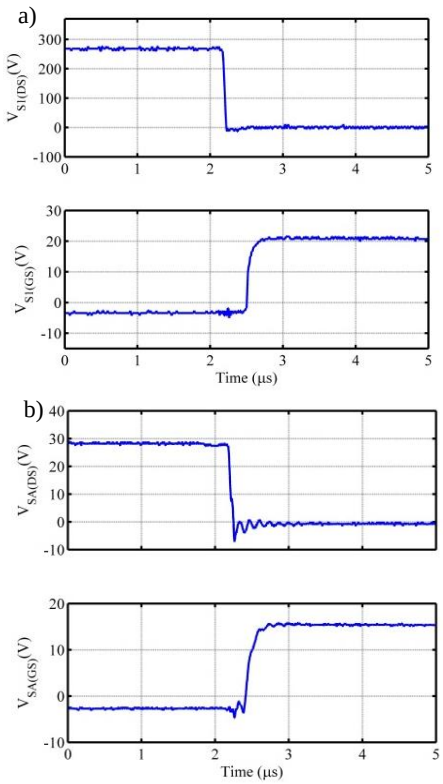

Fig. 4 Drain-source and gate-source voltage of primary-side, a), and secondary-side MOSFETs, b), highlighting zero-voltage turn-on switching of the devices.

2.2. Avalanche-rugged Power MOSFETs

Both transistor types used are avalanche rugged, that is, they can withstand energy dissipation in the avalanche regime. This is an important figure of merit for power transistors, as it enables the design of fully-snubberless robust solutions. Whereas for low-voltage Si devices avalanche-ruggedness is achieved by design with well-established and amply investigated solutions (see [8,9], for example) in SiC

MOSFETs this feature is associated with the material physics and has not yet been thoroughly explored.

Since the CoolMOS transistors suffer from reliability issues when body diode is using for free-wheeling, for this application they are not a suitable substitute of the SiC MOSFETs, despite similar performance in terms of on resistance and current rating.

Fig. 5 shows experimental waveforms of the drain current, I_D, and drain-source voltage, V_{DS}, for unclamped inductive switching of the device: as can be seen, the device can safely withstand avalanche breakdown for a drain-current value of up to more than 10 A, which is more than twice the nominal input current. Its performance and degradation after repeated exposure to such event is under investigation. Other works have independently confirmed the avalanche robustness of SiC MOSFET technology [10].

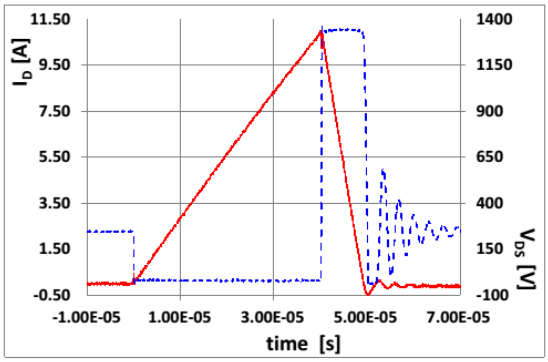

Fig. 5. Representative unclamped inductive switching waveforms for a 650V SiC power MOSFET.

2.3. Thermal management

A significant issue in designing reliable converters is thermal management, with regard to both the active device working temperature and its thermal cycling. To this aim, together with a proper circuit topology and device driving, the optimization of the device cooling plays a key role. To lower as much as possible the steady state temperature of critical devices, first of all, the heatsink design is carried on to maximize the heat transfer rate. However, it is well known [8,9,11] that optimizing cooling to limit as much as possible the amplitude of thermal cycles and the mean temperature has a big impact on extending the maximum achievable lifetime. Both these features should be obtained by increasing the volume of the system as less as possible, then it is mandatory developing a detailed thermal model of the device-heatsink assembly.

3. Heatsink design

3.1. Prototype testing

The prototype of the converter was assembled by mounting the two sections of the converter on separate PCBs and connecting them through the planar transformer. In both the boards, the power transistors were cooled by standard anodized aluminium heatsink (from Ohmite Mfg. Co.).

Fig. 6 shows an overall view of the prototype. Control boards are placed below the power sections.

For the thermally most critical components, which were the, the FA-T220-51E, heatsink, which exhibit a 3.4 K/W natural convection thermal resistance and a weight of 37 g, was used.

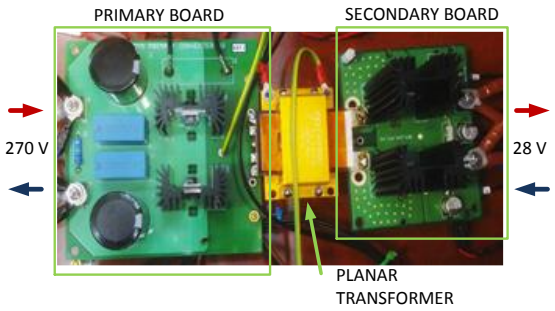

Fig. 6 Overall view of the prototype. From left to right: primary side board, transformer, secondary side board.

Power tests were performed on the prototype with natural and forced air convections. Indeed, in the avionic applications the converter is fan cooled in the nominal operating conditions but, it must be able to operate also in case of fan failure, with 50% power derating.

Fig. 7 shows the IR thermal map of the secondary section at steady state, with a delivered power of 600 W (50% of the maximum power) without fan.

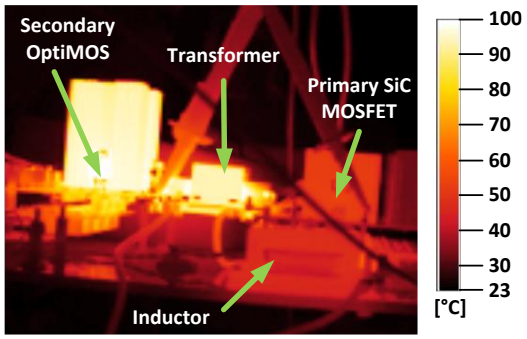

Fig. 7 IR thermal map at steady state, without fan ($P_{delivered}$ = 600 W, T_{amb} = 23 °C).

The same measurements were repeated in forced air conditions, by using a fan with air delivery of 54 l/s, corresponding to an air velocity of about 5 m/s. In this case, the maximum temperature of the secondary MOSFETs package was lowered to 80 °C.

Then, with the same boundary conditions, experiments were carried out increasing the delivered power till 1.2 kW. The dynamic thermal measurements obtained with and without forced air cooling are summarized in Fig. 8.

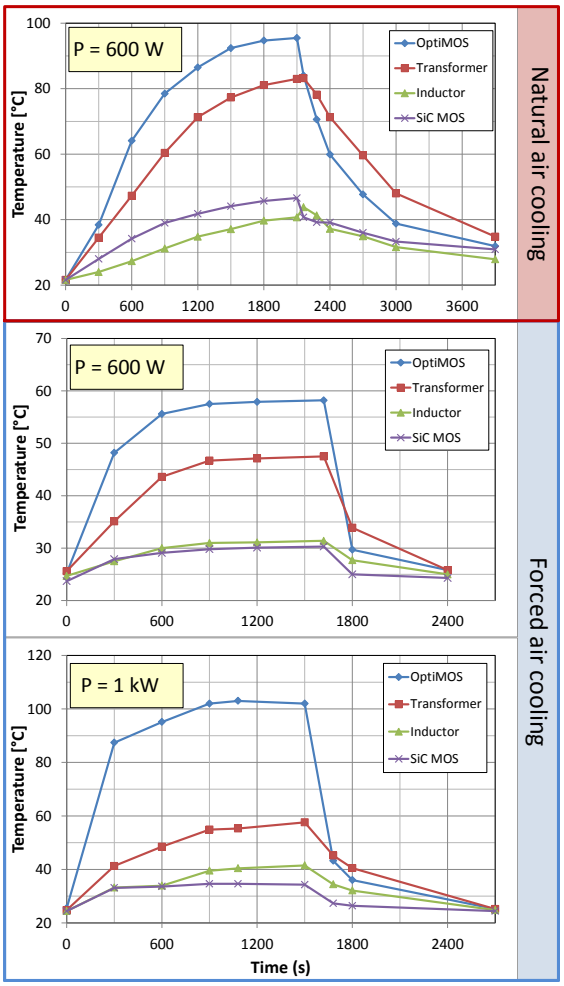

Fig. 8 Dynamic thermal measurements at different power ratings, with and without forced air cooling.

3.2. Thermal model fitting

Once the power losses of active and passive components are minimized by proper choice of topology, components, layout and driving, the only possible way to improve the thermal performances of the converter is the optimization of the thermal path toward the ambient. Due to the strict requirements in term of space, weight, ambient temperature, vibration and reliability, accurate 3D finite elements modelling of the system is an extremely useful step for a proper design.

Moreover, since the system reliability depends not only on the steady state temperature of the components but also from thermal cycles amplitude, dynamic thermal simulations are needed.

To reduce the computational complexity of the whole system thermal transient simulation, a model simplification procedure was adopted, starting from accurate and fixed thermal model of the single components, as described in [12,13]. The power losses of the components were used as heat sources, concentrated in the internal active volume of the devices (in particular we estimated about 4 W of total power losses for each transistor at half load). All the material parameters known from literature and components data-sheets were exploited while some parameters, as thermal contact resistances and, in 20% range, the convective heat exchange coefficient, were used to fit the model with the prototype thermal measurements.

Fig. 9 shows the good agreement obtained at the steady state condition with 600 W of power delivered and natural convection. Once obtained the fitting, the parameters were no more changed into the following simulation.

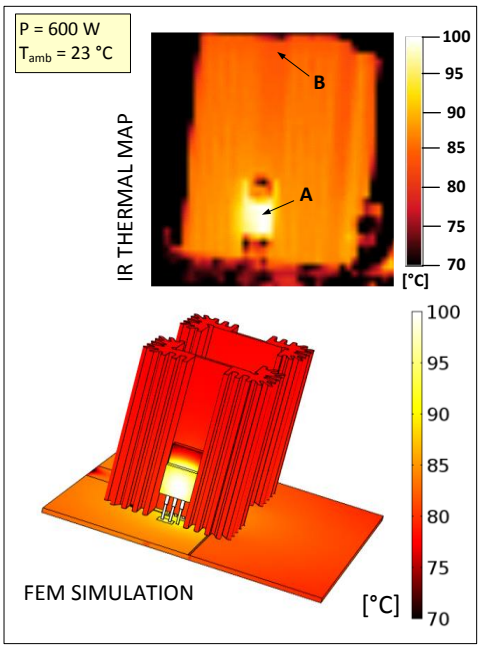

Fig. 9. Infrared thermal map on the secondary MOSFETs package and heatsink with natural convection, and thermal simulation at the same conditions, after fitting procedure.

The thermal transient of the converter secondary side, at the same conditions (50% delivered power and natural convection) was also simulated, without any more fitting, obtaining a good agreement with IR measurements, as shown in Fig. 10.

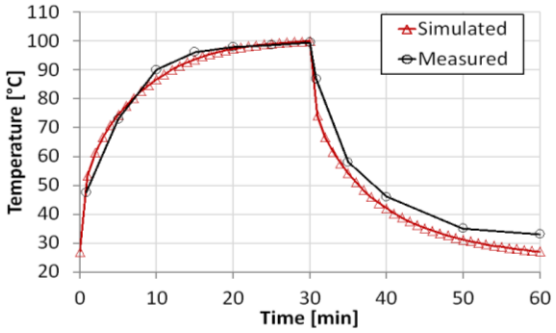

Fig. 10 IR and simulated thermal transient on the top of the secondary MOSFET package at 50% of delivered power and air natural convection (T_{amb} = 27 °C).

Similar good agreement was obtained between measurements and simulation with forced air cooling at the same boundary conditions (Fig. 11). The measurements were not performed at the rated power of 1.2 kW, since the MOSFET junction temperature exceeded the maximum allowed (175 °C) reported in the datasheets, as indicated by the simulation. Simulations indicate that the junction temperature reaches 208 °C at steady state in these operating conditions (on the hypothesis that losses are proportional to the square of the current).

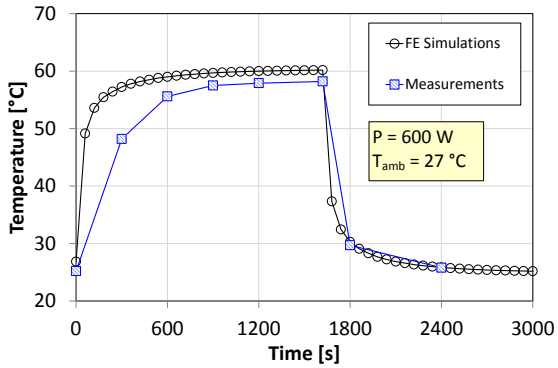

Fig. 11. Thermal transient on the top of the secondary MOSFET package with forced air convection (v = 5 m/s).

3.3. Thermal improvements by FEM design

By the set up FE model we investigate possible solutions to improve the thermal performance of the system, in particular focused on the heat-sink design, to find the best trade-off between thermal resistance and thermal capacitance.

The specific on maximum junction temperature have to be satisfied in both forced (100% rated power) and natural (50% rated power) cooling conditions, while the limitation of thermal cycling amplitude (defined for a period of 30 minutes) must be verified only at the rated power, with forced air cooling, since natural cooling is a condition allowed only in emergency cases.

Fig. 12 shows the simulated thermal map of the secondary side of the converter at the rated power (forced air) with an improved heat sink geometry which occupies the same volume than the previous one and weighs 68 g instead of 37 g. It can be observed that the MOSFETs case temperature reaches 134 °C, while the junction temperature is 164 °C, that is below the limit, but still too high for reliable operation. Moreover the amplitude of the thermal cycles is still too high.

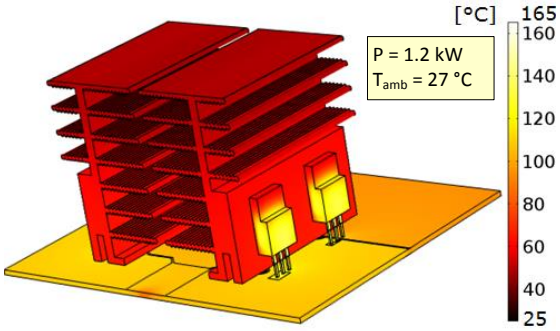

Fig. 12. Improved heatsink: simulated steady-state thermal map at full load. Tj = 164 °C, T_C = 134°C.

A completely new design is possible by choosing a device with a not Full Plastic (not-FP) TO220 package, and using the system chassis (dimensions: 300x100x30 mm^3) as heat-sink ("Chassis solution" in the following), as illustrated in Fig. 13. With this solution the thermal resistance to the ambient can be much lowered, and the heatsink thermal capacitance increases by one order of magnitude so further reducing the thermal cycles amplitude. With the same air forcing apparatus (but placed externally to the chassis, equipped with fins), the system can operate at the rated power with MOSFET's case temperature of 79°C and junction temperature of 83°C. The improvement is even better, considering that all the main heating elements in the converter (primary and secondary side, and the planar transformer) are now taken into account. These simulations were conducted supposing part of the forced air flowing inside the chassis through ventilation slots.

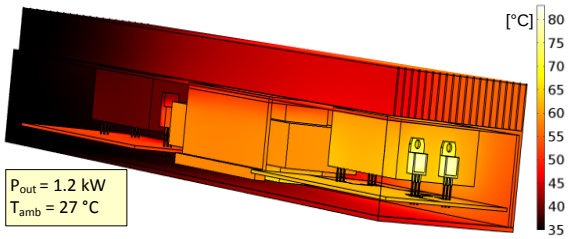

Fig. 13 Chassis solution (secondary side to the right): simulated forced air steady-state thermal map at full load. T_j = 83°C, T_C = 79°C.

Fig. 14 shows the corresponding thermal transient, which appears slower than in the previous solutions (also the prototype layout with not-FP devices is shown). It can be observed that an effective advantage in thermal cycles amplitude could be obtained only for period shorter than few minutes using the Chassis solution.

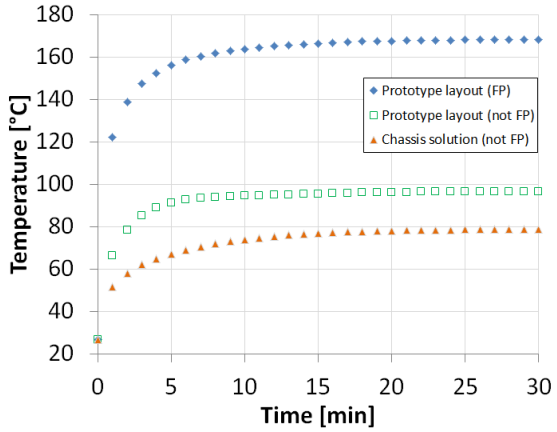

Fig. 14 Case temperature simulated thermal transient at the rated power, with forced air cooling, T_{amb} = 27°C for three of the analized solutions (see legend).

The solution with chassis acting as heat-sink also allows operation in the worst case condition for ambient temperature, which is 75°C in avionic application. In this case it was obtained T_j = 133°C and T_C = 129°C at the secondary side. Also in case of natural convection (half power) the MOSFET still operate under thermal limits, as illustrated in Tab. 1, which recaps the results obtained at different conditions with the last solution.

With ambient temperature of 75°C the planar transformer starts to be critical, since its temperature reaches 107°C, but deeper analysis has to be done on this component for accurate considerations and thermal optimization.

Table 1
Simulated temperatures [°C] obtained with the Chassis solution at different operating conditions.

Operation	T_j	T_C
1.2 kW (forced air 27°C)	83	79
600 W (natural air 27°C)	74	72
1.2 kW (forced air 75°C)	133	129
600 W (natural air 75°C)	124	122

Acknowledgments

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