Single Pulse Avalanche Robustness and Repetitive Stress Ageing of SiC power MOSFETs

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Abstract

This paper presents an extensive electro-thermal characterisation of latest generation silicon carbide (SiC) Power MOSFETs under unclamped inductive switching (UIS) conditions. Tests are carried out to thoroughly understand the single pulse avalanche ruggedness limits of commercial SiC MOSFETs and assess their aging under repetitive stress conditions. Both a functional and a structural characterisation of the transistors is presented, with the aim of informing future device technology development for robust and reliable power system development.

1. Introduction

Silicon Carbide (SiC) power MOSFET fabrication technology has considerably matured over the recent years and therefore, they are now commercially available to buy in large quantities from various different manufacturers. SiC wide band-gap (WBG) power semiconductor devices including MOSFETs are by now a commercial reality [1, 2].

MOSFETs are widely used in high switching frequency applications and hence the assessment of their stability, robustness and reliability is vital for the development of high frequency switching power systems. Of particular importance is the assessment of the device ability to withstand avalanche breakdown regime. In high speed switching applications, back EMF (electromagnetic force) is produced during device turn-off due to the sudden change of current in inductive loads or parasitic elements which may force the MOSFET into drain-to-source avalanche and damage the device [3]. Avalanche ruggedness is an important asset for overall system robustness and enables competitive snubber-less designs.

The avalanche ruggedness of a device is usually assessed under the most rigorous test conditions, i.e. Unclamped Inductive Switching (UIS) conditions (see [4], for instance). Important performance indicators are the device ability to withstand single pulse energy dissipation and modifications in its characteristics as a result of repetitive stress applied. In this work, the capability of state-of-the-art commercially available 1200 V SiC power MOSFETs to dissipate energy during avalanche breakdown under various single-pulse UIS test conditions was investigated and illustrated. The evolution of some critical parameters after repetitive UIS pulses, including gate-source threshold voltage (V_{th}) and body diode forward voltage (V_f), are also reported [5].

2. Experimental results

2.1. Test Setup

The schematics of a UIS test circuit is shown in Fig. 1. In order to avoid heating up the SiC MOSFET (DUT) before avalanche stress was applied, an auxiliary 3kV rated high voltage Si IGBT was connected in parallel to charge up the inductor current. A fixed 16V gate signal was used to drive the IGBT.

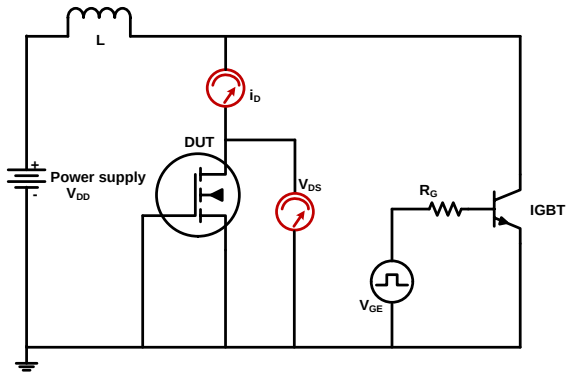


Fig. 1. UIS test circuit schematic

Fig. 2 shows the test circuit based on the circuit schematic in Fig. 1. In order to minimise stray inductance to avoid voltage overshoot, a double sided protoyping circuit board was used as a power plan and the use of wires were minimised by vertically mounting the gate driver directly. The overall capacitor bank is rated at 1.8kV to allow characterisation up to 1.8kV. The DUT is mounted horizontally on a hotplate to allow characterisation at different case temperatures (T_{CASE}) up to 200^{O}C. A high precision digital programmable signal generator was used to ensure fine control of the gate signal with resolution of 10ns.

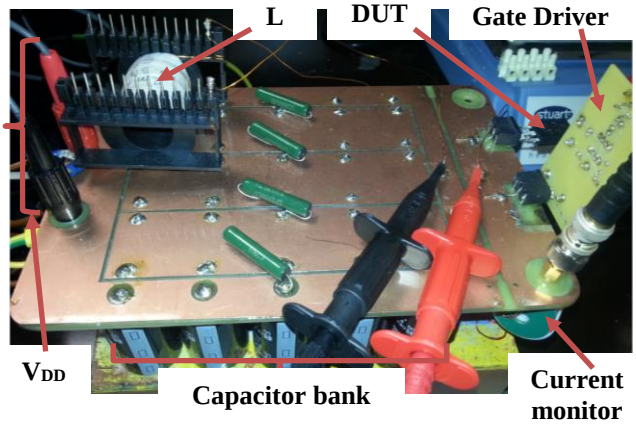


Fig. 2. UIS test circuit

The amount of energy dissipated by the devices during the time in avalanche, t_{AV} can be derived by calculating the time integral of the product of the drain-source voltage V_{DS} and the drain current I_D:

$$E_{AV} = \int_{t=0}^{t=t_{AV}} V_{DS}(t) \cdot I_D(t) dt \qquad (1)$$

Then, solving (1) for the time in avalanche yields:

$$E_{AV} = \frac{1}{2} L I_o^2 \cdot \frac{V_{BD(eff)}}{V_{BD(eff)} - V_{DD}} \qquad (2)$$

where $V_{BD(eff)}$ is the effective drain-source breakdown voltage during t_{AV}, which is not constant due to the thermal evolution of the device and I_{AV} is the current at the start of the avalanche event.

Fig. 3 shows the typical set of waveforms for a non-destructive single-pulse UIS event: V_{GE} is the gate signal applied to the IGBT (red); I_L is the current in the inductor (green) and V_{DS} is the voltage across the SiC MOSFET (blue). As can be seen, V_{DS} is initially equal to V_{DD} when device is OFF (In this study: 400V and 800V) but reaches a breakdown value $V_{BD(eff)}$ ~ 1900V during the UIS event. The actual breakdown voltage $V_{BD(eff)}$ is approximately 55-60% higher than the rated breakdown voltage $V_{BD(DSS)}$ of the device.

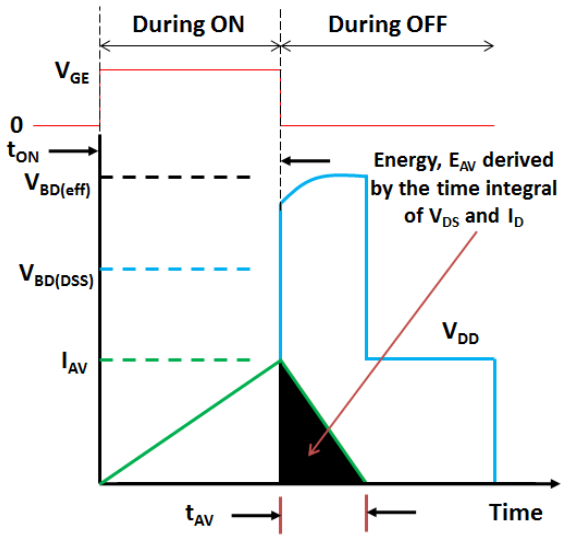
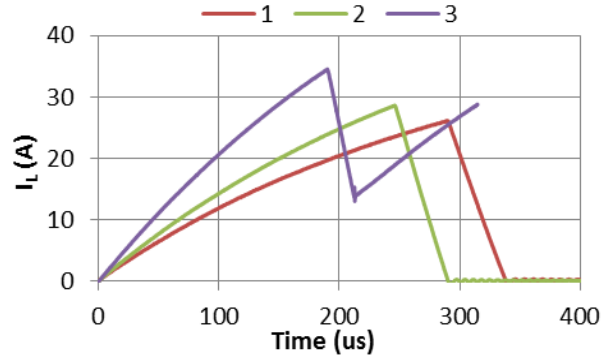


Fig. 3. Typical UIS test waveforms [4]

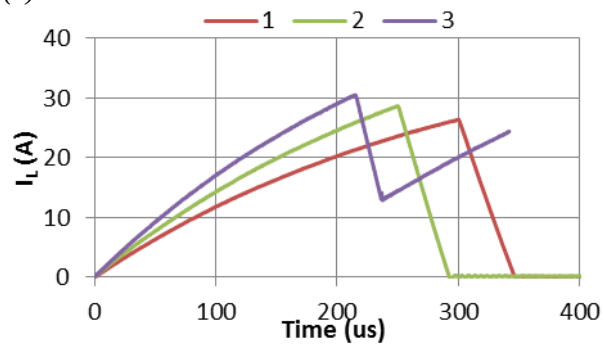
2.2. Single pulse robustness test

The main aim of this single pulse UIS test was to apply the same amount of E_{AV} = 1.2J (ca. 55% of the device rated capability) by varying the rate of avalanche energy dissipation. Different inductance values along with adjustable gate drive pulse enabled

to give different I_{AV} and t_{AV} values in order to obtain the same energy dissipation for all tests. Fig. 4 (a) and (b) show the current waveforms for V_{DD} = 400V and at T_{CASE} of 90^{O}C and 150^{O}C respectively.



(a)



(b)

Fig. 4. Single pulse UIS waveforms at T_{CASE} (a) 90^{O}C and (b) 150^{O}C, V_{DD} = 400V with various L values and constant E_{AV}

The summarised test conditions for the tests corresponding to Fig. 4 (a) and (b) are summarised in Table 1 and 2 respectively.

Table 1 – Test Conditions summary for Fig. 4 (a)

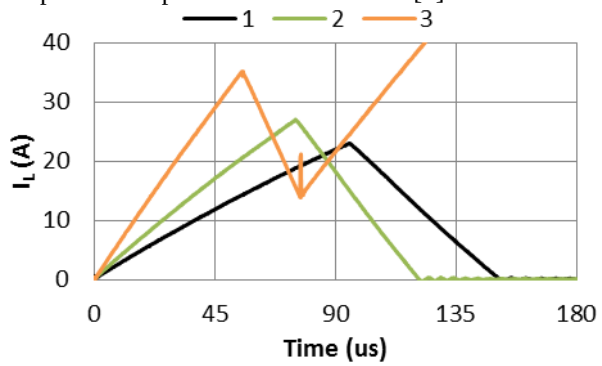
V_{DD} = 400V; T_{CASE} = 90^{O}C; E_{AV} = 1.2J					
#	***I_O (A)***	***L (uH)***	***$V_{BD(eff)}$ (V)***	***t_{ON} (us)***	***t_{AV} (us)***
1	26.2	2765	1849	290	50
2	28.7	2332	1855	246	46
3	**34.5**	**1625**	**1860**	**190**	**38.4**

Table 2 – Test Conditions summary for Fig. 4 (b)

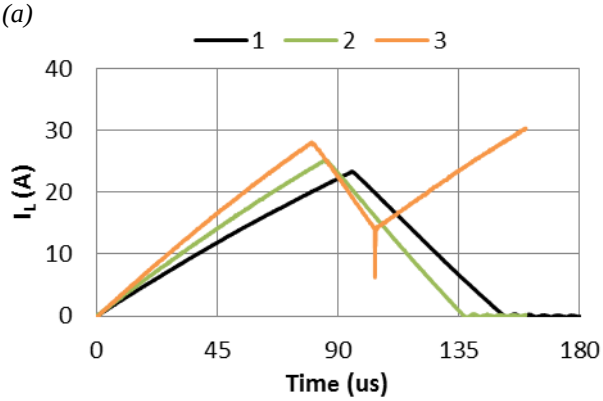
V_{DD} = 400V; T_{CASE} = 150^{O}C; E_{AV} = 1.2J					
#	***I_O (A)***	***L (uH)***	***$V_{BD(eff)}$ (V)***	***t_{ON} (us)***	***t_{AV} (us)***
1	26.5	2723	1900	300	47.7
2	28.5	2316	1902	250	44
3	**30.5**	**1876**	**1906**	**215**	**38**

The current waveforms at V_{DD} = 800V for 2 different T_{CASE} of 90^{O}C and 150^{O}C are shown in Fig. 5 (a) and (b) respectively.

Fig. 4 and 5 show that, even though the E_{AV} value was kept constant, transition from safe UIS to failure was caused by an increased power dissipation rate within the device. This demonstrates the fact that energy dissipation rate also play a role in determining the avalanche failure limits of power MOSFETs along with the E_{AV} value [6]. It is an indication of thermally driven failure type, since the maximum T_J increases as the power dissipation rate is increased [6].



(a)



(b)

Fig. 5. Single pulse UIS waveforms at T_{CASE} (a) 90^{O}C and (b) 150^{O}C, V_{DD} = 800V with various L values and constant E_{AV}

The summarised test conditions for the tests corresponding to Fig. 5 (a) and (b) are summarised in Table 3 and 4 respectively.

Table 3 – Test Conditions summary for Fig. 5 (a)

V_{DD} = 800V; T_{CASE} = 90^{O}C; E_{AV} = 1.2J					
#	***I_O (A)***	***L (uH)***	***$V_{BD(eff)}$ (V)***	***t_{ON} (us)***	***t_{AV} (us)***
1	23.0	2464	1881	95.2	56.3
2	27.0	1885	1885	75.1	46.9
3	**35.2**	**1100**	**1894**	**55.6**	**35.4**

Table 4 – Test Conditions summary for Fig. 5 (b)

V_{DD} = 800V; T_{CASE} = 150°C; E_{AV} = 1.2J					
#	I_O (A)	L (uH)	$V_{BD(eff)}$ (V)	t_{ON} (us)	t_{AV} (us)
1	23.4	2607	1874	95.2	56.8
2	25.3	2282	1885	84.8	53.2
3	**28.2**	**1844**	**1888**	**80.1**	**47.8**

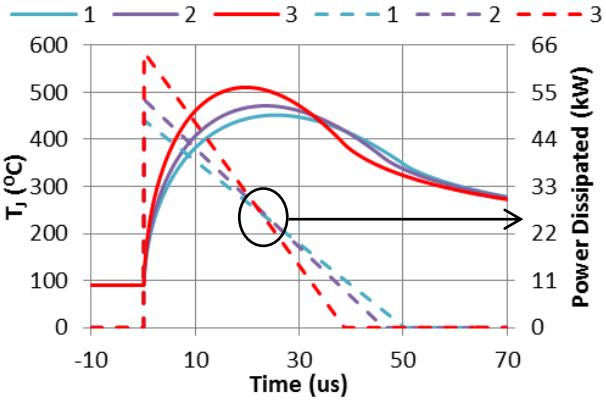


Fig. 6. Simulation of Junction temperature for test conditions from Table 1 at V_{DD} = 400V.

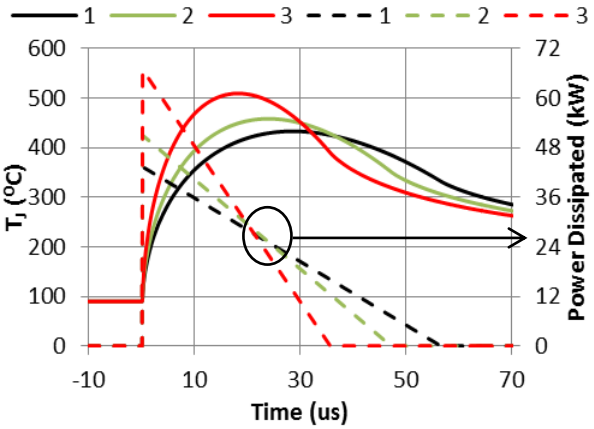


Fig. 7. Simulation of Junction temperature for test conditions from Table 3 at V_{DD} = 800V.

The T_J simulations in PSpice (solid lines) for tests at 90°C at 400V and 800V are included in Fig. 6 and 7 respectively to illustrate the critical T_J reached at failure. A physics-based 1-D compact equivalent circuit usually used for analysis of short transients in semiconductor chips was implemented for modelling the thermal performance of the device (see [7], for instance). The simulated critical T_J at failure test conditions for 400V and 800V is 511°C and 510°C respectively. A more detailed study on single-pulse transient UIS tests can be found in [4], [8]. Preliminary thermal maps showing temperature distribution in the chip (3.1 x 3.1 mm) before failure are included in the next section. A more detailed thermal measurement study is still needed before a conclusive explanation could be provided behind the cause of failure.

2.3. Transient IR thermal measurements

In order to detect information regarding the temperature distribution during avalanche operation, an ultrafast IR mapping system has been used on bare dies [9, 10]. Since the experimental set-up uses an equivalent time technique, only two thermal maps were taken at t_1 and t_2 (see Fig. 8) during each UIS test to avoid an excessive electro-thermal stress applied to the DUT. Thermal measurements have been carried out during three different UIS tests depicted in Fig. 8. In order to attain quantitative and calibrated information from the radiance data detected by the IR Camera, the emissivity map of the target surface has been evaluated using the "two point calibration" [11]. As a consequence, after a correction algorithm, thermal maps report good estimations of the device surface temperature.

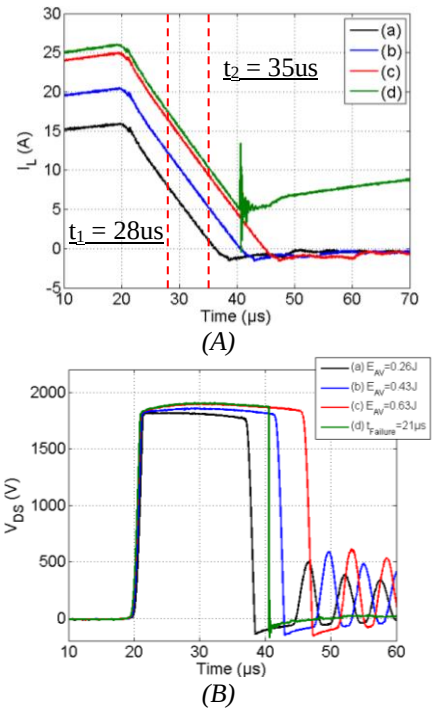


Fig. 8. UIS electrical waveforms: (A) I_L and (B) V_{DS}, with T_{CASE} = 27°C; L = 1.8mH; (a) V_{DD}=140V, t_{ON} = 200us (b) V_{DD}=180V, t_{ON}=200us (c) V_{DD}=200V, t_{ON}=220us; (d) V_{DD}=200V, t_{ON}=230us.

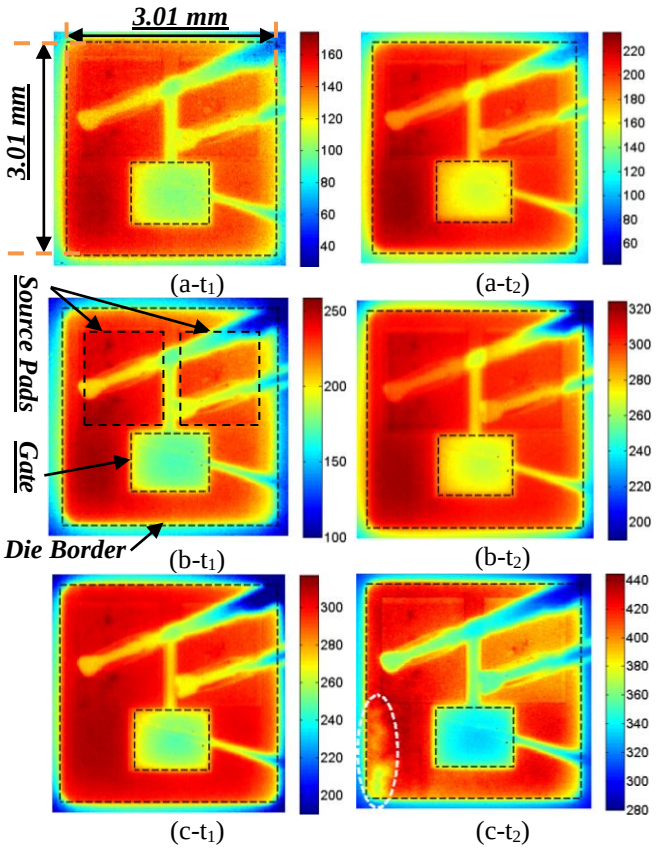


Fig. 9. Thermal maps taken during UIS tests of Fig. 8. The time instants are t_1=28us, t_2=35us.

During each tests, T_{CASE} has been fixed to 27°C. Referring to Fig. 9, in the first case (a) the device reached a maximum temperature of 225°C; the temperature distribution evidences a non-uniformly distributed avalanche current, with hottest area situated in the lower-left corner. In case (b) and (c), the temperature maps show peak temperatures of about 320°C and 442^{O}C respectively. In the last thermal measurement, IR maps show that: (i) at time t_1 the temperature distribution is quite uniform with a hottest point in the lower-left corner near the termination area (ii) at time t_2, the DUT undergoes a structural damage at the hottest point. This affirmation is based on the observation of an uneven temperature decrease just close to the previous hottest point.

Thermal maps in Fig. 9 for test conditions just before failure indicate damage to some cells in the lower-left corner of the chip and thus they are not conducting as much current as the other cells are and thus the reason for the temperature drop (dotted line). The simulated critical T_J was 510^{O}C and 511^{O}C for 2 different test conditions for the same E_{AV} but different V_{DD} which correlates to the chip temperature of 442^{O}C just **before** failure. The chip temperature and simulation T_J are quite close to each other and hence it is confirmed that the failure occurs when the critical T_J is reached inside the device as opposed to the failures seen in Si where the failures were caused due to the physics of the device. This is also an indication of the added robustness that could be achieved in SiC MOSFETs if structural related issues are addressed to fully utilize the capabilities of SiC WBG material.

2.3. Ageing test

For the ageing test, the device was subjected to a repeated dissipation of constant E_{AV} level well below its nominal maximum rating. This test was carried out at a fixed V_{DD} of 400V and T_{CASE} of 150^{O}C. The delay between the pulses was set to 2 s to allow the device to cool down. The device was turned OFF at I_{AV} of 35A with a t_{AV} of 22us which equalled to about E_{AV} = 0.7J. In order to monitor the changes in device characteristics, two parameters named the gate threshold voltage (V_{th}) and body diode forward voltage (V_f) were measured at regular intervals. All of these parameters show a marked deviation from the initial value, already after few thousand pulses. A total of 669k pulses were sent to the device and all the measurements obtained for V_{th} and V_f differ from the previous ones which demonstrates continuous degradation taken place in the device.

For this particular investigation, V_{th} is defined as the gate-source voltage when the drain current is equal to 5mA. Fig. 10 shows the evolution of gate-source V_{TH} when subjected to a repetitive E_{AV} of 0.7J at T_{CASE} of 150^{O}C, which highlights a considerable degradation of the device characteristics.

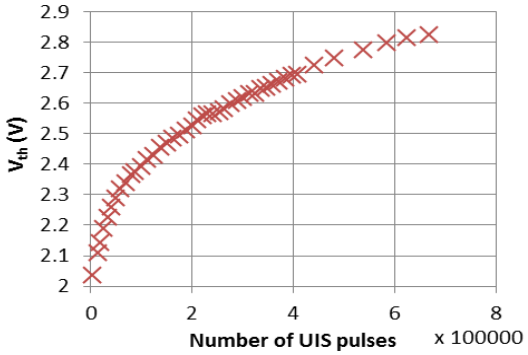


Fig. 10. Evolution of gate-source threshold voltage (V_{th}) as a result of repetitive UIS stress

Fig. 10 shows that the V_{TH} has a positive shift as the number of UIS pulses increase. The shift of the V_{TH} is

due to the interfacial charge (electrons for n-channel) trapped at and near the SiO_2-SiC interface and therefore leads to a significant degradation of the device performance by not only reducing the effective channel mobility considerably but also by shifting the threshold voltage [12].

The V_{TH} instability of SiC power MOSFETs is an ongoing area of research and previous studies show that the V_{th} instability can be reduced by applying a nitric oxide (NO) or nitrous oxide (N_2O) postoxidation anneal during the device manufacturing stage. Improvement of V_{TH} stability is a major requirement in the development of technologically matured SiC power MOSFETs to allow power electronics circuitry solely based on SiC devices [12,13].

Power MOSFETs have a parasitic body diode which consists of the source-drain p-n junction. Fig. 11 shows how the V_f changed during the test. During the avalanche event, the current flows through the body diode of the device and hence this quantity gives an indication of the impact that repetitive avalanche stress had on the body diode.

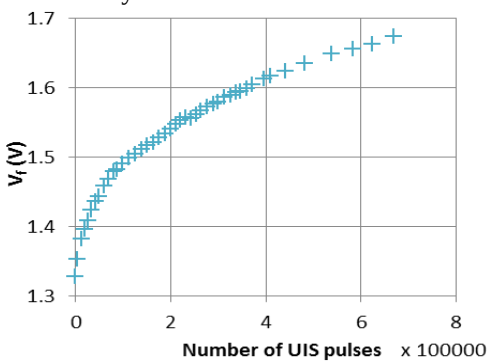


Fig. 11. Evolution of body diode forward voltage (V_f) as a result of repetitve UIS stress

The body diode V_f of the SiC MOSFET also has a positive shift as the number of UIS pulses increase. The basal plane dislocations present in the substrate and epilayers give rise to the growth of stacking faults. The growth of stacking faults sufficiently kill the lifetime of minority carriers which effectively prevent conduction modulation through them and therefore results in an increase of V_f. Manufacturers have encountered this problem in the past and found that improvements in the growth process of thick epitaxial layer using hot wall chemical vapor deposition (CVD) results in reduction of the density of basal plane defects in the blocking layer of the device which has allowed large area power diodes with no V_F degradation [14].

3. Conclusions

This paper presented a detailed functional as well as structural characterisation of state of the art commercial 1200V SiC power MOSFETs under single-pulse and repetitive UIS test conditions to demonstrate robustness and avalanche ruggedness. The single pulse robustness test show that not only the E_{AV} but also the rate of power dissipation plays a role in determination of avalanche failure. The thermal maps are comparable with the T_J simulation confirming that the failure is related to critical T_J being reached inside the chip and as a result some cells are damaged. The repetitive results show a continuous degradation of the device characteristics. The results show that SiC MOSFETs have a sufficient level of robustness which is hindered by the structure and packaging related issues which need to be further researched upon in order to allow a step forward towards the development of robust and reliable power systems based on SiC devices.

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