

A Simple Current Control Strategy for a Four-Leg Indirect Matrix Converter

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Abstract—In this paper the experimental validation of a predictive current control strategy for a four-leg indirect matrix converter is presented. The four-leg indirect matrix converter can supply energy to an unbalanced three-phase load whilst providing a path for the zero sequence load. The predictive current control technique is based on the optimal selection among the valid switching states of the converter by evaluating a cost function, resulting in a simple approach without the necessity for modulators. Furthermore, zero dc-link current commutation is achieved by synchronizing the state changes in the input stage with the application of a zero voltage space vector in the inverter stage. Simulation results are presented and the strategy is experimentally validated using a laboratory prototype.

Index Terms—AC-AC Conversion, Matrix Converter, Four Leg Converters, Current Control, Predictive Control, Modulation Schemes

NOMENCLATURE

\mathbf{i}_s	Source current	$[i_{sA} \ i_{sB} \ i_{sC}]^T$
\mathbf{v}_s	Source voltage	$[v_{sA} \ v_{sB} \ v_{sC}]^T$
\mathbf{i}_i	Input current	$[i_A \ i_B \ i_C]^T$
\mathbf{v}_i	Input voltage	$[v_A \ v_B \ v_C]^T$
i_{dc}	dc-link current	
v_{dc}	dc-link voltage	
\mathbf{i}	Load current	$[i_u \ i_v \ i_w]^T$
\mathbf{v}	Load voltage	$[v_u \ v_v \ v_w]^T$
\mathbf{i}^*	Load current reference	$[i_u^* \ i_v^* \ i_w^*]^T$
C_f	Filter capacitor	
L_f	Filter inductor	
R_f	Filter resistor	
R	Load resistance	
L	Load inductance	

I. INTRODUCTION

In recent years, the interest in matrix converters applications has increased [1]–[3]. Matrix converter topologies offer an “all silicon solution” for ac-ac power conversion, achieving sinusoidal input and output waveforms with bidirectional power flow and being capable of operating under high temperatures

and pressures [4]–[6]. Moreover, due to the absence of electrolytic capacitors, matrix converters could be more compact, robust and reliable when compared to conventional topologies [2].

Compared to a conventional back-to-back converter, the physical space saved by a matrix converter has been estimated as 60%. This characteristic makes the matrix converter a suitable topology for specific applications such as wind-diesel topologies, distributed generation applications, emergency vehicles, military and aerospace applications, external elevators for building construction and skin pass mills [2], [7], [8].

As reported in [6], there are a number of different topologies for direct ac-ac converters. Among them, the indirect matrix converter (IMC) has a similar performance to the standard direct matrix converter (DMC). The IMC is very similar to a back-to-back converter but includes bi-directional switches in the rectifier and has no dc-link capacitor. The lack of a storage element offers the possibility to reduce losses because the commutation of the input stage can be achieved with zero dc-link current [9], [10].

When energy is supplied to a three-phase load it may be necessary to take into account the unbalance nature of the load and the need for a path for the zero sequence current. This path could be provided by connecting the neutral of the load to the neutral point of a zig-zag transformer [11]–[13]. However, this topology could be costly and bulky. Another option is to use a four-leg voltage source converter (VSC) on the load side where the fourth leg would then provide the needed neutral connection for the load. As reviewed in [14], there are several topologies that can handle zero sequence voltage and current caused by an unbalanced source and/or load in three-phase four-wire systems. As reported in [15]–[18], a matrix converter can also be used to supply energy to an unbalanced three-phase load.

The four-leg indirect matrix converter (4Leg-IMC) can be controlled and modulated using a carrier-based pulse width modulation (PWM) and three-dimensional space vector modulation (3D-SVM) techniques [17]–[22]. Compared to

the carrier-based PWM technique, the 3D-SVM offers many advantages such as good dc-link utilization and minimum output distortion, but it has complex modeling and a higher computational requirements and is therefore not intuitive for implementation [21], [22].

Model predictive control (MPC) is an attractive alternative to the aforementioned classical methods due to its fast dynamic response and simple concept as well as the possibility to include constraints in the design of control. The first time that the idea of use a predictive controller for current control in power electronics was presented was in [23]. This was a unique very early paper, and very advanced for the time. This paper had a reduced impact at that time, mainly because microprocessors and the theory for predictive control were not sufficiently developed. Nowadays this idea constitutes a real alternative for the control of power converters as reported in [24]–[26]. Thanks to the sustained increase of computational power of control platforms (such as digital signal processors (DSPs), field programmable gate arrays (FPGAs) and dSPACE controllers) [27], now is possible the implementation of predictive control techniques as well as other more complex techniques such as fuzzy, adaptive, sliding mode and genetic algorithms [28]–[31].

MPC techniques have been demonstrated as a potential alternative to control very complex power converters topologies such as matrix converters [26]. In fact, [30], [32]–[42] have been presented several implementations for direct and indirect topologies. In [32], [33], [42] a predictive current control with instantaneous reactive power minimization has been proposed for both the three-phase direct and indirect matrix converter, which has been evaluated using a clean ac-source [32], [42] and a distorted ac-supply [33]. The main issue observed was that an instantaneous reactive power minimization can obtain input currents in phase with its respective source voltage but it cannot ensure a sinusoidal waveform when distortion is presented in the ac-source. In order to solve this issue, different implementations were proposed by the authors and summarized in [38]. Among them, an active damping implementation was proposed in [34], [35] to improve the input current behavior but this strategy mitigates only the current harmonics produced by the input filter and commutation of the switches but cannot mitigate any distortion of the ac-supply. An imposed waveform for the input current was proposed in [36], [37] which effectively improves the input current but at the cost of an increased switching frequency. Other techniques such a fuzzy implementation in combination with predictive control and a predictive torque control for an induction machine fed by a direct matrix converter were proposed in [30] and [40], [41], respectively, but at the cost of a more complex mathematical and prediction model.

This paper presents the experimental use of finite-set model predictive control (FS-MPC) for the current control of 4Leg-IMCs. As reported in [43]–[45], the FS-MPC utilizes an optimization function that considers all possible switching states. However, due to the discrete nature of the power converters and since the 4Leg-IMC has a finite number of switching states (sixteen for the inverter side and nine for the rectifier side), the predictions and optimizations are greatly simplified; and

can thus be digitally implemented in current microprocessors. Moreover, this scheme does not require internal current control loops nor does it require modulators, thus its complexity is greatly reduced. In [43] the mathematical model of the converter and the predictive current control strategy were introduced and the method is validated using simulation results. An improved control strategy was introduced in [44] in order to reduce the common mode voltage. [45] presents a predictive voltage control strategy which is very different to the idea presented and experimentally validated in this paper. In this paper the topology of the converter is different because it includes an output filter which requires also a different mathematical and prediction model.

In this paper the main novelty and contribution are:

- Experimental implementation of a predictive current control strategy for a four-leg indirect matrix converter. To the best of our knowledge this is the first publication where a predictive current control strategy has been experimentally implemented and validated for a four-leg indirect matrix converter, which constitutes the main contribution of this paper.
- The experimental implementation of the zero dc-link current commutation strategy and delay compensation needed for discrete implementations.

II. FS-MPC OPERATING PRINCIPLE IN POWER CONVERTERS

As mentioned in [24], [26], [46], FS-MPC considers a finite number of valid switching states for the converter to solve, at every sampling time T_s , an optimization problem. Each valid switching state is considered to predict the behaviour of the system by using a discrete model. The number of predictions is given by the number of valid switching states of the converter. Each prediction is compared with its respective reference using a predefined cost function. The switching state that minimizes this cost function is finally selected to be applied in the converter during the next sampling time. This is done without the need of any modulation stage.

A. Generalized FS-MPC Operating Principle

The basic structure of the FS-MPC strategy can be summarized as shown in Fig. 1, where:

- n : number of valid switching states of the converter.
- $\mathbf{x}(k)$: variables used in the model to calculate the predictions for each one of the n possible valid switching states of the converter.
- $\mathbf{x}^p(k+1)$: n prediction variables.
- $\mathbf{x}^*(k+1)$: reference variables.

In order to explain the basic structure and operating principle of FS-MPC the predictive current control strategy is considered for a well know two-level voltage source inverter (2L-VSI), but this explanation could be easily extended to other topologies.

The predictive current control strategy is performed by:

- 1) Measuring the load currents ($\mathbf{x}(k) = \mathbf{i}(k)$).

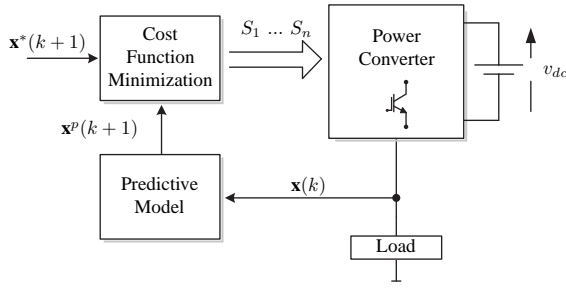


Figure 1. Operating principle of the FS-MPC.

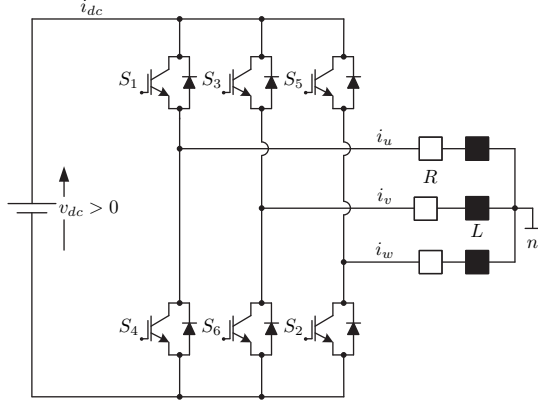


Figure 2. Three-phase voltage source inverter.

- 2) Predicting the behaviour of the load currents for each valid switching state of the converter ($\mathbf{x}^p(k+1) = \mathbf{i}^p(k+1)$).
- 3) Evaluating the cost function g for each prediction.
- 4) Selecting the switching state that minimizes the cost function g_{min} .
- 5) Applying the new switching state to the converter during the next period $k+1$.

In order to predict the load current a mathematical model of the converter and load is necessary. The basic structure of the 2L-VSI is shown in Fig. 2. Each leg contains two switches that connect the load to either the positive or negative line. As an operating constrain, only one switch on each leg must be conducting in order to avoid a short-circuit of the dc-link and to avoid interrupt the load current due to the inductive characteristic of the load. Thus, only two possible switching states are valid in each leg. Since this is a three-phase converter, a total of eight valid switching states can be applied, these are summarized in Table I.

It can be deduced from Fig. 2 that the output voltages are synthesized as a function of the inverter switching states and dc-link voltage:

$$\mathbf{v} = \begin{bmatrix} v_u \\ v_v \\ v_w \end{bmatrix} = \begin{bmatrix} S_1 - S_4 \\ S_3 - S_6 \\ S_5 - S_2 \end{bmatrix} v_{dc} \quad (1)$$

If a passive $R-L$ load is considered, the following relation can be formed:

$$\mathbf{v} = L \frac{d\mathbf{i}}{dt} + R\mathbf{i} \Rightarrow \frac{d\mathbf{i}}{dt} = \frac{\mathbf{v} - R\mathbf{i}}{L} \quad (2)$$

Table I
VALID SWITCHING STATES ON THE 2L-VSI.

State	S_1	S_2	S_3	S_4	S_5	S_6
1	1	1	0	0	0	1
2	1	1	1	0	0	0
3	0	1	1	1	0	0
4	0	0	1	1	1	0
5	0	0	0	1	1	1
6	1	0	0	0	1	1
7	1	0	1	0	1	0
8	0	1	0	1	0	1

where $\mathbf{i} = [i_u \ i_v \ i_w]^T$. A discrete model is necessary to perform the calculation and implementation of the predictive controller in a digital processor. By approximating the derivative $\frac{d}{dt}\mathbf{i}$ by:

$$\frac{d}{dt}\mathbf{i} \approx \frac{\mathbf{i}(k+1) - \mathbf{i}(k)}{T_s} \quad (3)$$

and replacing this in eq.(2), the following discrete form of the load current equation, is obtained:

$$\mathbf{i}(k+1) = \frac{T_s}{L}\mathbf{v}(k) + \left(1 - \frac{RT_s}{L}\right)\mathbf{i}(k) \quad (4)$$

where $\mathbf{i}(k)$ correspond to the measurement of \mathbf{i} at instant k and $\mathbf{v}(k)$ is given as a function of the valid switching states and the measurement of v_{dc} at instant k , based on eq.(1).

The prediction of $\mathbf{i}(k+1)$ is compared with a predefined reference $\mathbf{i}^*(k+1)$ in a cost function, defined as:

$$g(k+1) = |\mathbf{i}^*(k+1) - \mathbf{i}(k+1)| \quad (5)$$

$\mathbf{i}^*(k+1)$ can be extrapolated by using the present and previous values of the current reference as:

$$\mathbf{i}^*(k+1) = 3\mathbf{i}^*(k) - 3\mathbf{i}^*(k-1) + \mathbf{i}^*(k-2) \quad (6)$$

If T_s is sufficient small, then for simplicity it can be assumed that $\mathbf{i}^*(k+1) \approx \mathbf{i}^*(k)$. The switching state that minimizes $g(k+1)$ is selected and applied to the converter during the next sampling time and this procedure is repeated at every sampling time.

As the main objective of this section is provide to the reader a general overview of the operating principle of FS-MPC, there are some issues that have not been considered in this paper but have already discussed in [26]. Among them the most critical issues that must be taken into consideration are uncertainties in the prediction model, mainly due to parameters variations under different operation conditions and also measurement errors, other discretization methods instance Euler approximations, horizon predictions longer than one and the cost function to be considered (quadratic, square, absolute error, etc.).

III. FOUR-LEG INDIRECT MATRIX CONVERTER (4LEG-IMC)

The topology of the 4Leg-IMC is shown in Fig. 3. This circuit consists of two power stages: the rectifier with bidirectional switches and a three-phase, four-leg voltage source

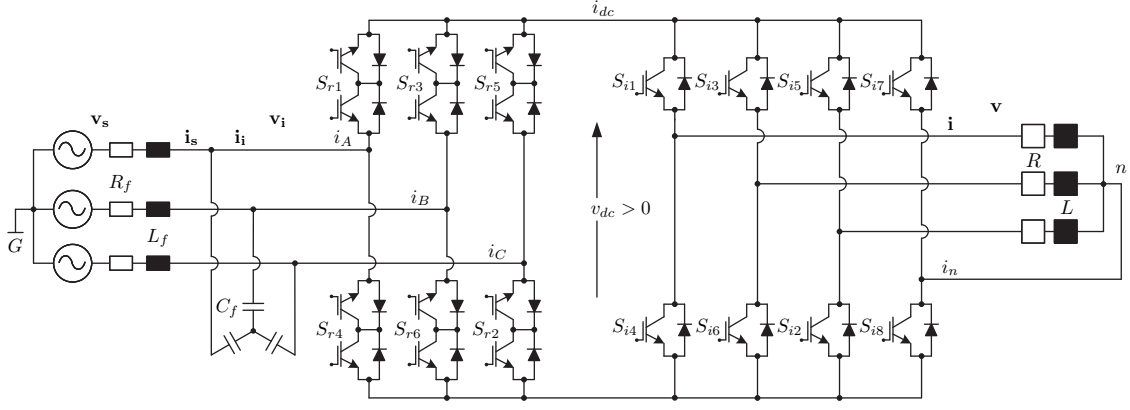


Figure 3. Circuit topology of a four-leg indirect matrix converter.

inverter with unidirectional switches. Both stages are linked by a dc-link without any storage element; its weight and size are thus reduced and the reliability of the system is improved when compared to conventional topologies. A filter is required at the input side in order to protect the converter from over-voltages as well as to mitigate the harmonic content in the input current due to the commutation of the switches.

From Fig. 3 is possible to identify the relation between input and output variables of the converter in order to define its mathematical model. The dc-link voltage v_{dc} is given as a function of the the input voltage $\mathbf{v}_i = [v_A \ v_B \ v_C]^T$, and the instantaneous input transfer matrix as:

$$v_{dc} = T_r \mathbf{v}_i \quad (7)$$

with

$$T_r = [S_{r1} - S_{r4} \quad S_{r3} - S_{r6} \quad S_{r5} - S_{r2}] \quad (8)$$

Similarly, the input currents $\mathbf{i}_i = [i_A \ i_B \ i_C]^T$ can be synthesized as a function of the dc-link current i_{dc} and the transpose of the matrix T_r :

$$\mathbf{i}_i = T_r^T i_{dc} \quad (9)$$

The dc-link current i_{dc} is defined as a function of the output current vector $\mathbf{i} = [i_u \ i_v \ i_w]^T$ and the instantaneous transfer matrix of the inversion stage:

$$i_{dc} = T_i \mathbf{i} \quad (10)$$

with

$$T_i = [S_{i1} - S_{i7} \quad S_{i3} - S_{i7} \quad S_{i5} - S_{i7}] \quad (11)$$

The output three-phase voltage $\mathbf{v} = [v_u \ v_v \ v_w]^T$ can be synthesized as a function of the dc-link voltage v_{dc} and the transpose of the matrix T_i :

$$\mathbf{v} = T_i^T v_{dc} \quad (12)$$

The neutral current i_n circulating through the fourth-leg is given by:

$$i_n = i_u + i_v + i_w \quad (13)$$

As mentioned above, a filter is used on the input side in order to avoid over-voltages and mitigate the harmonic distortion

caused by the commutations. This filter has a second order model defined as:

$$L_f \frac{d\mathbf{i}_s}{dt} = \mathbf{v}_s - \mathbf{v}_i - R_f \mathbf{i}_s \quad (14)$$

$$C_f \frac{d\mathbf{v}_i}{dt} = \mathbf{i}_s - \mathbf{i}_i \quad (15)$$

where L_f is the inductance, R_f the resistor and C_f the capacitor of the input filter.

On the output side, and assuming a resistive-inductive load, the following equation describes the behavior of the load:

$$L \frac{d\mathbf{i}}{dt} = \mathbf{v} - R \mathbf{i} \quad (16)$$

with R and L being the load resistor and inductance, respectively. Table II and Table III summarize the respective switching states of the 4Leg-IMC, which are valid for the formulation of the mathematical model of the converter and they must be taken into consideration by the predictive algorithm.

These tables correspond to the nine and sixteen valid switching states for the rectifier and the inverter stages, respectively. By considering the constraints of no short circuits at the input and no open lines in the output, there are one-hundred forty-four possible switches combinations for the 4Leg-IMC. Another operational condition for this converter is that the dc-link voltage must always be positive $v_{dc} > 0$. As indicated in eq. (7), the dc-link voltage is synthesized by the rectifier stage switches and the input voltages \mathbf{v}_i . At any instant, only three of the nine valid switching states can be applied to the rectifier stage to produce a positive dc-link. For this reason, at every sampling time, only three of the nine valid switching states are considered [9], [32]. The number of valid switching states is therefore reduced to forty-eight. It should be noted that the 4Leg-IMC topology includes an extra degree of freedom that alleviates the complexity of the commutation sequence, the zero dc-link current commutation. This approach has been introduced in [5], [9], [32] and commutates the three-phase to two-phase matrix converter (rectifier stage) during a freewheeling operation when either all the upper devices or all the lower devices in the inverter circuit are gated. It is important to make sure that short circuit of the input lines is avoided. The open circuit of the load in this case would not cause any problem as the dc-link current would be zero.

Table II
VALID SWITCHING STATES ON THE RECTIFIER STAGE.

State	S_{r1}	S_{r2}	S_{r3}	S_{r4}	S_{r5}	S_{r6}
1	1	1	0	0	0	0
2	0	1	1	0	0	0
3	0	0	1	1	0	0
4	0	0	0	1	1	0
5	0	0	0	0	1	1
6	1	0	0	0	0	1
7	1	0	0	1	0	0
8	0	0	1	0	0	1
9	0	1	0	0	1	0

Table III
VALID SWITCHING STATES ON THE INVERTER STAGE.

State	S_{i1}	S_{i2}	S_{i3}	S_{i4}	S_{i5}	S_{i6}	S_{i7}	S_{i8}
1	1	1	0	0	0	1	0	1
2	0	1	1	1	0	0	0	1
3	0	0	0	1	1	1	0	1
4	1	1	1	0	0	0	0	1
5	1	0	0	0	1	1	0	1
6	0	0	1	1	1	0	0	1
7	1	0	1	0	1	0	0	1
8	0	1	0	1	0	1	0	1
9	1	1	0	0	0	1	1	0
10	0	1	1	1	0	0	1	0
11	0	0	0	1	1	1	1	0
12	1	1	1	0	0	0	1	0
13	1	0	0	0	1	1	1	0
14	0	0	1	1	1	0	1	0
15	1	0	1	0	1	0	1	0
16	0	1	0	1	0	1	0	1

The zero dc-link current commutation therefore allows a dead-time commutation of two bidirectional switches on the input side during the period of time while the inverter stage is in a freewheel state. At first sight the main advantage of this commutation technique is the reduction in the switching losses of the input stage which would be negligible as it can be arranged to commute at zero current.

IV. PROPOSED PREDICTIVE CURRENT CONTROL STRATEGY FOR THE 4LEG-IMC

A. Control scheme

The control strategy validated experimentally in this paper is shown in Fig. 4. The aim of this method is to determine the optimum switching state of the converter, which generates the least amount of tracking error with respect to the load reference, and to apply this state at the next commutation. Further, the control strategy must also assume a positive voltage in the dc-link. To comply with both of these objectives, the control strategy is broken down into the following steps:

- 1) The reference of the output current is defined as $i^*(k+1)$. The input voltage $v_i(k)$ is measured and also the output current $i(k)$.
- 2) These measurements and the model of the system are used to estimate $v(k+1)$; then, $v_{dc}^p(k+1)$ and the output current $i^p(k+1)$ are predicted for the next sample period for each of the valid switching states of 4Leg-IMC.

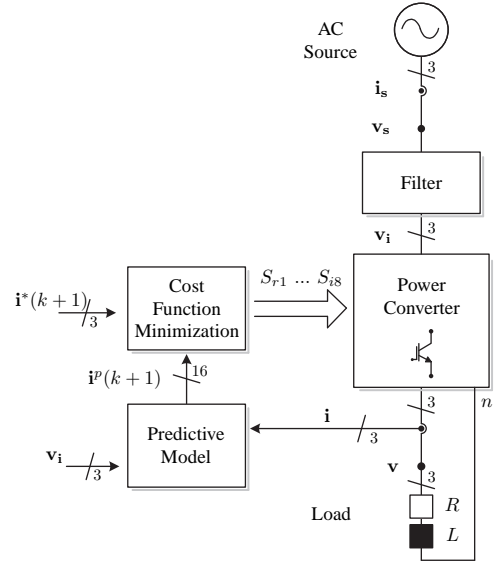


Figure 4. Proposed predictive current control scheme for the 4Leg-IMC.

- 3) Finally, the predictions are evaluated in a cost function g . The state which generates the least tracking error will be applied during the next sampling time.

B. Prediction model

The discrete nature of power converters and control platforms gives rise to the requirement that the system equations be formulated in discrete time. The voltage v_{dc} is defined by the input voltage at 4Leg-IMC v_i and the matrix of the rectifier states T_r . Therefore, the dc-link voltage in the next sample time $k+1$ is given by the following expression:

$$v_{dc}(k+1) = T_r(k+1)v_i(k). \quad (17)$$

The discrete expression of the output current i is obtained by using the Euler approximation as follows:

$$i(k+1) = \frac{T_s}{L}v(k) + \left(1 - \frac{R}{L}T_s\right)i(k), \quad (18)$$

where T_s is the sample time, i is the measure of the output current at instant k , and v is the estimation of the output voltage at time instant k , which is obtained as a function of the valid switching states of the converter.

C. Cost function definition

The cost function determines the tracking error that would be generated by each of the predictions with respect to the reference given for the next sample time $k+1$. The switching state which generates the least tracking error in the cost function is selected and applied during the sample time $k+1$. There are multiple ways to define tracking error. In this paper, the quadratic error will be used, as shown in the equation (19):

$$\begin{aligned} \Delta i(k+1) = & (i_u^*(k+1) - i_u(k+1))^2 + \\ & (i_v^*(k+1) - i_v(k+1))^2 + \\ & (i_w^*(k+1) - i_w(k+1))^2. \end{aligned} \quad (19)$$

Further, the cost function must guarantee that a positive voltage is applied in the dc-link. This condition could be added to the cost function, but this would greatly increase the calculations required. For that reason, it is preferable to select the state of the rectifier beforehand as follows: the rectifier has six valid switching states of which only three are positive at any given time; it is therefore possible to immediately eliminate those which are not. Then, the three positive switching states are compared, and the greatest of the three is selected. Thus, the switching state that generates the greatest voltage in the dc-link will be applied. With the maximum voltage in the dc-link guaranteed, the cost function g will only evaluate the tracking error of the output current. The cost function can therefore be expressed by the following equation:

$$g(k+1) = \Delta i(k+1). \quad (20)$$

V. SIMULATION RESULTS

In this section, the predictive current control method is validated using Matlab-Simulink and the parameters given in Appendix-Table V. Steady-state tests are carried out, and the dynamic behavior of the control strategy is studied. The current references are given as:

$$\begin{aligned} i_u^*(k+1) &= I_u \sin(2\pi f T_s), \\ i_v^*(k+1) &= I_v \sin(2\pi f T_s - 2\pi/3), \\ i_w^*(k+1) &= I_w \sin(2\pi f T_s + 2\pi/3), \end{aligned} \quad (21)$$

where I_u , I_v and I_w , correspond to the amplitudes of phase u , v and w , respectively and f is the output frequency.

In Fig. 5 is shown the behavior of the 4Leg-IMC while operating with balanced output current references given by $I_u = I_v = I_w = 6[A]$, and an output frequency of $f = 30[Hz]$. Fig. 5(a) shows the output currents i , output current references i^* , and the neutral current i_n . Good behavior of the output currents is observed as they track their respective references. As expected, since the reference currents are balanced, the neutral current is zero with only high order harmonics due to the commutations. As shown in Fig. 5(b), maximum dc-link voltage is obtained the entire time, independent of the load current conditions, and this voltage presents a waveform similar to a six-pulse rectification. Due to this condition, the source current i_s is given as depicted in Fig. 5(c). The ripple observed in these waveforms is produced by the resonance of the input filter due to the commutations, but this issue is beyond the scope of this paper.

Fig. 6(a) shows the behavior of the 4Leg-IMC operating with unbalanced output current references given as $I_u = 2[A]$, $I_v = 4[A]$, and $I_w = 6[A]$, respectively, with an output frequency of $f = 30[Hz]$. This is the typical application for three-phase four-wire systems, where the load demand varies during each phase. The controller handles each phase current independently and thus the load currents track to their references with low steady-state error. This proves that the predictive strategy can control each current independently. The neutral-current, which is the sum of the three-phase currents, flows through the fourth leg and presents a sinusoidal waveform because the unbalanced references are given with the same reference frequency.

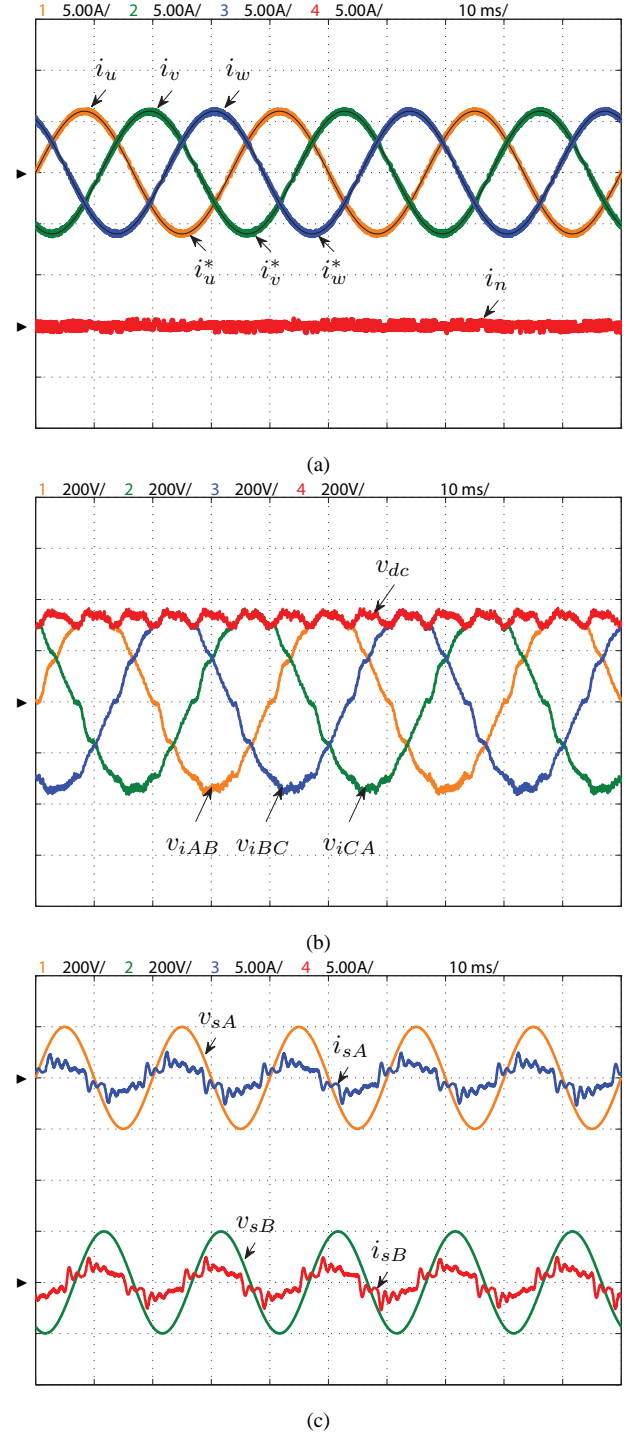


Figure 5. Simulation results with balanced references; (a) top: output current reference i_o^* and i_o , bottom: neutral current i_n . (b) line-to-line input voltages v_i and dc-link voltage v_{dc} . (c) top: source voltage v_{sA} and source current i_{sA} , bottom: source voltage v_{sB} and source current i_{sB} .

Fig. 6(b) shows the behavior of the 4Leg-IMC operating with unbalanced current references ($I_u = 4[A]$, $I_v = 6[A]$, and $I_w = 2[A]$) during a time window of 30[ms] and a frequency of $f = 60[Hz]$. Again, a very good tracking of the load current to its respective references with very low error and a fast dynamic response is observed. As expected, due to the unbalanced load current references, a neutral current i_n

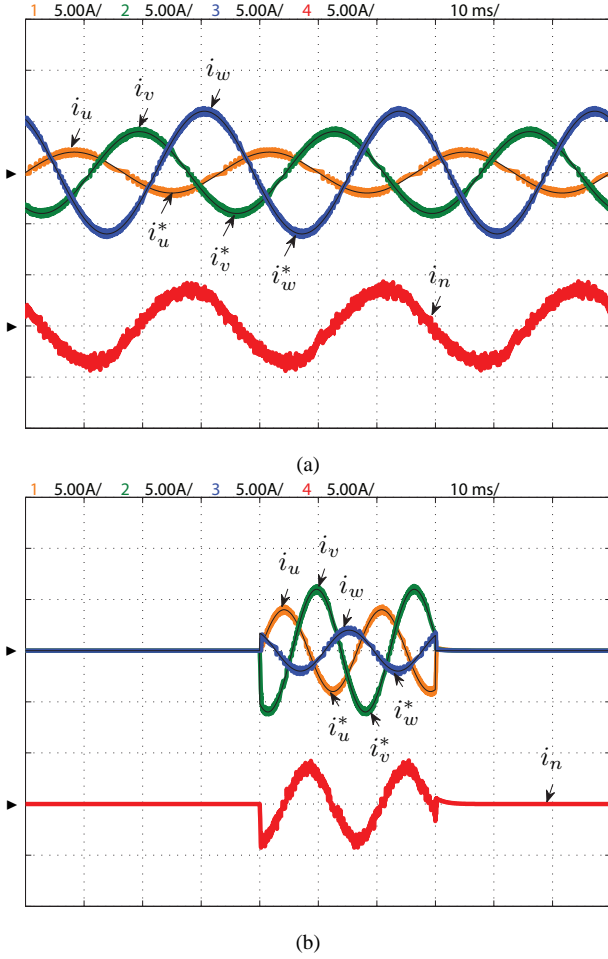


Figure 6. Simulation results with unbalanced references in steady state (top, $f = 30[\text{Hz}]$) and transient state (bottom, $f = 60[\text{Hz}]$): output current reference i_o^* , output current i_o and neutral current i_n .

circulates when the step from 0[A] to the different reference values is applied. The results showed fast dynamic response with no overshoot for any of the output currents.

VI. EXPERIMENTAL RESULTS

A. Description of the experimental setup

In order to validate and demonstrate the feasibility of the proposed current control method, an experimental prototype designed by University of Nottingham has been used. The converter was built with Semikron SKM75GB123D dual IGBT modules for the rectifier side and a Semikron SK35GD126ET module for the inverter side. The control algorithm has been implemented using a host PC running MATLAB-Simulink 2006a software with Real-Time Interface (RTI). The dSPACE DS1103 controller is used to handle the control processes such as load current prediction, load voltage estimation, and cost function minimization. The load currents are measured by LEM LAH 25-NP sensors. Feedback from the sensors is sent to the controller through the DS1103 I/O connector. The switching state to be applied in the converter is sent from the dSPACE after $t = 19[\mu\text{s}]$ initialized the interruption to a Nexys3 FPGA, which performs the zero dc-link commutation strategy (in $5[\mu\text{s}]$, where the dead-times has been defined as

400[ns]) in order to operate the converter safely. The converter requires a commutation sequence that allows a safe change of the rectifier switching state. This problem can be addressed by synchronizing the state changes in the rectifier with the application of a zero voltage space vector in the inverter stage. Under this condition, no current circulates through the dc-link and the rectifier state can be changed without the help of auxiliary commutation circuits [9], [10].

B. Delay compensation

A large number of calculations are required in the predictive algorithm, and this causes a considerable time delay in the actuation. This delay can deteriorate the performance of the system if is not considered in the design of the controller. A solution to compensate for this delay is to calculate the cost function at the end of the next sampling period, $g(k+2)$. Thus, the selected switching state can be applied at instant $k+1$, and therefore one sampling period is available for calculations. To accomplish this, the control scheme is experimentally implemented as follows:

- 1) Measurement of the load currents.
- 2) Application of the switching state (calculated in the previous interval).
- 3) Estimation of current values at time $k+1$, considering the applied switching state.
- 4) Prediction of the load current for the next sampling instant $k+2$ for all possible switching states.
- 5) Evaluation of the cost function for each prediction.
- 6) Selection of the switching state that minimizes the cost function.

C. Zero dc-link current commutation

As previously mentioned, FS-MPC selects the optimal switching state that minimizes the cost function g and applies it to the converter during the next period $k+1$. This optimal state is one of the n possible valid switching states of the converter of both the rectifier and inverter stages. In order to ensure a safe commutation of the switches it is necessary a synchronization of both stages. This is accomplished by considering a zero dc-link current commutation strategy which can be synthesized by applying either state 15 or 16 (Table III) of the inverter stage. In other words zero dc-link current is achieved when all the switches related to positive node P (S_{i1} , S_{i3} , S_{i5} , S_{i7}) are closed or when all the switches related to negative node N (S_{i4} , S_{i6} , S_{i2} , S_{i8}) are closed. With any of these two available switching states, the load current flows in a loop closed by the upper switches or by the lower switches of the inverter, allowing the rectifier commute safe without any extra suppressing circuit or complex strategy. As an example, in Fig. 7 is observed that the initial state of the rectifier correspond to state 6 in Table II and in the inverter stage is applied state 13 (Table III), Fig. 8(a). In order to generate zero dc-link current, state 15 is applied to the inverter as observed in Fig. 8(b). While this state is applied, zero dc-link current is circulating and thus the rectifier can applied now state 1 of Table II without overvoltages and any interruption of the current (Fig. 8(c)).

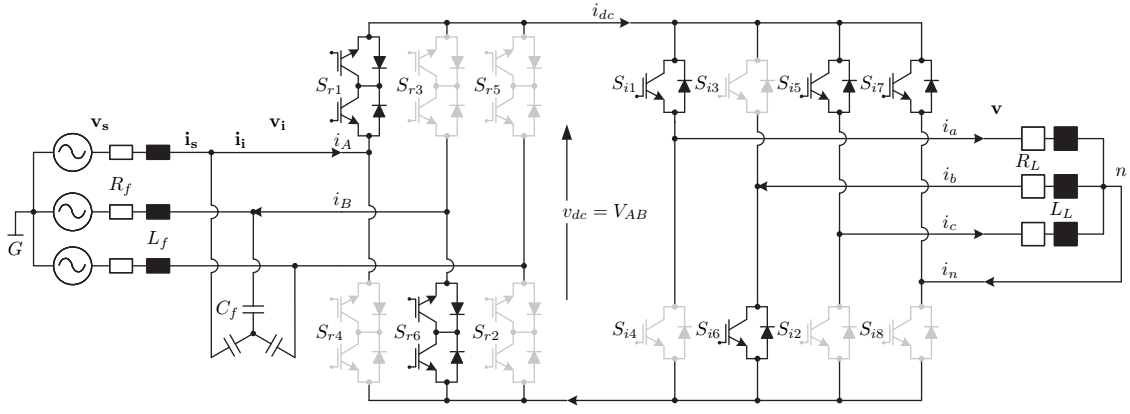


Figure 7. Initial state of the 4Leg-IMC.

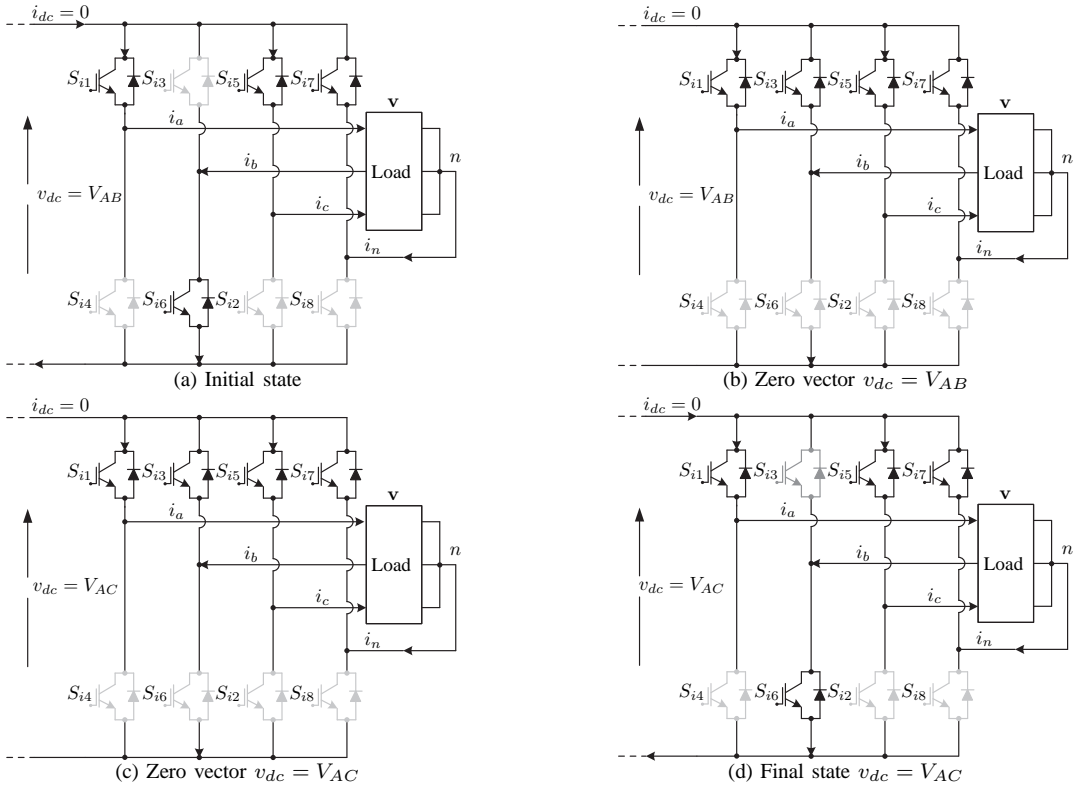


Figure 8. Zero dc-link current strategy.

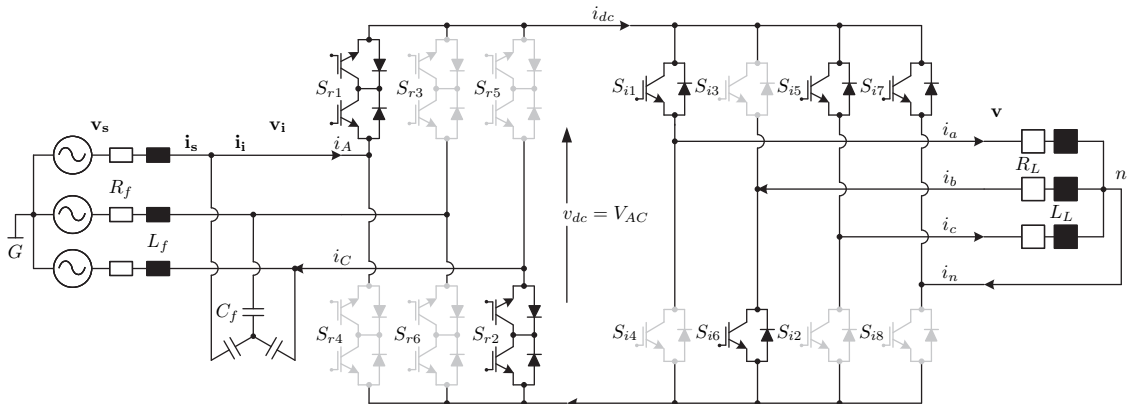


Figure 9. Final state of the 4Leg-IMC.

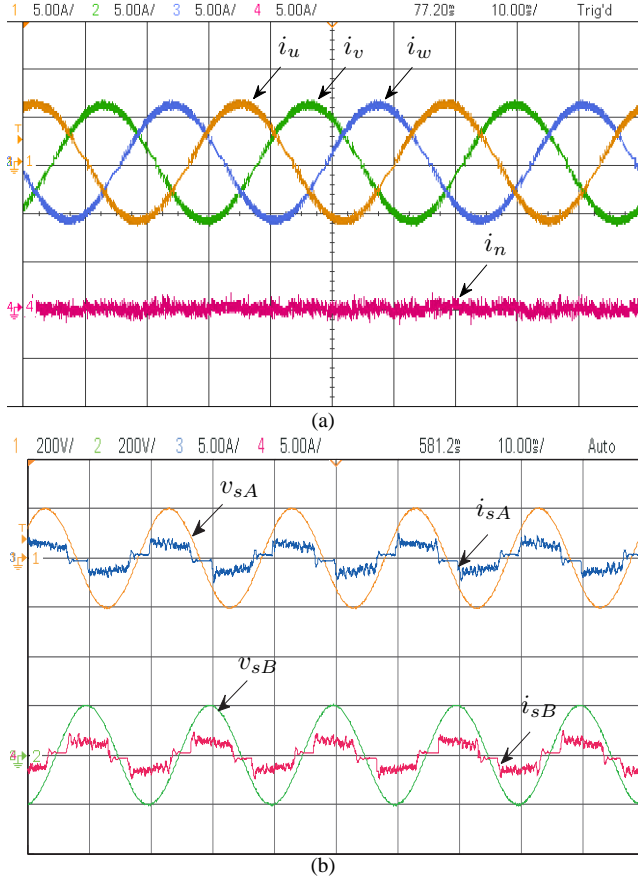


Figure 10. Experimental results with balanced references; (a) top: output current i , bottom: neutral current i_n (b) top: source voltage v_{sA} and source current i_{sA} , bottom: source voltage v_{sB} and source current i_{sB} .

After that, the inverter state can change to a new switching state or to keep the initial as depicted in Fig. 8(d).

D. Experimental results in steady and transient states

Fig. 10 and Fig. 11 show the behavior of the 4Leg-IMC operating with the same references considered in simulation section, where nearly the same behavior is observed in each case. Due to channel limitations of our oscilloscopes, it was not possible to measure the dc-link voltage. However, in Fig. 10 it is evident that the performance of the input current is almost the same as the simulation results when maximum dc-link voltage is applied. Fig. 11 shows the behavior of the 4Leg-IMC operating with unbalanced output current references. As previously mentioned, this operating condition is very important because this is the typical application for three-phase four-wire systems. The output current behaves well, with good tracking of its respective references, and it performs almost the same as in the simulation. Again, this experimentally demonstrates that the method can independently control each phase current.

In order to observe the dynamic behavior of the proposed method and compare it with the simulation results, Fig. 11(b) shows the behavior of the 4Leg-IMC operating with unbalanced current references. As expected, a good tracking to their references is observed and due to the unbalanced

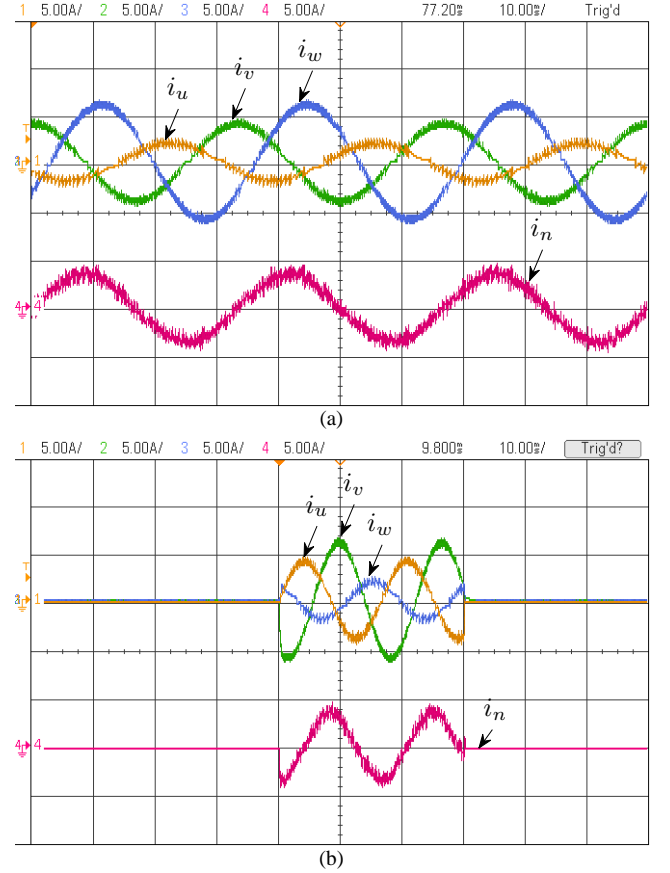


Figure 11. Experimental results with unbalanced references in steady state ((a), $f = 30[\text{Hz}]$) and transient state ((b), $f = 60[\text{Hz}]$): output current i , neutral current i_n .

load current references, a neutral current i_n is circulating in the time window. Fast dynamic response is obtained with no overshoot for all the output currents, obtaining almost the same waveforms as those exhibited in the simulation results.

In order to assess the performance of the proposed control scheme, the percentage mean absolute current reference tracking error $\%e_{i_{ix}}$ and THD percentage parameters, which have been defined in [47], are used. Table IV shows the performance analysis of the proposed control method at different points of operation, and it compares the simulations to the experimental results. In all cases, the error is below 3[%].

Note that compared to the simulations, this result is slightly higher in the experimental results. Case-2 presents the greatest errors, obtaining an average error of 2.68[%]. The calculation of THD is less than 6[%] in the experimental and simulation results, except in cases where unbalanced references are applied; there, the phases of smaller amplitude have greater THD. The cases with higher THD are those with a reference amplitude of 2[A], with the maximum in case-4. As expected the performance evaluation corroborates the good behavior of the proposed strategy in experimental and simulated implementations for a wide range of frequencies.

VII. DISCUSSION

Several control objectives, variables and constraints can be included in the cost function, allowing a simultaneous control

Table IV
SUMMARY OF STEADY-STATE ANALYSIS FOR SIMULATION AND EXPERIMENTAL RESULTS.

Case	Phase	Frequency [Hz]	Amplitude [A]	Simulation		Experimental	
				[%]THD	[%] $\bar{\epsilon}_i$	[%]THD	[%] $\bar{\epsilon}_i$
Case-1	<i>u</i>	30	6	4.4074	1.5979	5.4879	2.1443
	<i>v</i>		6	5.6831	1.6493	5.2848	2.2013
	<i>w</i>		6	5.6569	1.6551	5.4568	2.2257
	<i>avg</i>			5.2491	1.6341	5.4099	2.1907
Case-2	<i>u</i>	60	6	4.3790	1.6156	5.4168	2.7133
	<i>v</i>		6	5.6210	1.6434	5.3082	2.6312
	<i>w</i>		6	5.7396	1.7598	5.2876	2.6805
	<i>avg</i>			5.2465	1.6730	5.3375	2.6805
Case-3	<i>u</i>	30	2	13.6633	1.6101	16.6992	1.8828
	<i>v</i>		4	7.5341	1.6193	7.9202	1.9596
	<i>w</i>		6	5.4164	1.6179	5.4012	2.1257
	<i>avg</i>			8.8713	1.6158	10.0069	1.9894
Case-4	<i>u</i>	60	2	12.7347	1.5143	17.3034	2.0548
	<i>v</i>		4	7.6324	1.6263	7.6937	2.1270
	<i>w</i>		6	5.4099	1.6961	5.2254	2.5816
	<i>avg</i>			8.5923	1.6122	10.0742	2.2545
Case-5	<i>u</i>	30	6	3.1194	1.1392	5.3964	2.4126
	<i>v</i>		0	~0	~0	~0	~0
	<i>w</i>		4	5.5228	1.1437	7.8876	2.1858
	<i>avg</i>			2.8807	0.761	4.428	1.9876
Case-6	<i>u</i>	60	6	3.1301	1.2135	5.3724	1.9196
	<i>v</i>		0	~0	~0	~0	~0
	<i>w</i>		4	5.5360	1.1953	7.8014	1.8945
	<i>avg</i>			2.8887	0.8029	4.3912	1.0079

of all of them. However, when these control objectives are of a different nature, the combination of them in the cost function is not easy to implement and requires some weighting factors in order to prioritize between one control objective and another. This is still an open issue for research because there are no analytical or numerical procedures to adjust these parameters, they are determined using empirical methods. [26], [48] introduce different types of cost functions as well as procedures to select and adjust the optimal weighting factors depending on the application and type of cost function. An alternative implementation that does not requires weighting factors has been recently presented in [49].

One disadvantage when experimental implementations of FS-MPC are undertaken is the large computation requirement to evaluate the predictions related to each valid switching state of the converter. This computational demand increases for a converter (such as the 4Leg-IMC) with a large number of valid commutation states. Despite the new advances in more powerful and faster processors [31], this computation time introduces a considerable time delay which can deteriorate the performance of the system if not considered in the design of the controller. As reported in [26], [50], not only does the computation time introduce this delay but also this delay can appear due to the need for future values of the references in the cost function, specially if T_s is not sufficient small. As previously discussed, this issue has been taken into consideration by predicting the variables for $k = 2$ instead $k = 1$, because the real effect of apply the selected switching state is only reflected after the next sampling time. The main purpose of this paper has been to describe the experimental validation of a simple control strategy for the four-leg indirect matrix converter. As demonstrated by simulation and experimental results, this simple control strategy generates a very good load current

with almost sinusoidal waveform. The consequence of this technique is the square waveform of the input current, which is similar to a classical diode rectifier with large inductance at the load. In some applications, the users can operate with this low quality current as shown in [2], where the harmonics can be cancelled by an array of converters interconnected by a multi-winding transformer. As reported in [2], some applications that can be found are: wind turbine generator systems, external elevators, skin-pass mills, among others. The control of the input side implies a more complex prediction model and control algorithm, with an additional prediction model, more measurements and computation time, obtaining an improved behavior of the input current such as depicted in Fig. 12. As observed, by including a new term in the cost function, it is possible to obtain current in phase with its respective source voltage, but then new issues appear such as the resonance of the input filter (specially with uncertainties in the filter model, measurements errors and with a not optimized input filter) as well as the selection of adequate weighting factors in the cost function. This issue is not in the scope of this paper.

VIII. CONCLUSION

In this paper the experimental validation of a predictive current control strategy for a four-leg indirect matrix converter has been presented which represents a very attractive alternative for power electronics applications.

Simulation and experimental results have demonstrated that predictive control is very effective because it considers, in a very convenient way, the discrete nature of the converter switching states and the discrete nature of the microprocessor used to perform the control strategy. Our simulation and experimental results demonstrated a very good performance of the system in terms of percentage mean absolute current

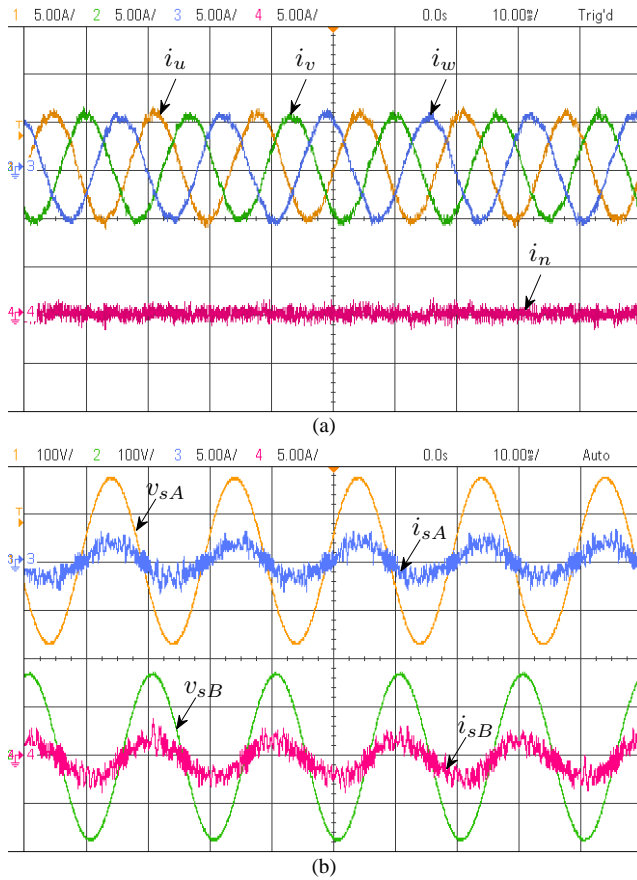


Figure 12. Experimental results with minimization of the instantaneous input reactive power; (a) $f = 60$ [Hz] top: output current i , bottom: neutral current i_n (b) top: source voltage v_{sA} and i_{sA} , bottom: source voltage v_{sB} and i_{sB} .

reference tracking error $\%e_{ix}$ and THD percentage parameters which have been shown to be acceptable for these applications. Future research considers the assessment with classical modulation and control techniques and other issues such as the study under uncertain in the parameters, and improvement of the input current behaviour.

APPENDIX

Simulation and experimental parameters are presented in Table V.

Table V
SIMULATION AND EXPERIMENTAL PARAMETERS

Variables	Description	Value
T_s	Sampling time	30 [μ s]
V_s	Supply phase voltage	200 [V_{ph}]
f_s	Supply frequency	50 [Hz]
L_f	Input filter inductance	3 [mH]
C_f	Input filter capacitance	15 [μ F]
R_f	Input filter resistance	1 [Ω]
R_L	Load resistance	10 [Ω]
L_L	Load inductance	15 [mH]

ACKNOWLEDGMENTS

The authors wish to thank the financial support from CONICYT Initiation into Research 11121492 Project, and the financial support of CONICYT/FONDAP/15110019. Furthermore,

the work of C. F. García was supported by CONICYT Scholarships for PhD studies in Chile and Programa de Iniciación a la Investigación Científica (PIIC) financed by Universidad Técnica Federico Santa María.

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