A Hybrid Inverter Solution for Medium Voltage Applications using Series Capacitor and a CSI Active Power Filter (SC-APF)

S Papadopoulos*, M Rashed, C Klumpner, P Wheeler

Department of Electrical and Electronics Engineering, University of Nottingham.
**eexsp19@nottingham.ac.uk*

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Abstract

This paper proposes a new hybrid inverter solution for medium/high voltage applications that consists of a slow switching inverter using high voltage or series connected switching devices, fitted with a low kVA rated auxiliary current source inverter to cancel the switching ripple produced by the main inverter. The reduction in CSI voltage stress is obtained by connecting it to the MV grid via a series capacitor which makes the solution suitable for retrofitting older inverters equipped with large passive filters. The paper describes the design procedure, the control scheme and validates the feasibility of the idea by including simulation results and evaluation of the waveform quality and also an estimation of the semiconductor losses.

1 Introduction

Conversion of DC into AC at medium and high voltage level has become a very important research topic now when the need to transfer very large amounts of power (GW) over long distances favour HVDC transmission systems. In the medium term, it is predicted that the distribution system will remain AC which requires the use of high voltage DC/AC inverters. Standard two level inverters built using series connected devices were the initially used in the first generation of forced commutated HVDC systems for their simplicity and the easiness to embed redundancy by adding additional devices in series; however, difficulties in achieving static and more importantly dynamic voltage sharing during switching meant that the harmonic performance of such inverters was poor, limited by the low switching frequency. In the last 5 years, forced commutated IGBTs with ratings of 6.5kV became commercially available which would reduce the number of series connected devices needed in a two-level inverter and therefore lower complexity and cost. However, the switching performance of a medium voltage (voltage rating >1.7kV) forced commutated device which for same kVA switched, results in higher switching loss, is also a limiting factor that will limit the switching frequency to approximately 1 kHz, which means power quality will remain a problem for a two-level medium/high voltage inverter implementation.

Multilevel voltage inverter topologies[1-4] such as cascaded H-bridge flying capacitor and diode clamped inverters, proposed more than 15 years ago, promised to solve the limitations of the series connected inverters but their application was limited in practice to a low (3) number of levels. The most important drawbacks were that the modulation and control became very complex and also that the building of the large stack on inverters required different connection paths for the clamping diodes or capacitors that resulted in large and uneven stray inductances. As a result these topologies have been found to be quite difficult to implement as a building block that would enable mass production of identical modules in custom designed system solutions. This is the reason why the Modular Multilevel Converter/Inverter (MMC) proposed few years ago [5] has gained increased popularity in a short period of time.

This paper proposes a solution aimed at improving the harmonic performance of a slow switching medium/high voltage inverter by means of employing an auxiliary inverter with very low installed power to cancel the switching harmonics caused by the main converter, being therefore a solution that can also be suitable for retrofitting older implementations. It relies on using a Current Source Inverter (CSI) which is known to be very good at synthesising a current reference, in this case the switching current ripple which is in the hundreds Hz range of the main MV inverter with the lowest switching frequency. A series capacitor to block most of the fundamental (50Hz) voltage is connected in series with the CSI to minimise its voltage ratings so standard/fast switches (ratings up to 1.2kV) could be used.

The hybrid concept proposed in this paper is similar to [6] where the auxiliary inverter cancels the switching ripple which is a small fraction of the main inverter current. In respect to the hybrid filter idea, [7] has demonstrated the implementation of a hybrid active filter consisting of a series LC filter controlled with an isolated inverter whilst [8] has demonstrated the idea of implementing a medium voltage active filter by using a low voltage 3-phase voltage source

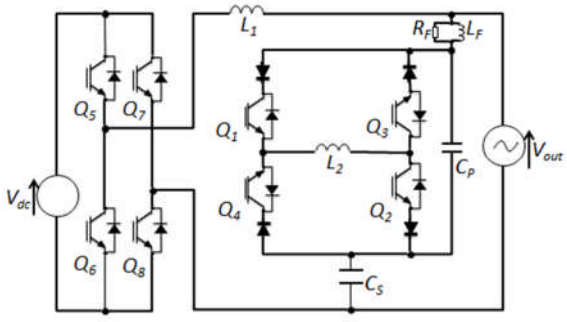

Figure 1: Proposed hybrid topology

Main Bridge	Auxiliary Bridge
2-level VSI	3 level-CSI
Medium Voltage	Low voltage
Low switching frequency	High switching frequency
IGBTs	RB-IGBTs or equivalent

Table I: System features

active power filter (APF) in series with a capacitor to minimise the 50Hz fundamental component voltage stress across the converter whilst also minimising the cost. The use of a series capacitor with a CSI has been investigated in [9-12] but for low voltage applications.

The novelty of this paper in relation to [2] is that it addresses medium/high voltage applications and that the installed power of the auxiliary inverter is further reduced by using a series connected capacitor to cancel most of the fundamental (50Hz) AC voltage (similar to[8]). By using a current source inverter (CSI) (as in [12]) the circuit does not need the current controllers a VSI would need in an active filter application, since the AC reference currents are synthetized directly, therefore, being able to switch slower for same current tracking performance.

Table I gives an overview of the system. The circuit topology, shown in fig. 1, is made up of a slow switching medium voltage VSI main bridge ($Q_{5\text{-}8}$) that interconnects with the MV grid via a line side inductance L1 that is designed to limit the switching current ripple while the Series Capacitor Active Power Filter (SC-APF) auxiliary bridge ($Q_{1\text{-}4}$) is a CSI connected in series with a capacitor (C_s) that is designed to block most of the 50Hz voltage. Capacitor C_p along with L_fR_f is the CSI second order low pass filter necessary to decouple the PWM output current of the SC-APF.

2 Design Procedure

The design procedure for this system has been separated into three main stages. The primary stage is the MV VSI design according to the grid requirements which will define the max switching frequency current ripple amplitude which will then dictate the current rating of the auxiliary bridge. The second stage is the design of the auxiliary CSI bridge and of the series capacitor which is dependent on the chosen maximum voltage rating as fraction of the supply voltage level. The final stage is the design of the parallel CSI filter capacitor which will then define the values of the CSI output filter. The circuit design stages are carried out at the relevant frequencies: the supply fundamental, the main bridge switching and the auxiliary bridge switching frequencies, by assuming the validity of the superposition principle.

$$\Delta I_{L_1} = \frac{V_{dc}}{2 f_{sw} L_1} \quad (1)$$

2.1 Main Bridge Design

The VSI inverter is designed assuming an open loop control at a low switching frequency. The frequency chosen has to be as low as possible to minimise switching losses however sufficiently high to avoid production of low order harmonics and interaction of the switching harmonics with the low order harmonic content typically existent in an AC supply. The size of the inductance L_1 is defined by the desired ripple amplitude at the switching frequency which, for a VSI that produces 2-level voltages will occur during the zero crossing of the grid voltage where the main inverter duty cycle is 0.5 (1)

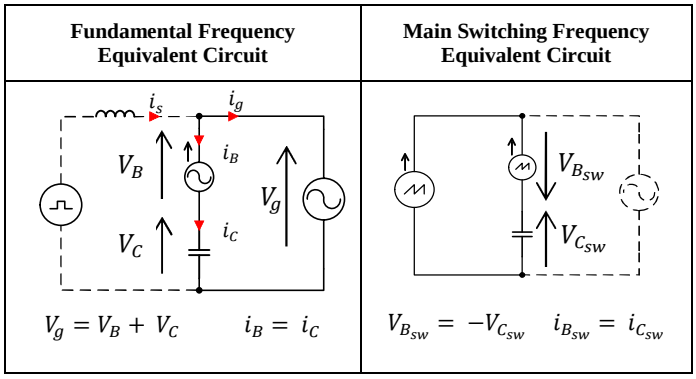

Figure 2: Simplified equivalent circuits at switching and fundamental frequency

2.2 Series Capacitor Design

The auxiliary bridge design is separated into the 50Hz and main bridge switching frequency design. The auxiliary CSI bridge is designed to operate at a high switching frequency to be able to cancel most of the switching harmonics.

Figure 2 depicts the equivalent circuit for each relevant frequency and the basic voltage equations. At the fundamental frequency, the sum of the auxiliary bridge and series capacitor voltages has to be equal to the grid voltage. The fundamental current processed by the APF will therefore define the voltage across the series capacitor and subsequently the fundamental voltage drop on the CSI bridge.

Limiting the fundamental maximum voltage drop on the bridge to a small percentage (K) of the grid voltage will create a circular voltage phasor trajectory and a corresponding circle for the current as shown in fig 3a. The circle can be separated into 3 operating regions out of which region 3 is undesirable as it will require the CSI to inject power into the circuit which is impossible and region 2 requires higher current for the same bridge voltage drop. Operation within region 1 will give the corresponding phasor diagram shown in fig 3b based on which the control system is derived.

Figure 3c shows the phasor diagrams for the two operating limits for maximum and minimum fundamental current component. In a lossless situation, the active current demand is zero therefore only the minimum reactive current is required given by (2) to sustain the required voltage drop. The series capacitance must be designed for maximum current at operating limit 2 where the fundamental current is at its

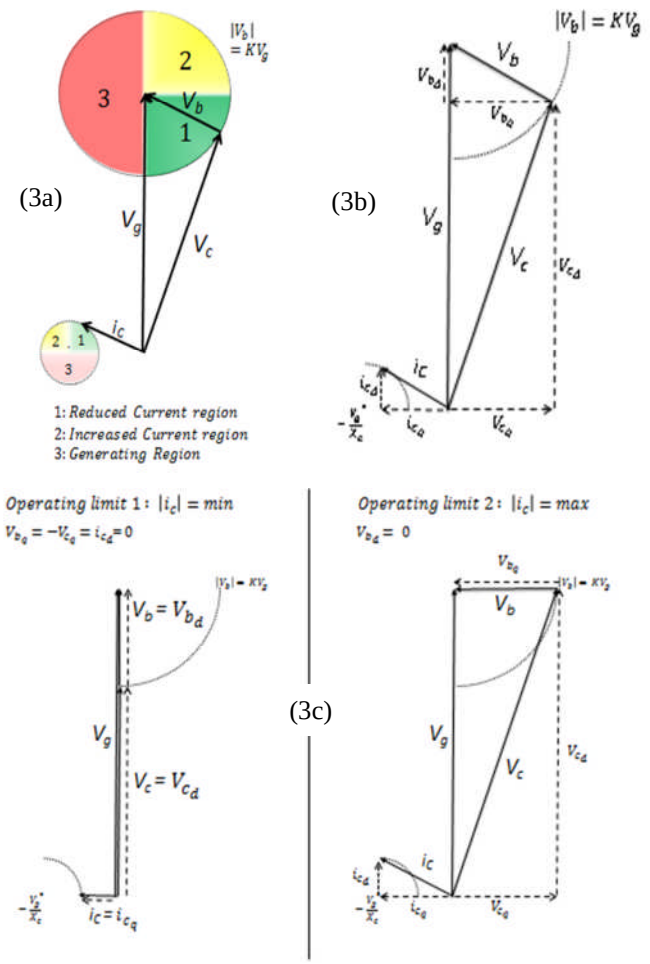

Figure 3a-c: Fundamental frequency phasor diagrams

$$\text{At operating limit 1: } |i_c| = i_{c_q} = \frac{(1-K)V_g}{X_c} \tag{2}$$

$$\text{At operating limit 2: } |i_c| = \frac{\sqrt{(K^2+1)}V_g}{X_c} \tag{3}$$

maximum given by (3) and the maximum active current component must be limited to the radius of the current circle given by (4). The active current component i_d relates to the DC link power while the total current that includes also the reactive current i_q goes towards controlling the capacitor voltage drop.

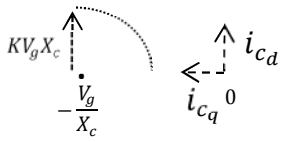

Figure 4: Current phasor diagram showing maximum i_d limit

$$|i_{c_d}| \leq \frac{KV_g}{X_c} \tag{4}$$

The size of the series capacitor will determine the placement and radius of the fundamental current circle. It is desired that the series capacitance is as small as possible to minimise the fundamental current demand. At the main switching frequency, the size of the CSI bridge voltage is equal to the capacitor voltage which is given by (5). The capacitance size is therefore a compromise between the SC-APF fundamental current demand and the switching voltage stress.

$$V_{b_{sw}} = |i_{sw}|X_c = \frac{|i_{sw}|}{\omega C_s} = -V_{c_{sw}} \tag{5}$$

$$C_{s_{min}} = \frac{|i_{sw}|}{\omega_{sw}|V_{c_{sw}}|} \tag{6}$$

$$C_{s_{max}} = \left(\frac{S}{P}\right)\frac{\widehat{i_s}}{\widehat{V_g}\omega} \tag{7}$$

The minimum capacitance is given by (6) for a given voltage switching voltage limit. Since the reactive current component is correlated with the voltage drop across the capacitor, (7) can be used to give the maximum capacitance for a given maximum reactive power produced by the APF. The design approach therefore guarantees that the voltage drop on the auxiliary bridge will never exceed the device rating whilst also limiting the maximum reactive power absorbed by the auxiliary bridge to utilise the voltage drop.

2.3 Output CSI Filter Design

Unlike [9] where Cp was calculated to be a potential divider, the capacitance is calculated based on defining the maximum leakage switching current to be absorbed by the capacitor. C_p is therefore chosen as a percentage of series capacitor C_s. The parallel capacitance C_p is required to be large enough to provide effective decoupling of CSI switching current ripple whilst only a small fraction of the cancelling main bridge switching current is bypassed. The ratio of fundamental current absorbed by the parallel capacitor is given by (8) based on operating limit 2 and should be negligible. Due to capacitor current bleeding the switching ripple reference must be compensated by a gain based on the capacitor ratio (10)

$$\frac{i_{c_s\,fund}}{i_{c_p\,fund}} = \frac{|V_{c_{max}}|C_s}{|V_{b_{max}}|C_p} \tag{8}$$

$$G = 1 + \frac{C_p}{C_s} \tag{10}$$

The inductance and damping resistor are subsequently calculated for a second order low pass filter with cut-off frequency below half the auxiliary CSI switching frequency and negligible phase shift at the main switching frequency.

3 Control System

The control scheme is shown in figure 5. The main switching frequency reference current component is compensated for by a gain G based on the ratio of capacitors Cs and Cp.

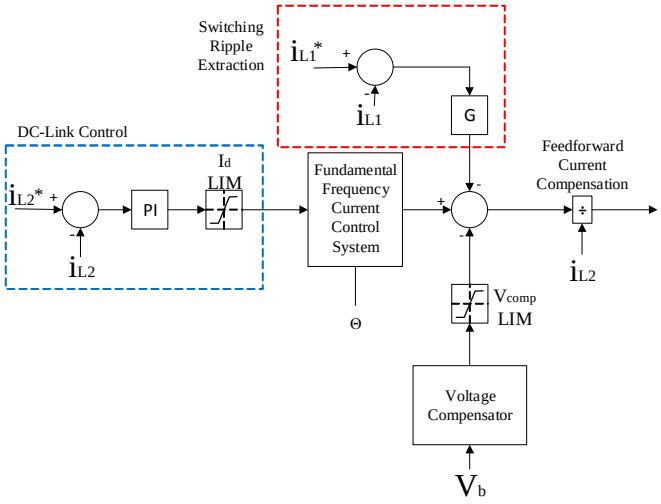

Figure 5: Auxiliary bridge control scheme overview

The fundamental frequency current is calculated based on the auxiliary inductor L_2 DC-link current demand (limited to (4)) using (10) and (11) shown below for a given desired voltage drop .

$$i_{c_d} = \frac{V_{b_q}}{X_c} = \frac{V_{c_q}}{X_c} \quad (10)$$

$$i_{c_q} = \frac{\sqrt{(KV_g)^2 - (i_{c_d}X_c)^2}}{X_c} \quad (11)$$

The control system has to be synchronised with the grid voltage angle θ to perform a dq-αβ transformation and accurately calculate the overall fundamental current demand.

A capacitor voltage compensator is required in order to avoid any DC voltage drift which could create instability and possible damage if the overall voltage exceeds the device ratings. To minimise the distortion caused on the AC side by the low frequency DC link inductor current ripple, a feed forward compensation block is used.

4 Estimation of Losses

A power loss model has been designed to estimate the losses for the circuit assuming the main inverter operates with a $2kV_{pk}$ medium voltage grid and using Infineon FF400R33KF2C 3.3kV/400A whilst the auxiliary CSI uses Semikron SEMiX202GB066HDs 600V/200A IGBTs. The maximum switching current ripple amplitude at 1 kHz has been chosen to be 20% of the fundamental peak to peak current.

f_{fund}	50Hz	L_1	10mH
$f_{sw\ main}$	1kHz	L_2	10mH
$f_{sw\ aux}$	50kHz	ΔI_{L1}	160A
V_g	2kV	Cs_{min}	35µF
I_g	320A	Cs_{max}	50µF

Table II: calculated values for simulated circuit

Cs	50µF
Cp	5µF
Lf	20µH
Rf	4Ω
Id_{limit}	π

Table III: calculated values for C=50µF

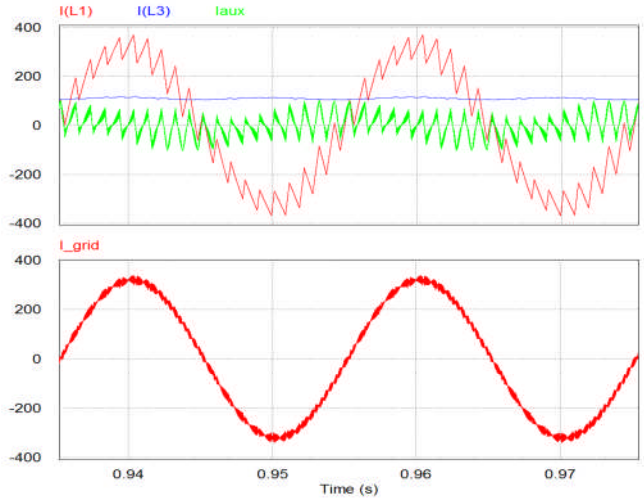

Figure 6: Main bridge current (red), SC-APF DC-link current(blue) and output current(green) and grid current (red)

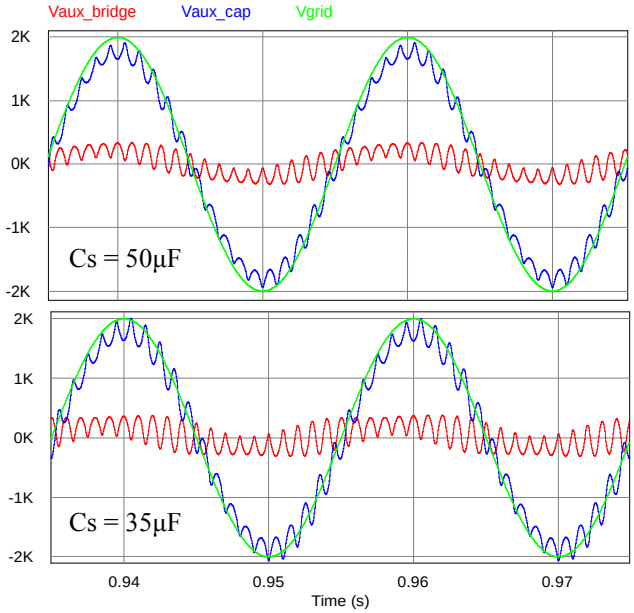

Figure 7: Grid voltage (green), Series capacitor voltage Vc (blue) and Auxiliary bridge voltage Vb(red)

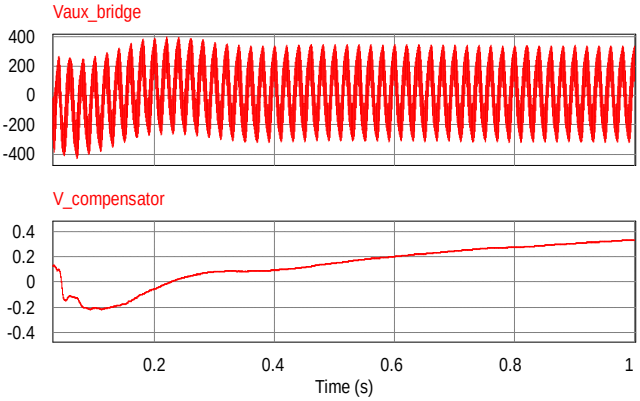

Figure 8: Auxiliary bridge voltage Vb(above) over 1 second along with voltage compensator output (below) during initial startup

The maximum fundamental voltage drop on the SC-APF has been set to 10% of the grid voltage (K=0.1) and the maximum reactive power to be absorbed at 10% of the active component of the main VSI resulting therefore in a power factor of 0.995. The simulation results are presented in this section using the two limits for series capacitance (35 and 50µF) according to the values in tables II and III.

Figure 6 shows the main and auxiliary bridge output currents, the DC-link current set at 110A and in the lower graph, the resultant clean output current revealing the effect of harmonic cancelation. Figure 7 shows the corresponding voltage drop on the SC-APF and series capacitor compared to the grid voltage. It can be observed that the fundamental voltage remains below 10% while the overall voltage that accounts also for the voltage drop produced by the main switching current passing through the series capacitor, remains below 20% of the grid voltage for both capacitor sizes. It can be observed that the switching harmonics cause a larger voltage drop for a smaller capacitor. Figure 8 reveals the auxiliary CSI bridge voltage over a longer period along with the voltage compensator output demonstrating that the voltage never exceeds the designed maximum value during the initial transient period. Figure 9 shows the series and parallel capacitor currents revealing that the decoupling of the CSI switching ripple current takes place in the parallel capacitor.
The harmonic content of the auxiliary and output currents are shown in figure 10 with a zoom in on figure 11 for a series capacitance of 50µF. It can be observed that all harmonics remain below 1% of the fundamental current showing compliancy with the grid standards whist most of them also remain under 0.1%. Due to the triangular shape of the current switching ripple the harmonics produced drop to negligible levels above 5kHz. The THD for current harmonics up to 6.5 kHz has been calculated at 0.7%. Table IV reveals an analysis of the three most significant harmonics for both capacitance sizes showing 97% harmonic cancellation at the main switching frequency (1 kHz) therefore proving the effectiveness of using the APF in cancelling the current ripple produced by the main converter.

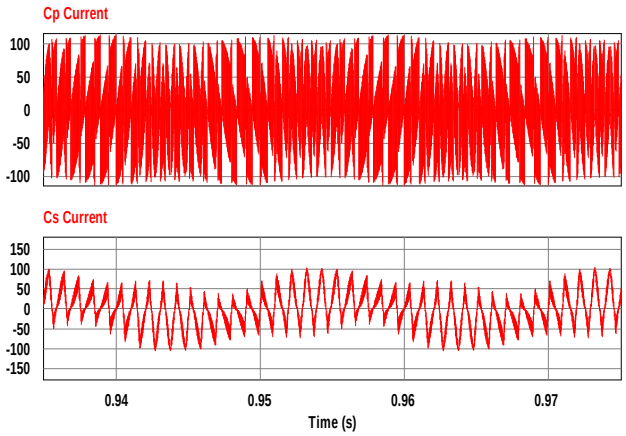

Figure 9: Series capacitor (bottom) and Parallel capacitor (top) currents

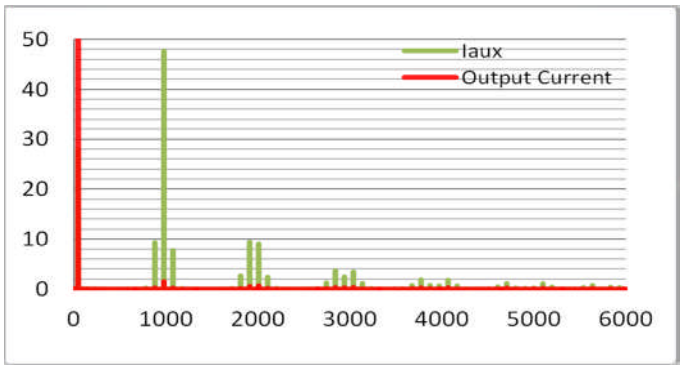

Figure 10: Auxiliary current harmonic content and output current harmonic content against frequency

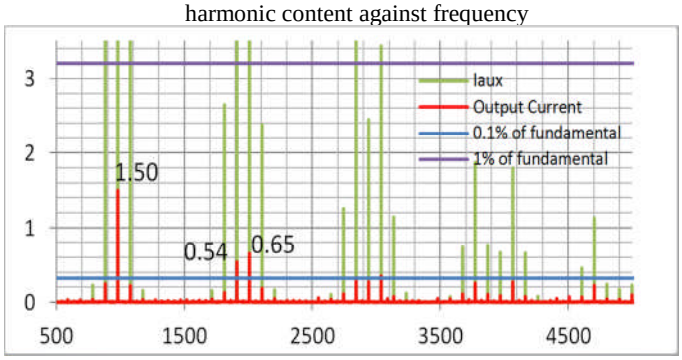

Figure 11: Closer look on largest current harmonics

	Cs = 50µF			Cs = 35µF		
Harmonic frequency /kHz	1	1.95	2.05	1	1.95	2.05
Amplitude /A	1.5	0.54	0.65	0.92	0.55	0.57
Percentage reduction /%	97	94	93	97	94	94
Percentage of fundamental amplitude /%	0.47	0.17	0.2	0.29	0.17	0.18

Table IV: Analysis of larger harmonics

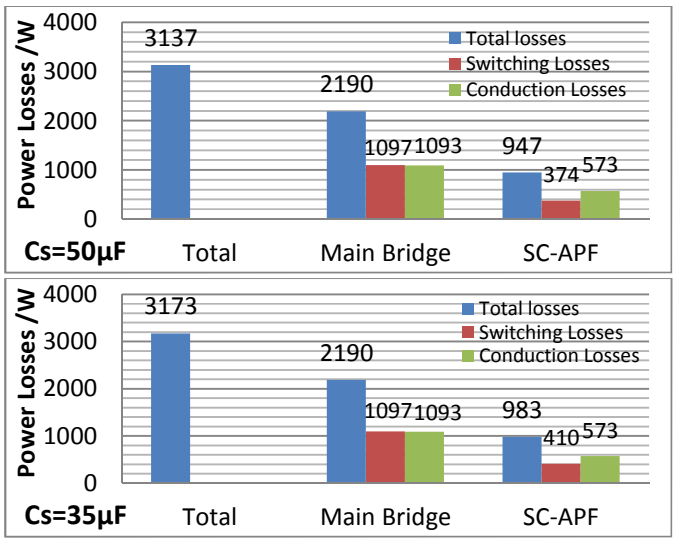

Figure 11: Power loss breakdown

The semiconductor power losses have been estimated at 0.9% as relative to power processed in both cases with the main bridge being by far the biggest contributor with 2.1kW of losses compared to less than 1kW for the auxiliary bridge. Looking at the installed power (no. of devices x peak voltage stress x peak current stress) in the auxiliary CSI devices, it can be concluded that it adds up only 6% to the installed

power in the main inverter and the reason is that the CSI is rated at a small fraction of the grid voltage (20% + margin) and is rated only for the main bridge current ripple that needs to be cancelled (20% + margin) by the use of a series capacitor and switching current harmonic elimination scheme whilst maintaining very high output current quality impossible to achieve with a passive filter approach. The reactive power requirement to maintain the voltage drop on the capacitor is limited to low levels and causes negligible phase shift on the output current. The use of a CSI auxiliary bridge requires a relatively simple control scheme without requiring additional control loops that would impose higher switching frequencies as is the case of using an auxiliary VSI. The existence of a triangular current ripple in the main bridge inductance which is characterised by a rapid decay of the amplitude of higher frequency harmonics compared to a square wave ripple, means that a lower bandwidth for the active filter is required therefore the THD of the resulting current remains at significantly low levels. The switching harmonics created by the auxiliary bridge at 50kHz have very low filtering requirements considering also that the power grid has typically inductive behaviour, thus establishing this solution as an effective harmonic mitigation scheme.

5 Conclusion

A novel hybrid inverter topology was proposed in this paper for high/medium voltage applications to achieve cancellation of the main slow-switching inverter current ripple by using a small size auxiliary inverter. The design procedure for the components in order to maintain low voltage and current stress on the auxiliary inverter is presented as well as its control strategy. Simulation results investigating the quality of the resulting grid current waveform shows cancelation of 97% of the 1kHz switching current harmonic that results in THD of the grid current of 0.7% whilst the added installed power in the auxiliary inverter accounts only for 6% of the main bridge inverter and the total losses of the hybrid system remain under 1% due to the possibility to reduce/optimise the switching losses/frequency of the main inverter. Due to the nature of the hybrid solution, this is suitable to retrofit older high voltage inverter installations which initially relied on large passive filters that are typically characterised by higher losses.

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