Active DC Voltage Balancing PWM Technique for High-Power Cascaded Multilevel Converters

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***Abstract*— In this paper a dedicated PWM technique specifically designed for single-phase (or four wire three-phase) multilevel Cascaded H-Bridge Converters is presented. The aim of the proposed technique is to minimize the DC-Link voltage unbalance, independently from the amplitude of the DC-Link voltage reference, and compensate the switching device voltage drops and on-state resistances. Such compensation can be used to achieve an increase in the waveform quality of the converter. This is particularly useful in high-power, low supply voltage applications where a low switching frequency is used. The DC-Link voltage balancing capability of the method removes the requirement for additional control loops to actively balance the DC-Link voltage on each H-Bridge, simplifying the control structure. The proposed modulation technique has been validated through the use of simulation and extensive experimental testing to confirm its effectiveness.**

***Index Terms*— Multilevel Converters; Predictive Control; Smart Grid.**

I. INTRODUCTION

IN recent years multilevel converters have been identified as a favored topology for high power applications as a result of advantages such as high levels of modularity, availability, overall efficiency, and high output waveform quality. This is achieved at the expense of increased numbers of components and control complexity [1]–[3]. In electrical traction drives multilevel inverters have been successfully applied in order to improve system reliability and reduce failures on motor windings as a result of the lower common mode voltages that they produce [4], [5]. The same advantages can be achieved when applied to Hybrid Electric Vehicles. In addition to this functionality, when the DC side is connected to a set of batteries or other energy storage devices the multilevel converter can be used to maintain the charge balance of the energy storage system [6], [7]. Multilevel converters have also been applied for power quality improvement and FACTS where, especially in aerospace applications, the reduced filtering requirement needed for multilevel converter represents an advantage in terms of total converter weight and cost [8]–[11]. In the coming years, multilevel converters are likely to be used increasingly in electrical power grids in order to achieve a higher flexibility and reliability and allow smart power management in the presence of different energy sources and utilities connected to the grid.

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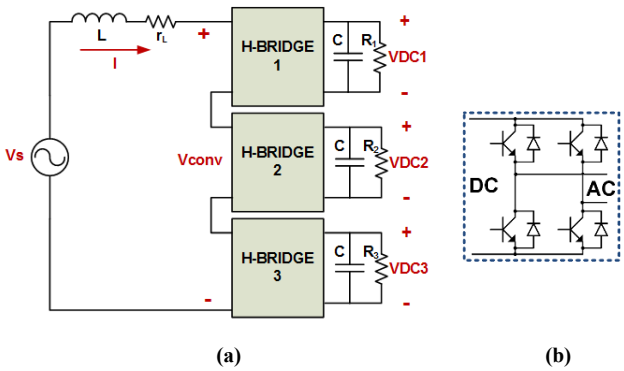
An example is the replacement of distribution level substation transformers with high power multilevel back-to-back converters. In all the aforementioned applications, multilevel converters are being increasingly considered as a fundamental technology, as a result of their capability to handle high-power, utilizing low voltage power devices, whilst maintaining superior quality output waveforms, even at low device switching frequency [12]–[17]. Amongst all the possible multilevel converter topologies [2], [18], [19], Cascaded H-Bridge converters (CHB) represent an interesting solution in several applications where its reduced number of components when compared to other multilevel converter topologies and high modularity are important features which lend themselves to the improvement of overall system efficiency and reliability [20]. Even though three-phase converters are widely used in high power applications [20], [21], a single-phase configuration is largely employed in Photovoltaic inverters [22], traction applications [5] or in neutral-connected three-phase power distribution systems [23]. The main issues with the CHB converter is the requirement for isolated DC-Link voltages as well as the significant effect of device voltage drop and on-state resistance in applications with high number of levels and relatively low application AC side voltages. Furthermore, in the active rectifier configuration, balanced DC-Link voltages are required to achieve optimal operation considering a symmetrical (and therefore fully modular) configuration. DC-Link voltage balancing methods have been proposed in literature for CHB active rectifiers and they can be divided into two main groups depending on whether the DC-Link voltage balancing method is integrated in the controller [8], [24]–[26], using additional control loops, or directly into the modulator [27]–[29]. In this paper the latter case is considered and a novel modulation technique, developed for single-phase systems and suitable for high power multilevel CHB converters, is introduced. The proposed modulation strategy is based on the Distributed Commutation Modulator (DCM), described in [30], [31]. DCM is a PWM technique specifically designed for multilevel CHB converters. The aim of DCM is to minimize the commutation frequency of the individual devices, distributing these commutations evenly amongst the converter HB cells. As a result, the converter losses are equally distributed across the devices, increasing the converter reliability, without compromising the output voltage waveform quality. However, the balancing of the DC-Link voltages represents an issue for the DCM strategy as such a technique is able to passively balance the DC-Link voltages only when balanced DC currents

are demanded. Moreover, in the DCM technique, the devices voltage drops and on-state resistances are not considered. In order to overcome these issues, an active DC-Link voltage balancing algorithm has been designed for DCM which accounts for the device voltage drops and on-state resistances, improving the output voltage waveform quality and maintaining good performances even when unbalanced DC currents are demanded. In [32] the concept of DC-Link voltage balancing algorithm is introduced as well as the device voltage drop and on-state resistance compensation. The main target of the proposed modulation strategy is, in contrast with DCM, to minimize the DC-Link voltage unbalance amongst the different converter cells in order to maintain the converter modularity and produce high quality waveforms, even if a low switching frequency is considered. Referring to Fig.1, the DC-Link voltage affects the distribution of the commutations amongst the devices only for unbalanced loads, i.e. when $R_1 \neq R_2 \neq R_3$. When the loads are balanced, i.e. when $R_1=R_2=R_3$, the device commutations are equally distributed amongst the CHB cells. When compared to other DC-Link voltage balancing techniques, the proposed algorithm presents a very fast and accurate response, avoiding the use of additional control loops. The device voltage drops and on-state resistances are also compensated, producing higher quality output voltage waveforms, in particular, in applications where a large number of CHB cells are used with a relatively low target AC side waveform magnitude, i.e. automotive applications [33]. The proposed modulator is implemented on a single-phase 7-level CHB, comprising three H-Bridges cells and described in section II, which is widely used in Photovoltaic inverters [34]–[36] or in neutral-connected three-phase power distribution systems [23]. Details of the proposed modulation technique are provided in section III, including examples of the operation of the proposed technique and a brief explanation of the DCM method. The obtained results are described in detail, highlighting the advantages and disadvantages of the proposed modulation technique. Simulation results are demonstrated for a single-phase 7-level converter in section IV, while experimental results from low voltage testing on a laboratory prototype are presented in section V.

II. Cascaded H-Bridge Converters

In Fig.1 the schematic diagram of a single-phase 7-level CHB converter, connected as an active rectifier, is shown.



(a) (b)

Fig. 1. Schematic diagram of a 7-level CHB in active rectifier configuration, (a) and a single HB circuit (b).

Although the proposed method is equally as effective in the inverter mode configuration, in order to test the capability of a DC-Link voltage balancing algorithm and avoid the necessity of isolated high voltage sources, the rectifier configuration is preferred. Referring to figure 1, the HBs are series-connected on the grid side and an inductive filter L, with a parasitic resistance r_L, is used to facilitate the required connection between the converter and the grid. Each HB cell is connected to a capacitor, C, and a resistor, R, used to represent the loading of the converter, which in reality could potentially be another converter, providing back-to-back operation, or a real load. For a symmetrical converter, the generic i-th cell is connected to a voltage source and can produce three voltage levels, indicated as - $VDCi$, 0 and + $VDCi$. These voltage levels are associated, respectively, to states -1, 0 and 1. As a consequence, an n-cell cascaded converter can produce $2n+1$ voltage levels on the AC side. The output voltage VCONV is composed of seven different voltage levels which can be produced by one or more combinations of H-Bridge states, as indicated in Table I.

TABLE I.
POSSIBLE VOLTAGE LEVELS OF A 3-CELL CONVERTER

V_{CONV}	*H-Bridges States*
$+3V_{DC}$	(111)
$+2V_{DC}$	(110) (101) (011)
$+V_{DC}$	(100) (010) (001) (11-1) (1-11) (-111)
0	(000) (10-1) (-101) (1-10) (-110) (01-1) (0-11)
$-V_{DC}$	(-100) (0-10) (00-1) (-1-11) (-11-1) (1-1-1)
$-2V_{DC}$	(-1-10) (-10-1) (0-1-1)
$-3V_{DC}$	(-1-1-1)

III. Proposed Modulation Technique

As stated in the introduction, the main goal of the proposed modulation method is to minimize DC-Link voltage imbalances and compensate the device voltage drops and on-state resistances. To achieve such a result, a fast response to any unbalance on the DC loads is required. For this reason the balancing algorithm is fully integrated into the modulation scheme, without using any additional controllers. It is important to note that since one of the targets of the proposed algorithm is to equalize the voltages on the capacitors, their average value is considered as the reference voltage for each DC-link capacitor in the algorithm, while the total DC-Link voltage is set to the reference value using a Proportional-Integral action external to the modulator. In order to reduce stress on the power switches and improve their reliability, the commutations are permitted only between adjacent voltage levels i.e. it is possible to switch only one leg of one H-Bridge cell during every sampling interval. The algorithm is modular and applicable to a generic n-level CHB converter; however increasing the number of voltage levels requires an obvious increase in computational effort.

A. Control Scheme

Fig. 2, shows the control block diagram implemented for the converter of Fig.1, where VDC denotes the total DC-Link voltage and VDC^* is the desired DC-Link voltage. A single-phase Phase-Locked-Loop (PLL) is used in the control scheme to obtain the supply phase angle, θ, and RMS value, $V_{s,RMS}$. The PLL scheme is obtained by cascading the orthogonal system

generator proposed in [37], based on the Second Order Generalized Integrator, with the three-phase PLL presented in [38], based on a steady-state linear Kalman filter.

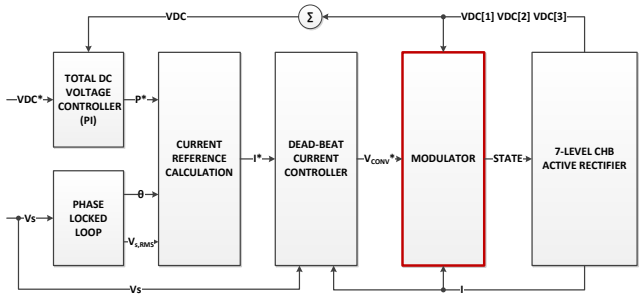


Fig. 2. Overall control scheme.

The line current is controlled in order to obtain the required DC-Link voltage; to achieve this goal, the current reference I^* is calculated, at every sampling period T_s of the controller, as follows [39]:

$$I^*(t_k + iT_s) = \frac{P^*}{V_{s,RMS}\sqrt{2}} sin(\theta + iT_s) \quad , \quad i = 1,2 \qquad (1)$$

where P^* is the required power, imposed by the voltage PI controller and t_k is the current time instant. The current reference I^* is predicted at two sampling instants, T_s and $2T_s$, in order to obtain a Dead-Beat current control law, described in [40]–[42] for various converter configurations, and in [23], [39] specifically for the proposed 7-Level CHB. The obtained control law is used to derive the desired voltage reference $V_{CONV}{}^*$ according to the following expression.

$$V_{CONV}{}^*(t_k + T_s) = V_s(t_k + T_s) - \frac{L}{2T_s}[I^*(t_k + 2T_s) - I(t_k)] + \\ + r_L I^*(t_k + T_s) \qquad (2)$$

The control output represents the desired converter voltage average value during the next sampling interval, applied using the proposed modulation scheme.

B. Distributed Commutation Modulator (DCM)

As mentioned in the introduction, the proposed technique can be seen as an improvement to the DCM technique [30], [31] where the commutations are distributed amongst the three H-Bridges in order to reduce the device switching frequency, and optimize the converter losses. Under normal operating conditions, the n converter cells are able to commutate sequentially so that each one can perform only one commutation every n sampling periods. Commutations are permitted only between adjacent voltage levels. As a consequence, the total switching frequency is half of the sampling frequency, while the device switching frequency of a single cell is approximately *1/(n-1)* for an *n*-level CHB. An example of normal operation is given in Fig. 4 where the 7-Level CHB of Fig. 1 is controlled in order to obtain a positive square waveform. As it is possible to see from the first waveform in Fig. 3, given a sampling frequency $f_s = 1/T_s$, the waveform produced by the 7 level CHB has a switching frequency $f_{sw} = f_s$. The H-Bridges are forced to commutate sequentially obtaining a switching frequency for a single H-Bridge of $f_{swHB} = f_{sw}/3$. Taking advantage of the zero vector redundancy, it is possible to obtain, for the device Q_1 of the H-Bridge 1, a switching frequency equal to $f_{sw}{}^{Q1} = f_{swHB}/2$. Clearly this operation condition is not always feasible when a multi-level waveform is produced and the modulation algorithm attempts to distribute the commutations amongst the devices. Two main issues have been identified using this technique. The DC-Link voltage balance is achieved with a symmetrical load on the three HBs and in any other case an additional control is required. The second issue appears in the case of high-power but relatively low voltage applications utilizing a large number of CHB cells, where the device voltage drops and on-state resistances can negatively affect the behavior of the modulator. An additional algorithm, described below, has been implemented to overcome these issues.

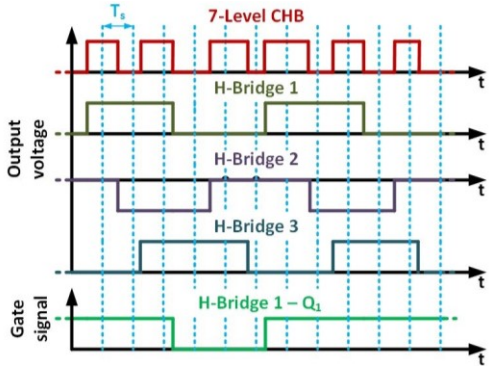


Fig. 3. DCM technique working principle.

C. Device voltage drop and on-state Resistance compensation

The device voltage drop and on-state resistance effect is compensated considering, instead of the measured DC-Link voltages, the effective voltages generated by the converter [43]. For each HB cell, three parasitic voltages, which are dependent on the current direction and amplitude, are defined as:

$$V_0 = sign(I) * (V_d + V_q) - I * (R_d + R_q) \qquad (3)$$

$$V_+ = -2 * (V_q + |I|R_q) \qquad (4)$$

$$V_- = 2 * (V_d + |I|R_d) \qquad (5)$$

In eqs. (3)-(5) the actual voltages generated by the converter are calculated on the basis of the diode and transistor voltage drops (V_d, V_q), the diode and transistor on state resistances (R_d, R_q), and on the current I flowing through the HB. In particular, when a zero voltage state is applied, the voltage VDC_{eff} produced at the output of the *i*-th cell is defined by the following equation:

$$VDCeff[i] = V_0 \qquad (6)$$

On the other hand, in case of positive power flowing through the HB cell (applied voltage and AC current have the same sign) the transistor are on and generate the voltage defined by the following equation:

$$VDCeff[i] = VDC[i] + V_+ \qquad (7)$$

Similarly, in case of negative power flow through the HB cell, the transistors are on and generate the voltage defined as follow:

$$VDCeff[i] = VDC[i] + V_- \qquad (8)$$

D. DC Link Voltage balancing algorithm

A simplified block diagram of the voltage balancing algorithm is presented in Fig. 4 for a 3-cell converter. The scheme is based on the application of iterative conditions in order to achieve the desired balance of the DC-Link voltages without losing the modularity of the algorithm.

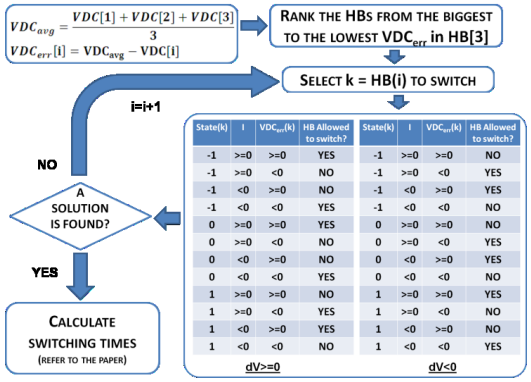


Fig. 4. DC voltage balancing basic principle.

The modulation algorithm begins with an update of the actual order of commutation of the 3 H-Bridges. From the measured DC-Link voltages on each capacitor, *VDC[1], VDC[2], VDC[3],* the average DC-Link voltage VDC_{avg} is calculated as in (9) and considered as a reference value.

$$VDC_{avg} = \frac{VDC[1] + VDC[2] + VDC[3]}{3} \quad (9)$$

Then, the DC-Link voltage error VDC_{err} is calculated for every HB from eq. (10).

$$VDC_{err}[i] = VDC_{avg} - VDC[i] \quad (10)$$

The switching order for the HBs is determined by the ranking, from the largest to the smallest, of the VDC_{err} absolute values. Supposing that *k*-th HB has been selected for the next switching, it is possible to calculate the normalized voltage error *dv* that has to be compensated by the selected HB as follows:

$$dv = \frac{V^* - \sum_{i \neq k} state(i) * VDCeff[i]}{VDCeff[k]} \quad , state(k) \neq 0 \quad (11)$$

$$dv = \frac{V^* + V_0 - \sum_{i \neq k} state(i) * VDCeff[i]}{VDC[k]} \quad , state(k) = 0 \quad (12)$$

where V^* is the voltage reference value and *state(i)* the current state of the generic *i*-th HB. In other words, *dv* corresponds to the normalized voltage that the selected *k*-th HB has to produce in the next sampling period on the basis of its current voltage level and the subsequent one. Under steady state operation usually $|dv|<1$; however it is possible, especially during fast transients of the voltage reference, that the absolute value of *dv* becomes larger than 1. Before performing any commutation, the modulator checks if the selected *k*-th HB is able to switch, considering its current state, and how the subsequent commutation will affect the DC-Link voltage balancing. The following three cases, valid for $dv>0$ and referred to the selected *k*-th HB state, are possible:

- ***state(k)=-1***: the selected HB is not able to generate the required positive voltage with only one commutation, thus the error is reduced applying the 0 voltage level for the whole sampling period. The commutation is permitted only if $VDC_{err}[k]$ and the AC current *I* have the same sign.
- ***state(k)=0***: the selected HB is able to generate the required positive voltage with only one commutation, thus the switching instant is calculated as in (13) or in (14), depending on the AC current sign.

$$t_x = T_m \left[1 - \left(dv - \frac{V_+}{VDC[k]}\right)\right] \quad , I \leq 0 \quad (13)$$

$$t_x = T_m \left[1 - \left(dv - \frac{V_-}{VDC[k]}\right)\right] \quad , I \geq 0 \quad (14)$$

If $dv>1$, it is clear from eq. (13) and (14) that $t_x<0$. In this case $t_x=0$ is imposed. The commutation is permitted only if $VDC_{err}[k]$ and the AC current *I* have the same sign.

- ***state(k)=1***: the selected HB is not able to not able to generate the required positive voltage. When $dv<1$, the voltage error is reduced by applying the 0 voltage level at the switching instant calculated by eq. (15).

$$t_x = T_m \left(dv - \frac{V_0}{VDC[k]}\right) \quad (15)$$

The commutation is permitted only if $VDC_{err}[k]$ and the AC current *I* have different signs.

- ***otherwise***: the modulator checks if another HB is able to switch to a higher voltage level without an increase the DC-Link voltage unbalance.

In Fig. 5 a switching pattern example for a positive error is described. As described in equations (3)-(8) the actual voltage applied by the converter is related to the current sign. Depending on the previously applied state, it is possible to determine three cases for the new commutation where the sign of the current determines the switching instant, as described in equations (13)-(15). Clearly such a commutation is allowed only if it does not increase the DC-Link voltage error as described in section II-D.

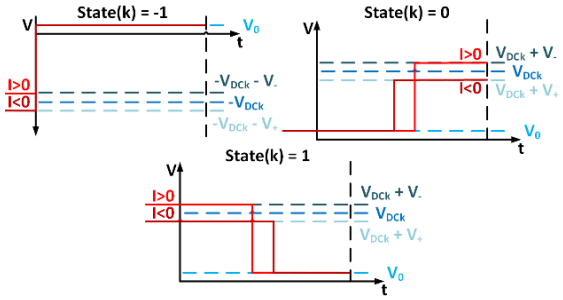


Fig. 5. Possible switching patterns for $0<dv<1$.

In case of $dv<0$, the following three cases for the selected *k*-th HB state are possible:

- ***state(k)=1***: the selected HB is not able to generate the required negative voltage with only one commutation, thus the error is reduced applying the 0 voltage level for the whole sampling period. The commutation is permitted only if $VDC_{err}[k]$ and the AC current *I* have different signs.
- ***state(k)=0***: the selected HB is able to generate the required negative voltage with only one commutation, thus the

switching instant is calculated as follows:

$$t_x = T_m\left[1+\left(dv-\frac{V_-}{VDC[k]}\right)\right] \quad , \; I \le 0 \quad (16)$$

$$t_x = T_m\left[1+\left(dv-\frac{V_+}{VDC[k]}\right)\right] \quad , \; I \ge 0 \quad (17)$$

If $dv<-1$, by considering eq. (16) and (17) it is clear that $t_x<0$. In this case $t_x=0$ is imposed. The commutation is permitted only if $VDC_{err}[k]$ and the AC current I have different signs.

- ***state(k)=-1***: the selected HB is not able to generate the required negative voltage. For the case where $dv>-1$, the voltage error is reduced applying the 0 voltage level at the switching instant calculated by eq. (18).

$$t_x = -T_m\left(dv-\frac{V_0}{VDC[k]}\right) \quad (18)$$

The commutation is permitted only if $VDC_{err}[k]$ and the AC current I have the same sign.

- ***otherwise***: the modulator checks if another HB is able to switch to a higher voltage level without an increase the DC-Link voltage unbalance.

IV. Simulation Results

Simulations have been carried out in order to compare the performance of the proposed modulation strategy. The power rating of the converter considered in simulation match the power rating used in the experimental tests (3kW). Operation in rectifier mode has been used to avoid the requirement of isolated high voltage sources. The proposed method, however, is equally as effective in the inverter mode configuration. A Dead-Beat current control, described in [23], [42], is used to impose the desired voltage reference. The complete control scheme is shown in Fig. 3 while the simulation parameters are shown in Table II. In order to highlight the effect of parasitic components, large values of V_d and V_q are considered during simulations. In this paper the proposed modulator is compared with the DCM technique illustrated in [31]. A comparison between the DCM technique and other well-known modulation techniques for CHB converters has already been carried out in [30]. In Fig. 7a and Fig. 7b it is possible to appreciate that the total DC-Link voltage is correctly regulated at the reference value with an optimal DC-Link voltage balance. However, with the proposed modulation strategy the DC-Link voltage oscillations are reduced, when compared to those observed with DCM.

TABLE II.
SIMULATION PARAMETERS

Symbol	Description	Value	Unit
V_d	Diode voltage drop	3	[V]
V_q	Transistor voltage drop	5	[V]
R_d	Diode on-state resistance	0.5	[mΩ]
R_q	Transistor on-state resistance	1	[mΩ]
r_L	Leakage resistance	1	[Ω]
L	Inductance	11	[mH]
C	Capacitance	3300	[μF]
R	Load resistance	20	[Ω]
f_s	Sampling frequency	2500	[Hz]

In Fig. 7c and Fig. 7d the line current and the grid voltage are shown for a switching frequency of 1.25 kHz. For the proposed technique the current is correctly regulated with the required phase alignment between grid voltage and current. The proposed modulation strategy also produces a lower THD value, compared with DCM, due to the active compensation of device voltage drops and on-state resistances which reduces the line current distortion. Fig. 7e and Fig. 7f illustrate, for both techniques, the converter output voltage versus the converter voltage reference and the voltages produced by the single HBs. The commutations are equally distributed amongst the HBs for both modulation strategies. In order to appreciate the superior capability of the DC-Link voltage balancing of the proposed modulation strategy, three unbalanced DC loads of 10Ω-20Ω-30Ω are implemented in the simulation. Such operating conditions frequently occur in solid state transformers [23] as well as in battery supplied inverters [36]. From Fig. 8a and Fig. 8b, which illustrate the DC-Link voltages, it is possible to observe that for the proposed modulation strategy the total DC-Link voltage is correctly regulated and the single DC-Link voltages are well balanced. When using the DCM technique under the same conditions, an unbalance of the DC-Link voltages is clearly evident. In Fig. 8c and Fig. 8d the line current and grid voltage are shown for a switching frequency of *1.25* kHz: using the proposed technique the current is correctly regulated with the required phase alignment between grid voltage and current. On the contrary, the DCM technique produces a significant distortion on the line current. The proposed modulation strategy clearly generates a lower THD value, compared with DCM. Fig. 8e and Fig. 8f illustrate, for both techniques, the converter output voltage versus the converter voltage reference as well as the voltages produced by the single HBs. Using the proposed strategy the commutations are not evenly distributed amongst the HBs anymore. Conversely, using the DCM technique, the even commutation distribution is maintained but the significant harmonic content affects the Dead-Beat controller, producing a distorted voltage reference.

V. EXPERIMENTAL RESULTS

The proposed modulator has been implemented and tested on a 3kW single phase 7-level CHB converter, shown in Fig.6, in the active rectifier configuration, as described in Fig. 1. A Spectrum Digital TI6711DSK board, interfaced to a custom FPGA board, is used to implement control and modulation schemes. The measurements of grid voltage, line current and DC-Link voltage (necessary for controller and modulation operation) are acquired using Hall Effect transducers.

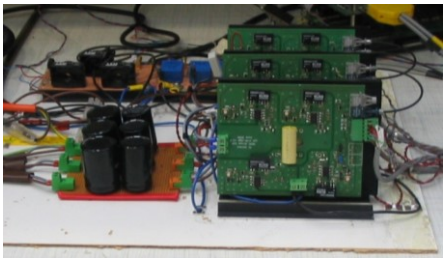


Fig. 6. Seven Level CHB converter used for experimental verification.

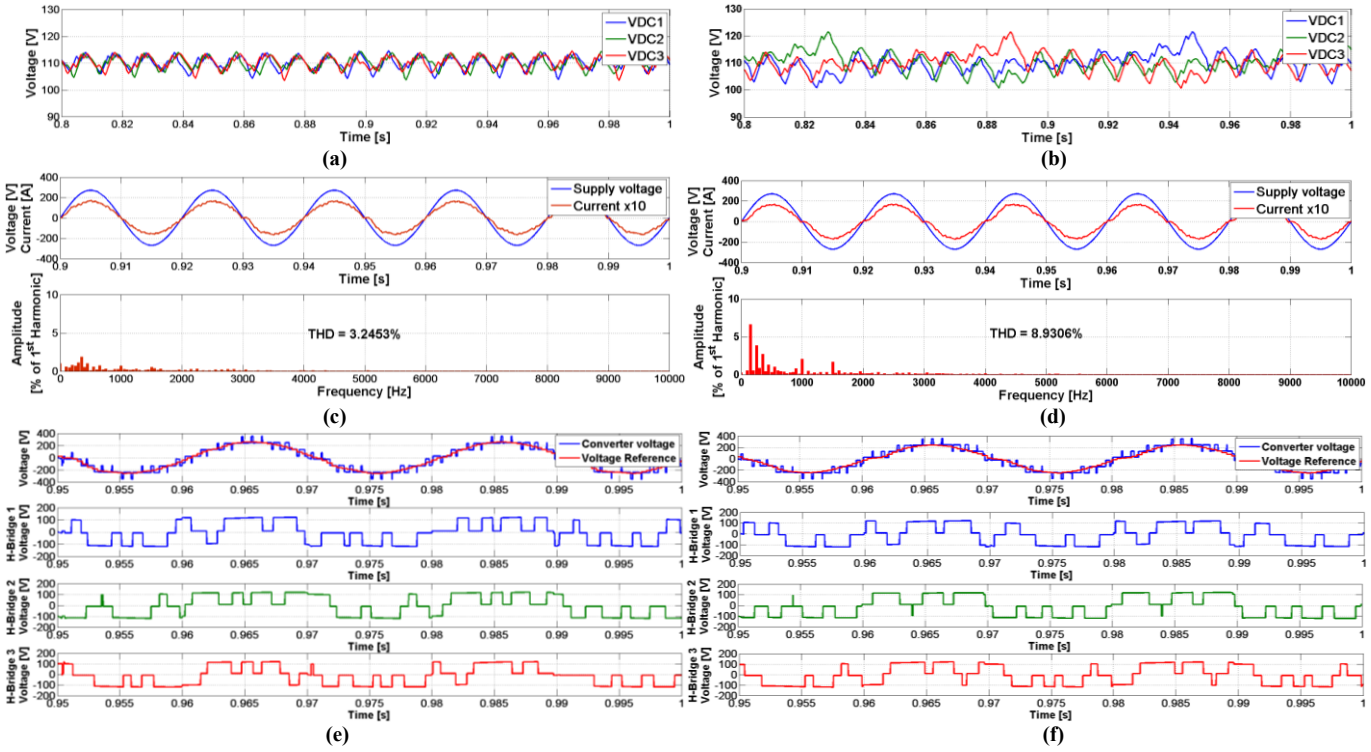


Fig. 7. Simulation results with DC Link voltage balancing algorithm, devices voltage drops and on-state resistances compensation (a), (c), (e) and DCM (b), (d), (f) for balanced DC loads: DC-Link voltages, AC current and voltages, converter voltage and reference, single H-Bridges voltages.

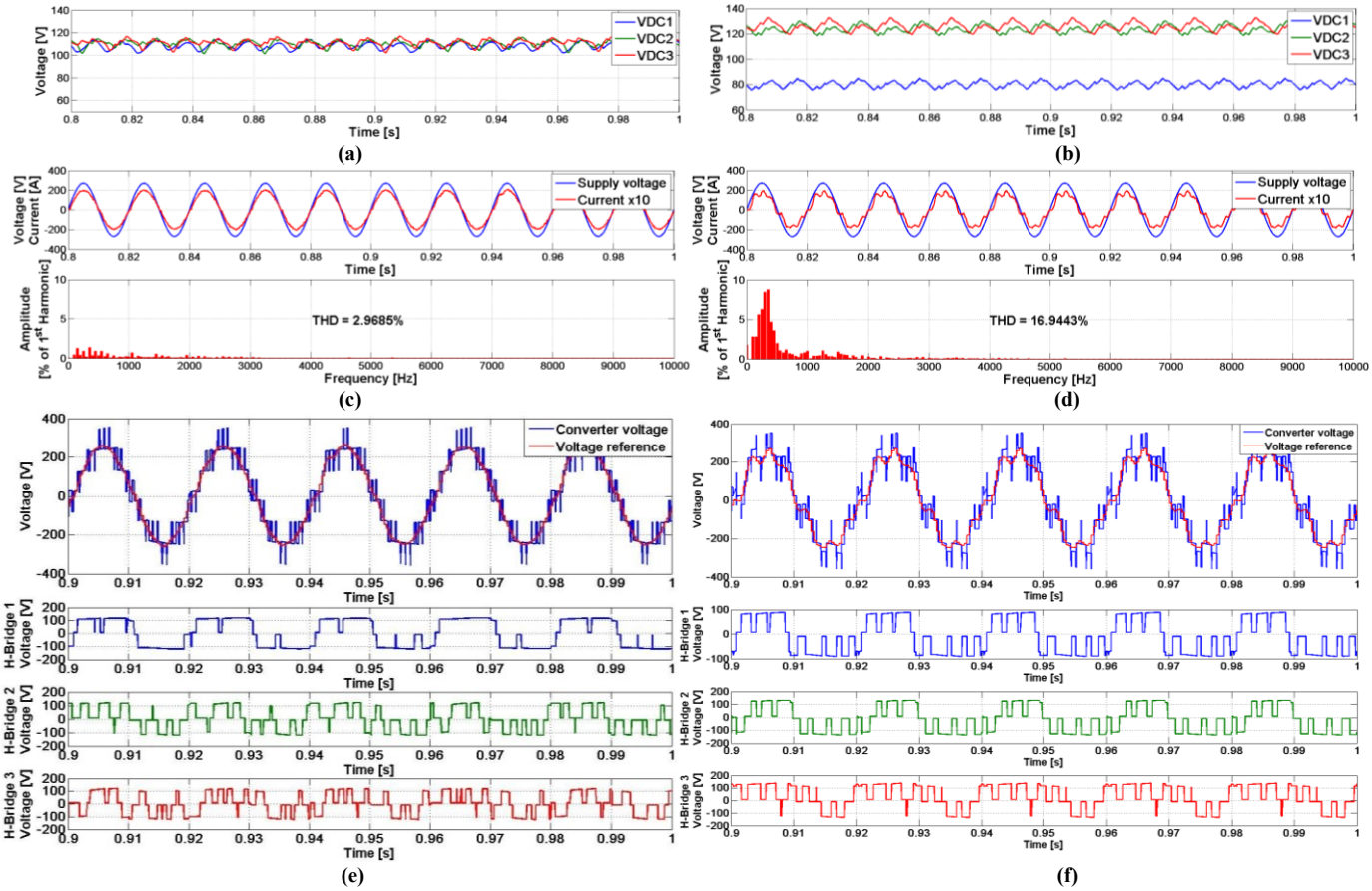


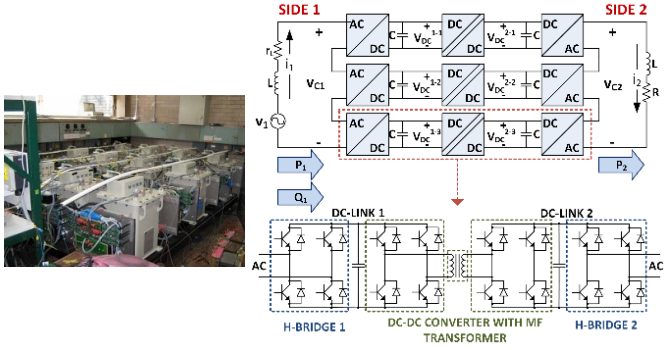
Fig. 8. Simulation results with DC Link voltage balancing algorithm, devices voltage drops and on-state resistances compensation (a), (c), (e) and DCM (b), (d), (f) for unbalanced DC loads: DC-Link voltages, AC current and voltages, converter voltage and reference, single H-Bridges voltages.

The experimental rig parameters are shown in Table III. Further experimental results have been obtained from a second converter with a similar configuration, shown in Fig. 9, denoted as UNIFLEX-PM converter [23], [44], [45].

TABLE III.
EXPERIMENTAL PARAMETERS FOR THE 3KW PROTOTYPE.

Symbol	Description	Value	Unit
V_d	Diode voltage drop	1.3	[V]
V_q	Transistor voltage drop	2.1	[V]
R_d	Diode on resistance	32	[mΩ]
R_q	Transistor on resistance	52	[mΩ]
r_L	Leakage resistance	0.51075	[Ω]
L	Inductance	11.15	[mH]
C	Capacitance	3300	[μF]
R	Load resistance	variable	[Ω]
f_s	Sampling frequency	2500	[Hz]

Each phase of the UNIFLEX-PM converter is composed of three fundamental cells, each one comprising four H-bridges and a medium frequency transformer. The control system for the converter has been implemented on a Texas Instruments TMS320C6713 DSP interfaced to five custom FPGA boards. Control of the DC/DC isolation modules, comprising two H-bridges and the MF transformer, is implemented entirely using the FPGA with the aim to equalize the DC-link voltages on the two sides of the converter [46].



(a) **(b)**

Fig. 9. UNIFLEX-PM converter: (a) Experimental rig, (b) Schematic diagram of one phase.

The tests have been performed using the parameters shown in Table IV [44], and a supply voltage of 190V rms. In this case the proposed control and modulation are implemented on side 1 while, on side 2, a Dead-Beat control with the DCM is implemented.

TABLE IV.
EXPERIMENTAL PARAMETERS FOR UNIFLEX-PM CONVERTER.

Symbol	Description	Value	Unit
V_d	Diode voltage drop	2.5	[V]
V_q	Transistor voltage drop	3.4	[V]
R_d	Diode on resistance	0.17	[mΩ]
R_q	Transistor on resistance	0.35	[mΩ]
r_L	Leakage resistance	0.3	[Ω]
L	Inductance	11	[mH]
C	Capacitance	3300	[μF]
R	Load resistance	30	[Ω]
f_s	Sampling frequency	2500	[Hz]

Four different experimental tests have been performed. The first one has been performed on the 3kW CHB considering three balanced DC loads of 60Ω. The results, shown in Fig. 10 for the 3kW CHB, allow the evaluation of the performance of the proposed modulator. It is clear that there is no phase-shift between converter current and supply voltage as required and the current harmonic content presents a low THD value, despite the harmonic content introduced by the supply voltage and the presence of error and noise on the measurement.

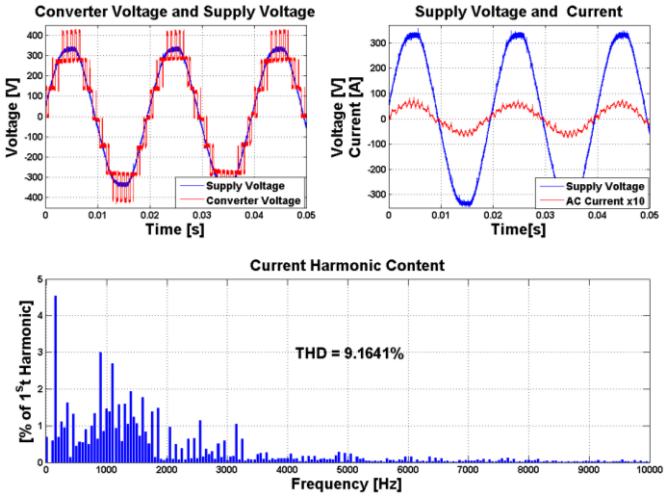


Fig. 10. Experimental results with the proposed technique for balanced DC loads on the 3kW prototype: Converter and Supply voltage, AC current and current harmonic content.

Clearly, there is no phase-shift between converter current and supply voltage as required and the current harmonic content presents a low THD value, despite the harmonic content introduced by the supply voltage and the presence of error and noise on the measurement. The second test and third test consider three variable DC loads from 63Ω-63Ω-64Ω to 51Ω-51Ω-52Ω and from 46Ω-46Ω-47Ω to 72Ω-72Ω-73Ω. The results, presented in Fig. 11 for the second test and in Fig. 12 for the third test, show the performance of the DC-Link voltage balancing algorithm. The DC-link voltage balance is consistently maintained and, after each step variation on the DC load, the control system recovers the desired total DC voltage value following the dynamic of the PI controller on the total DC-Link voltage. The total DC-Link voltage reference is calculated dynamically from the AC voltage rms value and presents some distortion that does not affect the control behavior. Moreover, the supply voltage and AC current are in phase as desired with reasonable current distortion considering the non-ideal supply voltage. The fourth test is performed on the UNIFLEX-PM converter using the proposed technique and the DCM technique. The results, presented in Fig. 14 for converter side 1 phase A, shows that even if a symmetrical converter is considered, the device parasitic parameters and unbalances in the power flow of the single Back-To-Back cells cause an unbalance in the DC-Link voltages that reflect on the generated converter voltage and line current using DCM. In particular the line current on phase A present a THD of more than 10%. On the other hand using the proposed technique the devices parasitic effects are compensated and the capacitor voltages are actively balanced results in a line current THD of 6.5%.

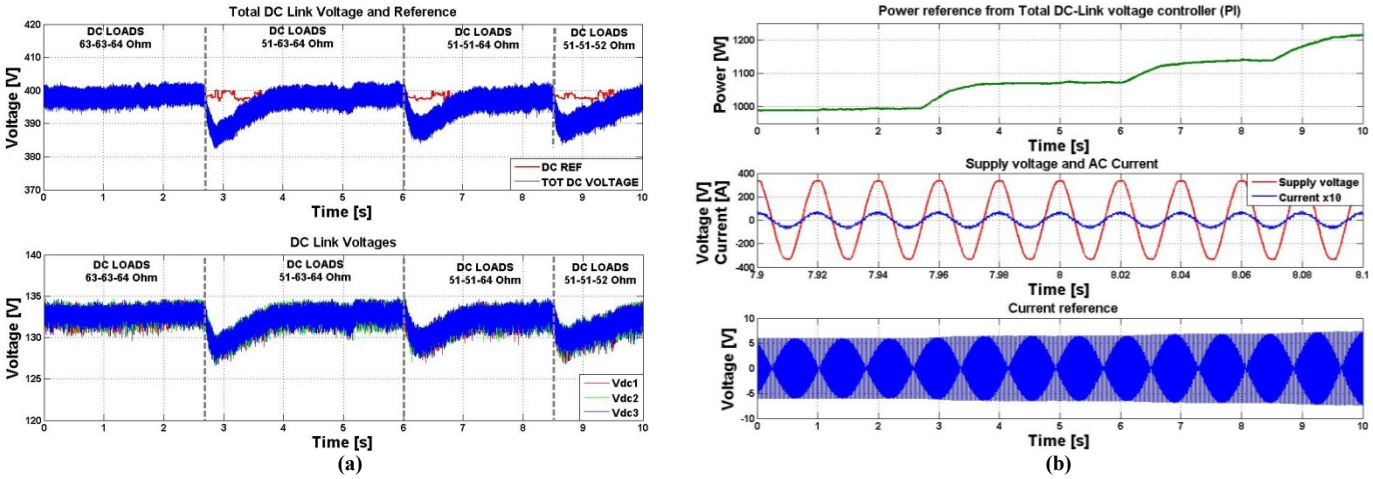


Fig. 11. Experimental results with DC Link voltage balancing algorithm and device voltage drop, ON resistance compensation for unbalanced DC loads: (a) Total DC-Link voltage and reference, Single DC-Link voltages (b) Power reference, supply voltage and current, current reference on the 3kW prototype.

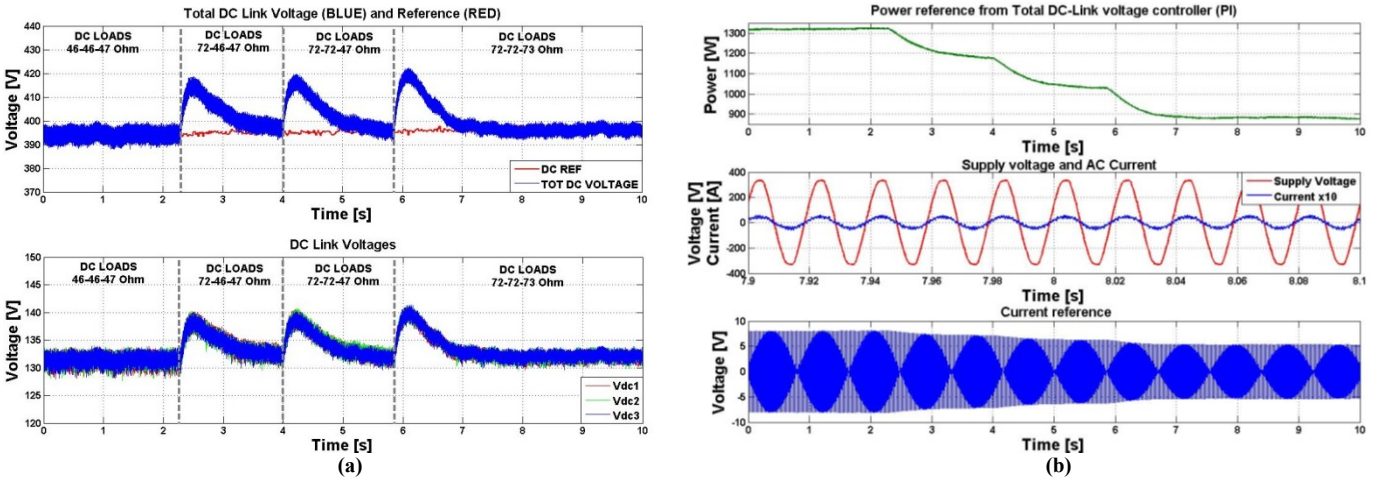


Fig. 12. Experimental results with DC Link voltage balancing algorithm and device voltage drop, ON resistance compensation for unbalanced DC loads: (a) Total DC-Link voltage and reference, Single DC-Link voltages (b) power reference, supply voltage and current, current reference on the 3kW prototype.

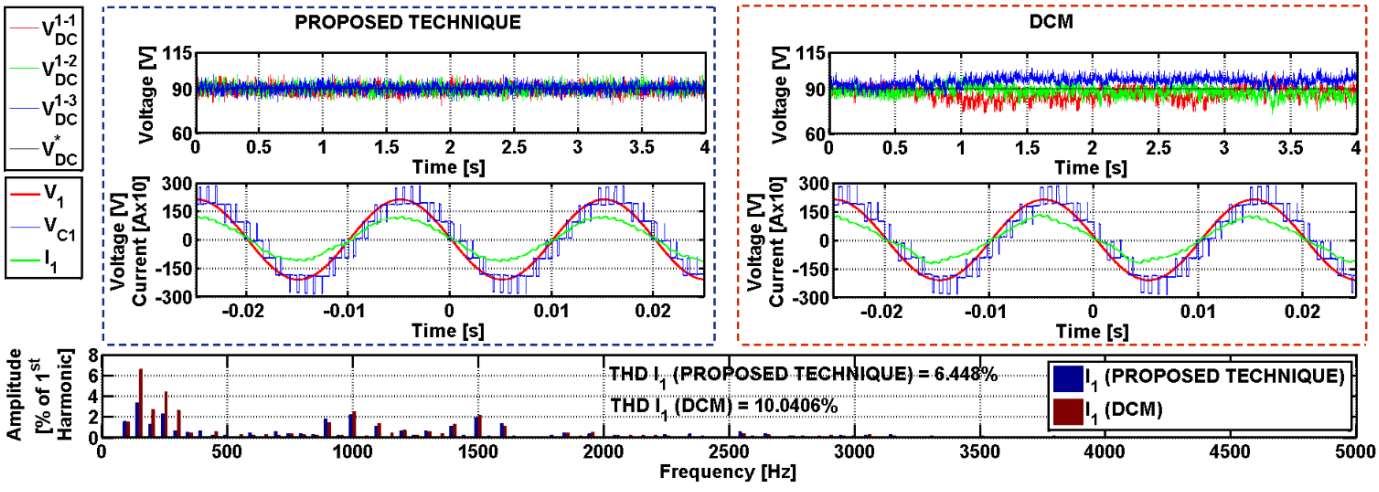


Fig. 13. Experimental results with DC Link voltage balancing algorithm and device voltage drop, ON resistance compensation on the UNIFLEX-PM prototype: single DC-Link voltages on phase A, supply voltage and current, converter voltage on phase A, line current harmonic spectrum.

VI. CONCLUSIONS

In this paper a new modulation concept, suitable for high power low switching frequency cascaded multilevel converters, is introduced. In order to minimize the switching frequency, only one leg of a single H-Bridge cell in each sampling interval is commutated, obtaining a total switching frequency that is the half of the sampling frequency. The aim of the presented modulation technique is to minimize the unbalance of the DC-link voltages, for any amplitude of the voltage reference, in order to obtain high quality waveforms whilst maintaining the modularity of the converter. In order to obtain a quick response to unbalance on the DC loads, the balancing algorithm is fully integrated into the modulation scheme without using any additional controllers. As a consequence, a high bandwidth response for the balancing algorithm is achieved even for extremely unbalanced load conditions. Moreover, device voltage drop and on-state resistance are compensated in order to extend the range of applications of the presented method to those cases where the parasitic effects of the devices may have a considerable effect, as for example automotive applications. The proposed algorithm is verified through simulation and experimental validation. The simulations show that compared to the DCM modulator [30], [31], the proposed modulation technique provides a balance of the DC-Link voltages without compromising the quality of the waveforms, in term of harmonic distortion, with both balanced and unbalanced DC loads. The modulator also naturally distributes the commutations amongst the H-Bridge cells in case of balanced DC loads. Experimental tests prove that it is possible to achieve the desired DC-Link voltage balancing even with a variation of 35% of the resistive DC loads. The proposed technique has been tested in comparison with DCM on CHB Back-To-Back converter showing that the proposed effect is not affected by the device parasitic parameters and converter asymmetries. In conclusion, using the proposed technique, it is possible to achieve an optimal balance of DC-link voltages and an active compensation for device parasitic effects in an n-level CHB active rectifier with any configuration of the DC loads, improving the quality of the AC waveforms and maintaining the modularity of the converter. However, clearly, increasing the number of voltage levels would clearly impact the required computational effort and a high-end DSP or micro-controller may be required.

REFERENCES

[1] L. G. Franquelo and J. Rodríguez, "The age of multilevel converters arrives," *IEEE Trans. Ind. Electron.*, no. June, pp. 28–39, 2008.

[2] J. S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, 1996.

[3] L. Harnefors and A. Antonopoulos, "Dynamic Analysis of Modular Multilevel Converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2526–2537, 2013.

[4] L. M. Tolbert and F. Z. Peng, "Multilevel Converters for Large Electric Drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, 1999.

[5] C. Cecati, A. Dell'Aquila, M. Liserre, and V. G. Monopoli, "A passivity-based multilevel active rectifier with adaptive compensation for traction applications," *IEEE Trans. Ind. Appl.*, vol. 39, no. 5, pp. 1404–1413, 2003.

[6] K.-M. Yoo, K.-D. Kim, and J.-Y. Lee, "Single- and Three-Phase PHEV Onboard Battery Charger Using Small Link Capacitor," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3136–3144, 2013.

[7] L. M. Tolbert, F. Z. Peng, T. Cunnyngham, and J. N. Chiasson, "Charge Balance Control Schemes for Cascade Multilevel Converter in Hybrid Electric Vehicles," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1058–1064, 2002.

[8] Z. Chen, Y. Luo, and M. Chen, "Control and performance of a cascaded shunt active power filter for aircraft electric power system," *IEEE Trans. Ind. Electron.*, vol. 59, no. 9, pp. 3614–3623, 2012.

[9] M. Odavic, V. Biagini, M. Sumner, P. Zanchetta, and M. Degano, "Low Carrier – Fundamental Frequency Ratio PWM for Multilevel Active Shunt Power Filters for Aerospace Applications," *IEEE Trans. Ind. Appl.*, vol. 49, no. 1, pp. 159–167, 2013.

[10] A. A. Valdez-Fernández, P. R. Martínez-Rodríguez, G. Escobar, C. A. Limones-Pozos, and J. M. Sosa, "A Model-Based Controller for the Cascade H-Bridge Multilevel Converter Used as a Shunt Active Filter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 5019–5028, 2013.

[11] A. Varschavsky, J. W. Dixon, M. Rotella, and L. Morán, "Cascaded Nine-Level Inverter for Hybrid-Series Active Power Filter , Using Industrial Controller," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2761–2767, 2010.

[12] P. R. Khatri, V. S. Jape, N. M. Lokhande, and B. S. Motling, "Improving power quality by distributed generation," *International Power Engineering Conference (IPEC)*, vol. 2, pp. 675–678, 2005.

[13] J. M. Guerrero, P. C. Loh, T. Lee, and M. Chandorkar, "Advanced Control Architectures for Intelligent Microgrids — Part II : Power Quality, Energy," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1263–1270, 2013.

[14] J. M. Guerrero, P. C. Loh, T. Lee, and M. Chandorkar, "Advanced Control Architectures for Intelligent Microgrids — Part I *: Decentralized and Hierarchical Control," IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1254–1262, 2013.

[15] R. Majumder, "Reactive Power Compensation in Single-Phase Operation of Microgrid," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1403–1416, Apr. 2013.

[16] R. M. Kamel, A. Chaouachi, and K. Nagasaka, "Three Control Strategies to Improve the Microgrid Transient Dynamic Response During Isolated Mode: A Comparative Study," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1314–1322, Apr. 2013.

[17] T. L. Vandoorn, J. D. M. De Kooning, B. Meersman, and J. M. Guerrero, "Voltage-Based Control of a Smart Transformer in a Microgrid," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1291–1305, 2013.

[18] J. Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, 2002.

[19] J. Ebrahimi, "A new multilevel converter topology with reduced number of power electronic components," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 655–667, 2012.

[20] M. Malinowski, K. Gopakumar, J. Rodríguez, and M. A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, 2010.

[21] D. E. Soto-Sanchez, R. Peña, R. Cárdenas, J. C. Clare, and P. W. Wheeler, "A Cascade Multilevel Frequency Changing Converter for High-Power Applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2118–2130, 2013.

[22] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep. 2005.

[23] S. Bifaretti, P. Zanchetta, A. J. Watson, L. Tarisciotti, and J. C. Clare, "Advanced power electronic conversion and control system for universal and flexible power management," *IEEE Trans. Smart Grid*, vol. 2, no. 2, pp. 231–243, 2011.

[24] H. Iman-Eini, J.-L. Schanen, S. Farhangi, and J. Roudet, "A Modular Strategy for Control and Voltage Balancing of Cascaded H-Bridge Rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2428–2442, Sep. 2008.

[25] M. Khazraei and H. Sepahvand, "Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 769–778, 2012.

[26] N. A. Rahim, M. Fathi, M. Elias, and W. P. Hew, "Transistor-Clamped H-Bridge Based Cascaded Multilevel Inverter With New Method of Capacitor Voltage Balancing," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 2943–2956, 2013.

[27] A. J. Watson, P. W. Wheeler, and J. C. Clare, "A Complete Harmonic Elimination Approach to DC Link Voltage Balancing for a Cascaded

Multilevel Rectifier," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2946–2953, Dec. 2007.
[28] J. I. Leon and S. Vazquez, "Unidimensional modulation technique for cascaded multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 2981–2986, Aug. 2009.
[29] Z. Shu, N. Ding, J. Chen, H. Zhu, and X. He, "Multilevel SVPWM With DC-Link Capacitor Voltage Balancing Control for Diode-Clamped Multilevel Converter Based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1884–1896, May 2013.
[30] S. Bifaretti, L. Tarisciotti, A. J. Watson, P. Zanchetta, A. Bellini, and J. C. Clare, "Distributed commutations pulse-width modulation technique for high-power AC/DC multi-level converters," *IET Power Electronics*, vol. 5, no. 6, pp. 909–919, 2012.
[31] S. Bifaretti, P. Zanchetta, A. J. Watson, L. Tarisciotti, A. Bellini, and J. C. Clare, "A modulation technique for high power AC/DC multilevel converters for power system integration," *IEEE Energy Conversion Congress and Exposition (ECCE),* pp. 3697–3704, 2010.
[32] L. Tarisciotti, A. J. Watson, P. Zanchetta, J. C. Clare, P. W. Wheeler, and S. Bifaretti, "A Novel Pulse Width Modulation technique with active DC voltage balancing and device voltage falls compensation for High-Power Cascaded multilevel active rectifiers," *IEEE Energy Conversion Congress and Exposition (ECCE),* pp. 2229–2236, Sep. 2012.
[33] F. Khoucha and S. Lagoun, "Hybrid cascaded H-bridge multilevel-inverter induction-motor-drive direct torque control for automotive applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 892–899, 2010.
[34] G. Buticchi, E. Lorenzani, and G. Franceschini, "A Five-Level Single-Phase Grid-Connected Converter for Renewable Distributed Systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 3, pp. 906–918, 2012.
[35] J. Chavarría, D. Biel, F. Guinjoan, C. Meza, and J. J. Negroni, "Energy-Balance Control of PV Cascaded Multilevel Grid-Connected Inverters Under Level-Shifted and Phase-Shifted PWMs," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 98–111, 2013.
[36] C. Yang and L. Chen, "A Single Phase Multilevel Inverter with Battery-Balancing," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1972–1978, 2013.
[37] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator," *IEEE Power Electronics Specialists Conference (PESC),* 2006, pp. 1–6.
[38] A. Bellini and S. Bifaretti, "Performances of a PLL based digital filter for double-conversion UPS," *International Power Electronics and Motion Control Conference (EPE/PEMC)*, pp. 490–497, 2008.
[39] L. Tarisciotti, A. J. Watson, P. Zanchetta, S. Bifaretti, J. C. Clare, and P. W. Wheeler, "An improved Dead-Beat current control for Cascaded H-Bridge active rectifier with low switching frequency," in *IET International Conference on Power Electronics, Machines and Drives (PEMD)*, 2012, pp. 1–6.
[40] V. Biagini, M. Odavic, P. Zanchetta, M. Degano, and P. Bolognesi, "Improved dead beat control of a shunt active filter for aircraft power systems," *IEEE International Symposium on Industrial Electronics (ISIE)*, 2010, pp. 2702–2707.
[41] S. Bifaretti, P. Zanchetta, M. Ciobotaru, F. Iov, and J. C. Clare, "Power flow control through the UNIFLEX-PM under different network conditions," *EPE Journal: European Power Electronics and Drives, vol. 19*, no. December, pp. 32–41, 2009.
[42] P. Zanchetta and D. Gerry, "Predictive current control for multilevel active rectifiers with reduced switching frequency," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 163–172, 2008.
[43] R. Betz and G. Mirzaeva, "Feed-forward compensation for multilevel cascaded h-bridge statcoms," *European Conference on Power Electronics and Applications (EPE)*, vol. Power Elec, pp. 1 – 10, 2009.
[44] A. J. Watson, G. Mondal, and H. Dang, "Construction and Testing of the 3.3 kV, 300 kVA UNIFLEX-PM Prototype," *EPE Journal: European Power Electronics and Drives*, vol. 19, no. December, pp. 59–64, 2009.
[45] L. Tarisciotti, P. Zanchetta, A. J. Watson, J. C. Clare, and S. Bifaretti, "A comparison between Dead-Beat and Predictive control for a 7-Level Back-To-Back Cascaded H-Bridge under fault conditions," *IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 2147–2154, 2013.
[46] A. J. Watson, P. W. Wheeler, and J. C. Clare, "Field programmable gate array based control of Dual Active Bridge DC/DC Converter for the UNIFLEX-PM project," *European Conference on Power Electronics and Applications (EPE)*, 2011, pp. 1–9.

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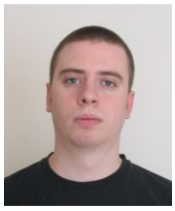

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